GD54/74LS74A

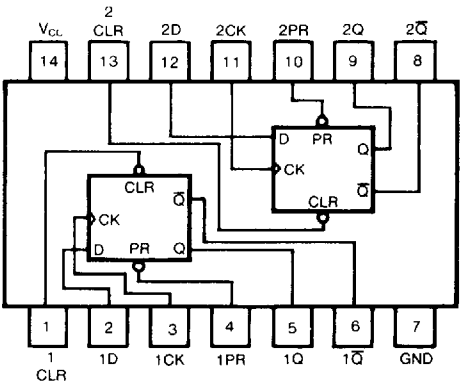
DUAL D-TYPE POSITIVE EDGE-TRIGGERD FLIP-FLOPS WITH PRESET AND CLEAR

Description

This device contains two independent D-type positive edge triggered flip-flops.

A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triger-ing occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

Pin Configuration



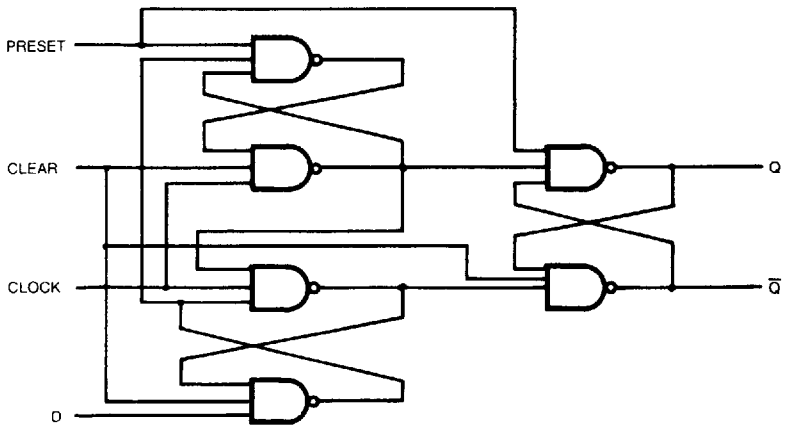
Suffix-Blank Plastic Dual In Line Package
Suffix-J Ceramic Dual In Line Package

Function Table

* The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at preset and clear are near V_{IL} maximum, Furthermore, this configuration is nonstable; that is it will not persist when either preset or clear returns to its inactive (high) level.

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_O	$\overline{Q}_O$

Function Block Diagram



Absolute Maximum Ratings

- Supply voltage, Vcc 7V
- Input voltage 7V
- Operating free-air temperature range 54LS −55°C to 125°C
  74LS 0°C to 70°C
- Storage temperature range −65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		54	4.5	5	5.5	V
			74	4.75	5	5.25	
I_{OH}	High-level output current		54,74			−400	μA
I_{OL}	Low-level output current		54			4	mA
			74			8	
f_{clock}	Clock frequency			0		25	MHz
t_w	Pulse width	Clock high		25			ns
		Preset or clear low		25			
t_{su}	Setup time	high-level data		20↑*			ns
		low-level data		20↑*			
t_h	Hold time			5↑*			ns
T_A	Operating free-air temperature		54	−55		125	°C
			74	0		70	

* ↑ for rising edge

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT
V_{IH}	High level input voltage				2			V
V_{IL}	Low-level input voltage			54			0.7	V
				74			0.8	
V_{IK}	Input clamp voltage	V_{CC}=Min, I_I=−18mA					−1.5	V
V_{OH}	High level output voltage	V_{CC}=Min, V_{IL}=Max		54	2.5	3.4		V
		I_{OH}=Max, V_{IH}=Min		75	2.7	3.4		
V_{OL}	Low level output voltage	V_{CC}=Min, V_{IL}=Max, V_{IH}=Min	I_{OL}=4mA	54,74		0.25	0.4	V
			I_{OL}=8mA	74		0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC}=Max, V_I=7V	D, CK				0.1	mA
			PR, CLR				0.2	
I_{IH}	High-level input current	V_{CC}=Max, V_I=2.7V	D, CK				20	μA
			PR, CLR				40	
I_{IL}	Low-level input current	V_{CC}=Max, V_I=0.4V	D, CK				−0.4	mA
			PR, CLR				−0.8	
I_{OS}	Short-circuit output current	V_{CC}=Max (Note 2)			−20		−100	mA
I_{CC}	Supply current	V_{CC}=Max (Note 3)				4	8	mA

Note 1 All typical values are at V_{CC}=5V, T_A=25°C
Note 2 Not more than one should be shorted at a time and the duration should not exceed one second
Note 3 I_{CC} is measured with all inputs grounded and all outputs open

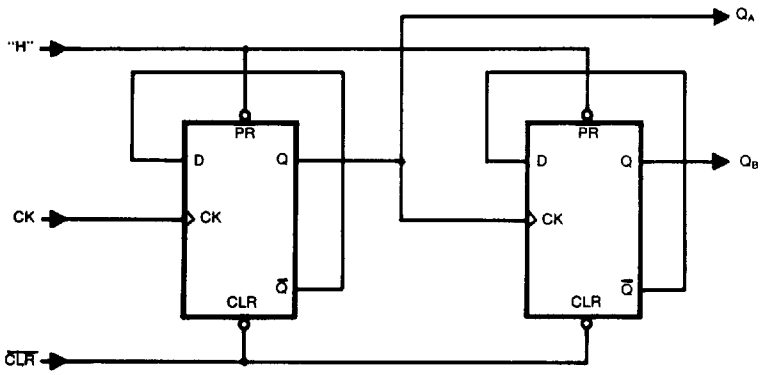
Switching Characteristics, $V_{CC}=5V$, $T_A=25°C$

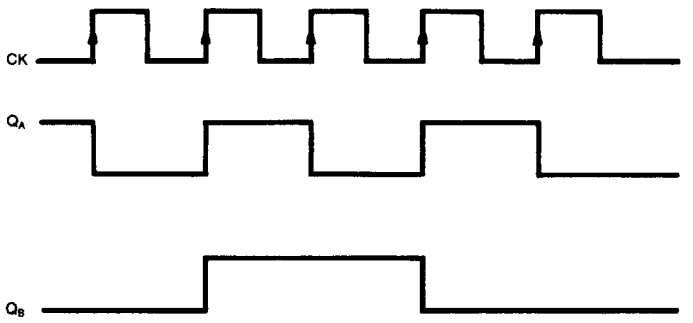
SYMBOL*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION#	MIN	TYP	MAX	UNIT
f_{max}			$C_L=15pF$	25	33		MHz
t_{PLH}	Clear, preset or Clock (as appropriate)	Q or $\overline{Q}$	$R_L=2K\Omega$		13	25	ns
t_{PHL}					25	40	

* f_{max}=maximum clock frequency
* t_{PLH}=propagation delay time, low-to-high-level output
* t_{PHL}=propagation delay time, high-to-low-level output.

#For load circuit and voltage waveforms, see page 3-11.

Application Example
¼ divider





#For load circuit and voltage waveforms, see page 3-12.