Low Voltage PLL Clock Driver

MPC956

LOW VOLTAGE PLL CLOCK DRIVER

The MPC956 is a 3.3V PLL based clock driver designed explicitly to support the MPC601 and MPC601+ microprocessor. The device synthesizes all of the current and future MPC601 processor frequencies from a 33.33MHz crystal source. The three processor clocks lag the BCLK's by one VCO period to ease system integration. For system architectures which support an asynchronous PCI bus a buffered copy of the 33.33MHz is provided. This output can be fanout further via the MPC903 to provide the PCI bus clocks.

- Provide PowerPC™ 601 Clocks (66, 80 and 100 MHz)
- Support ÷2, ÷3 and ÷4 Bus Modes
- Fully Integrated PLL
- Output Frequencies Synthesized from Single 33.33MHz Crystal
- Output Frequency Up to 200MHz
- Output–Output Skew 500ps
- Provides Asynchronous PCI Clock
- Power Management Features
- 3.3V V_{CC}
- 32–Lead TQFP Packaging
- ±150ps Cycle–to–Cycle PLL Jitter

FA SUFFIX
TQFP PACKAGE
CASE 873-01

The MPC956 provides a special power down mode for system power management. The scheme simplifies the design of a system which meets the Energy Star requirements. When asserted (driven to a logic HIGH) the Doze pin will seemlessly reduce all of the output frequencies of the chip. The reductions are implemented in a fashion to minimize power while keeping enough speed to not hamper the performance to the end user. Because the frequency reduction is timed internally there is no need to halt the system to implement the power down mode.

The 4 select pins choose among 14 possible ouput configurations. The configurations were chosen to represent the most common PowerPC 601 and PowerPC 601+ system applications. The outputs are synthesized from a 33.33MHz crystal, this crystal input is also buffered and provides a an output for use with an aynchronous PCI bus.

The MPC956 works from a 3.3V supply and is packaged in a 32 lead TQFP to optimize performance and board space requirements.

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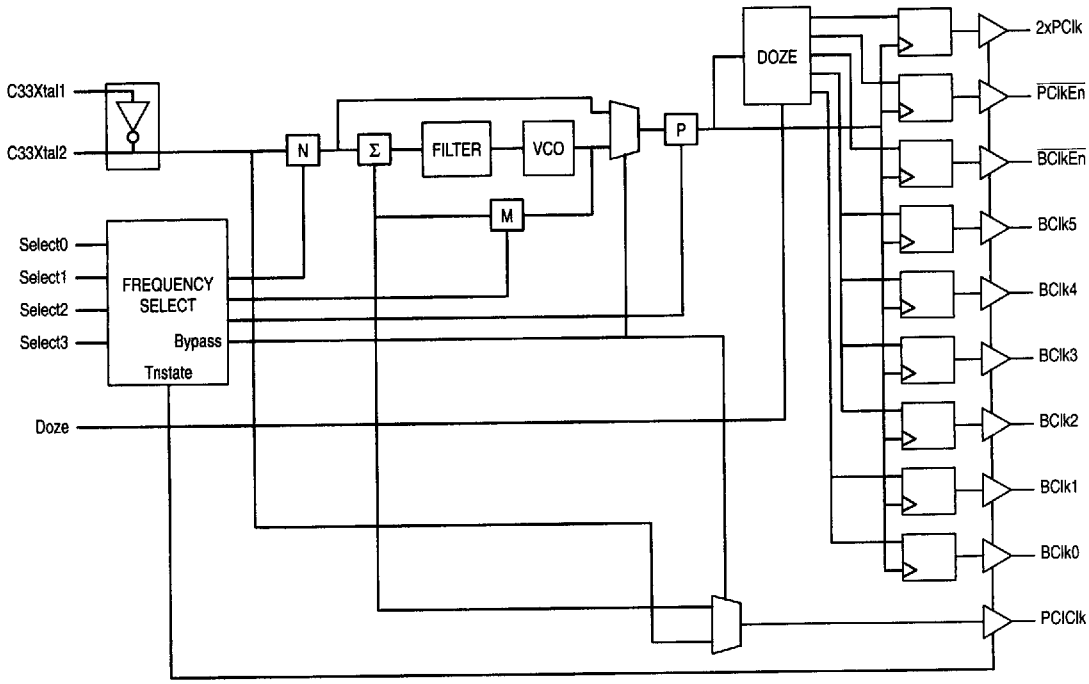
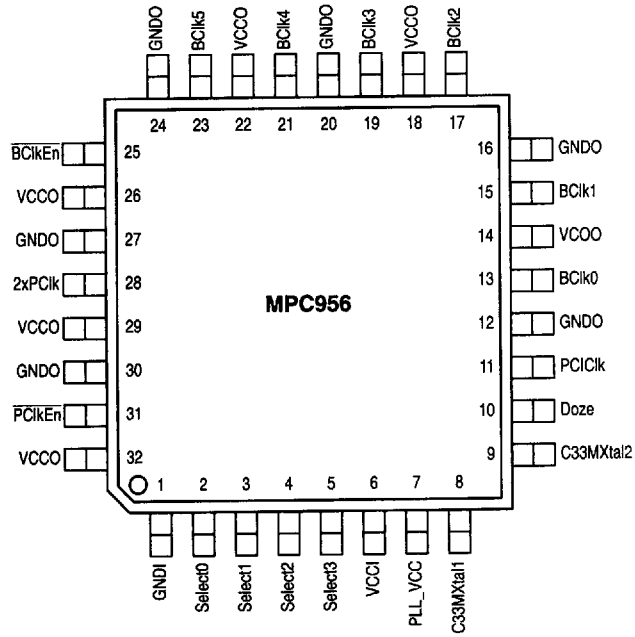
MOTOROLA

MPC956 LOGIC DIAGRAM





MPC956 OUTPUT FREQUENCIES

Select	2xPClk	2xPClk, Doze	$\overline{\text{PClkEn}}$	$\overline{\text{BClkEn}}$, BClkn	$\overline{\text{PClkEn}}$, $\overline{\text{BClkEn}}$, BClkn, Doze
0	133.33	33.33	66.66	33.33	16.66
1	160	40	80	40	20
2	160	40	80	26.67	20
3	200	50	100	50	25
4	200	50	100	33.33	25
5	240	60	120	60	30
6	240	60	120	40	30
7	240	60	120	30	30
8	266.66	66.66	133.33	66.67	33.33
9	266.66	66.66	133.33	44.44	33.33
10	266.66	66.66	133.33	33.33	33.33
11	300	75	150	75	37.50
12	300	75	150	50	37.50
13	300	75	150	37.50	37.50

*Current product only specified for 2xPClk of ≤200MHz.

DC CHARACTERISTICS (T_A = 0° to 70°C)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{DD}	Power Supply Voltage	3.0		3.8	V	
V_{IL}	Input LOW Voltage			$0.3V_{DD}$	V	
V_{IH}	Input HIGH Voltage	$0.7V_{DD}$		V_{DD}	V	
V_{OH}	Output HIGH Voltage	V_{DD} –0.4			V	
V_{OL}	Output LOW Voltage			0.4	V	
C_{IN}	Input Capacitance			4.5	pF	

AC CHARACTERISTICS (T_A = 0° to 70°C, V_{CC} = 3.3V ±0.3V)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
f_{Xtal}	Input Crystal Frequency		20		40	MHz	
f_{max}	Maximum Output Frequency	2xPLCK $\overline{\text{PCLKEN}}$ BCLK			200 100 50	MHz	1.4V, Z_o = 50Ω
t_{dc}	Output Duty Cycle	2xPCLK Other	35 45		65 55	%	1.4V, Z_o = 50Ω
t_{jitter}	PLL Cycle–to–Cycle Jitter (Peak–to–Peak)				±150	ps	Note 2
t_{skew}	Output–to–Output Skew	BLCK 2xPCLK, $\overline{\text{PCLKEN}}$, $\overline{\text{BCLKEN}}$		300 300	500 500	ps	1.4V, Z_o = 50Ω
t_{per}	Minimum Output Period	2xPCLK	4.85			ns	Fout2xP = 200MHz
t_{pw}	2xPCLK Pulse Width		1.75			ns	Fout2xP = 200MHz
t_{pskew}	BCLK to 2xPCLK Skew		$1/f_{VCO}$ –900		$1/f_{VCO}$	ps	Fout2xP ≤ 200MHz
t_{delay}	Time Delay	2xPCLK to $\overline{\text{BCLKEN}}$	50		550	ps	Note 1, 1.4V, Z_o = 50Ω
t_r, t_f	Output Rise/Fall Time				0.8	ns	1.0 to 1.8V, 1.4V, Z_o = 50Ω
t_{LOCK}	PLL Lock Time				10	ms	
t_{PZL}, t_{PZH}	Output Enable Time				20	ns	
t_{PLZ}, t_{PHZ}	Output Disable Time				20	ns	

1. Guaranteed to meet setup/hold times for the PowerPC™ 601 processor.
2. Guaranteed but not tested.

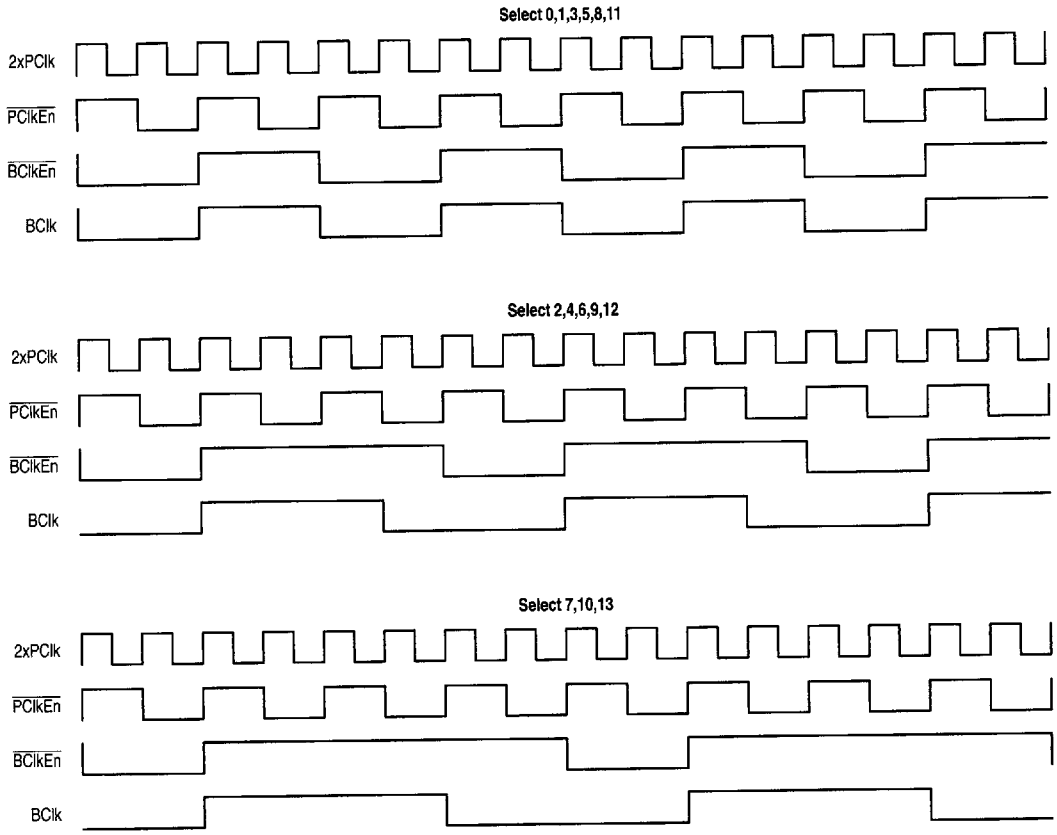


Figure 1. Timing Diagrams for Select Options
(For clarity, processor clock lag not shown)

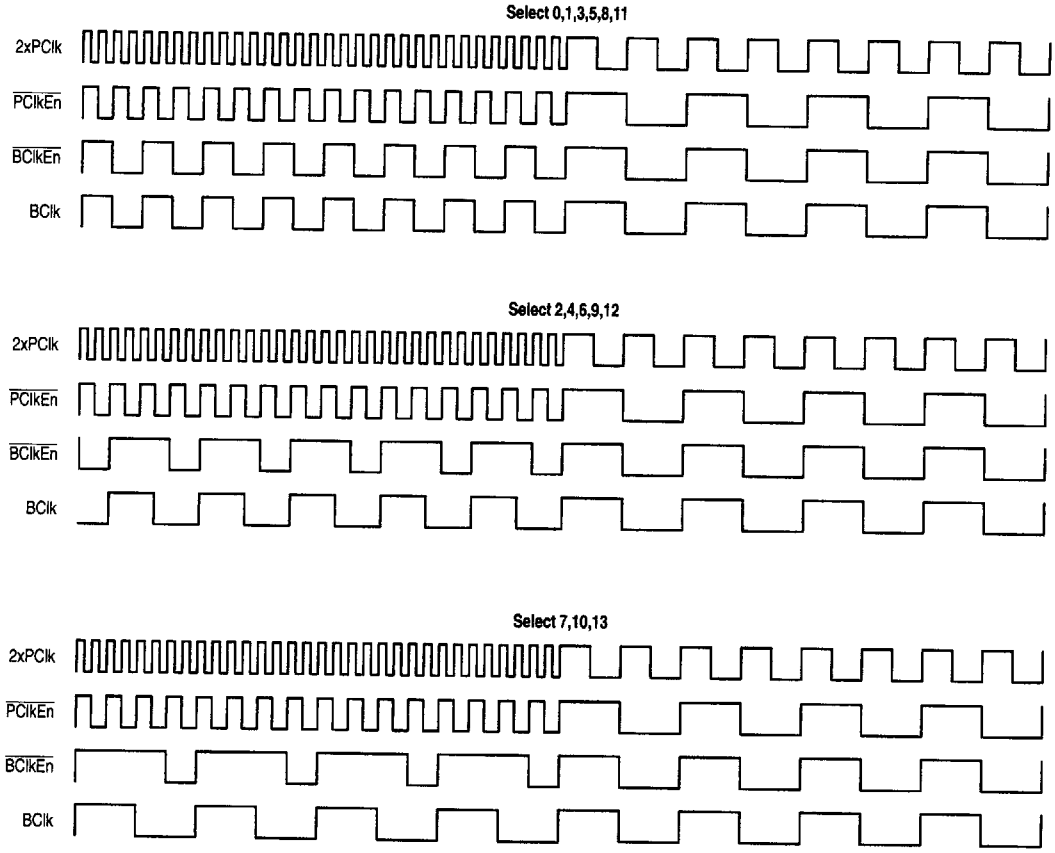


Figure 2. Timing Diagrams for Doze Mode Transitions
(For clarity, processor clock lag not shown)