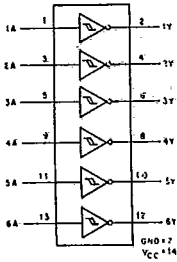


**CD54/74HC14
CD54/74HCT14**

File Number 1781

High-Speed CMOS Logic



Hex Inverting Schmitt Trigger

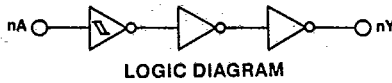
Type Features:

- Unlimited input rise and fall times
- Exceptionally high noise immunity

FUNCTIONAL DIAGRAM AND TERMINAL ASSIGNMENT

The RCA-CD54/74HC14 and CD54/74HCT14 each contain 6 inverting Schmitt Triggers in one package.

The CD54HC14 and CD54HCT14 are supplied in 14-lead ceramic dual-in-line packages (F suffix). The CD74HC14 and CD74HCT14 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface mount plastic packages (M suffix). Both devices are also available in chip form (H suffix).



LOGIC DIAGRAM

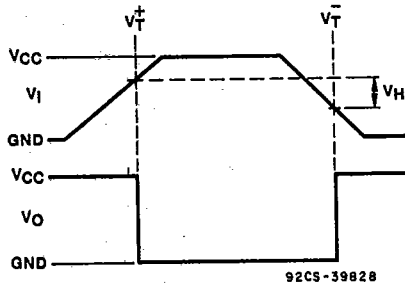
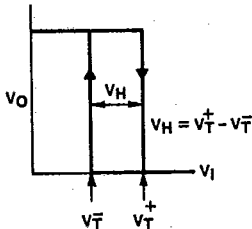


Fig. 1 - Hysteresis definition, characteristic, and test setup.

Family Features:

- Fanout (Over Temperature Range):
Standard Outputs - 10 LSTTL Loads
Bus Driver Outputs - 15 LSTTL Loads
- Wide Operating Temperature Range:
CD74HC/HCT: -40 to +85°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- Alternate Source is Philips/Signetics
- CD54HC/CD74HC Types:
2 to 6 V Operation
High Noise Immunity:
 $N_{IL} = 37\%$, $N_{IH} = 51\%$ of V_{CC} ; @ $V_{CC} = 5V$
- CD54HCT/CD74HCT Types:
4.5 to 5.5 V Operation
Direct LSTTL Input Logic Compatibility
 $N_{IL} = 18\%$, $N_{IH} = 67\%$ of V_{CC} @ $V_{CC} = 4.5V$
CMOS Input Compatibility
 $I_i \leq 1 \mu A$ @ V_{OL} , V_{OH}

TRUTH TABLE

INPUT	OUTPUT
A	Y
L	H
H	L

H = High Level
L = Low Level

HARRIS SEMICONDUCTOR SECTOR 27E D 430227J 0017483 4 HAS

HARRIS SEMICONDUCTOR 27E D 430227J 0017484 6 HAS

T-51-21

Technical Data

**CD54/74HC14
CD54/74HCT14**

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) -0.5 to +7 V

DC INPUT DIODE CURRENT, I_{IK} (FOR $V_i < -0.5$ V OR $V_i > V_{CC} + 0.5$ V) ± 20 mA

DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_o < -0.5$ V OR $V_o > V_{CC} + 0.5$ V) ± 20 mA

DC DRAIN CURRENT, PER OUTPUT (I_o) (FOR -0.5 V < V_o < $V_{CC} + 0.5$ V) ± 25 mA

DC V_{CC} OR GROUND CURRENT (I_{CC}) ± 50 mA

POWER DISSIPATION PER PACKAGE (P_o):

For $T_A = -40$ to $+60^\circ$ C (PACKAGE TYPE E) 500 mW

For $T_A = +60$ to $+85^\circ$ C (PACKAGE TYPE E) Derate Linearly at 8 mW/ $^\circ$ C to 300 mW

For $T_A = -55$ to $+100^\circ$ C (PACKAGE TYPE F, H) 500 mW

For $T_A = +100$ to $+125^\circ$ C (PACKAGE TYPE F, H) Derate Linearly at 8 mW/ $^\circ$ C to 300 mW

For $T_A = -40$ to $+70^\circ$ C (PACKAGE TYPE M) 400 mW

For $T_A = +70$ to $+125^\circ$ C (PACKAGE TYPE M) Derate Linearly at 6 mW/ $^\circ$ C to 70 mW

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPE F, H -55 to $+125^\circ$ C

PACKAGE TYPE E, M -40 to $+85^\circ$ C

STORAGE TEMPERATURE (T_{stg}) -65 to $+150^\circ$ C

LEAD TEMPERATURE (DURING SOLDERING):

At distance $1/16 \pm 1/32$ in. (1.59 ± 0.79 mm) from case for 10 s max. $+265^\circ$ C

Unit inserted into a PC Board. (min. thickness $1/16$ in., 1.59 mm) $+300^\circ$ C

with solder contacting lead tips only $+300^\circ$ C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For $T_A =$ Full Package-Temperature Range) V_{CC} .*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_i, V_o	0	V_{CC}	V
Operating Temperature T_A :			
CD74 Types	-40	+85	$^\circ$ C
CD54 Types	-55	+125	$^\circ$ C
Input Rise and Fall Times t_r, t_f			
at 2 V	0	Unlimited	ns
at 4.5 V	0	Unlimited	ns
at 6 V	0	Unlimited	ns

*Unless otherwise specified, all voltages are referenced to Ground.

HARRIS SEMICONDUCTOR 27E D 430227J 0017486 T HAS

T-51-21

Technical Data

CD54/74HC14 CD54/74HCT14

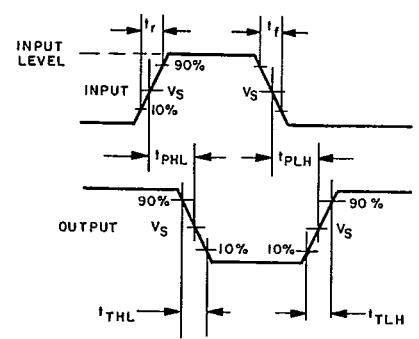
SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_A = 25^\circ C$, Input $t_r, t_f = 6 ns$)

CHARACTERISTIC	CL (pF)	TYPICAL		UNITS
		HC	HCT	
Propagation Delay, A to Y t_{PHL}, t_{PLH}	15	11	16	ns
Power Dissipation Capacitance* C_{PD}	—	20	20	pF

* C_{PD} is used to determine the dynamic power consumption, per inverter.
 $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where: f_i = input frequency
 C_L = output load capacitance
 V_{CC} = supply voltage

SWITCHING CHARACTERISTICS ($C_L = 50 pF$, Input $t_r, t_f = 6 ns$)

CHARACTERISTIC	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS
		HC		HCT		74HC		74HCT		54HC		54HCT		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Propagation Delay, A to Y t_{PLH} t_{PHL}	2	—	135	—	—	170	—	—	—	205	—	—	ns	
	4.5	—	27	—	38	—	34	—	48	—	41	—		57
	6	—	23	—	—	29	—	—	—	35	—	—		—
Output Transition Time t_{TLH} t_{THL}	2	—	75	—	—	95	—	—	—	110	—	—	ns	
	4.5	—	15	—	15	—	19	—	19	—	22	—		22
	6	—	13	—	—	16	—	—	—	19	—	—		—
Input Capacitance C_i	—	—	10	—	10	—	10	—	10	—	10	—	10	pF



	54/74HC	54/74HCT
INPUT LEVEL	V_{CC}	3V
V_S	50% V_{CC}	1.3V

92CS-36948RI

Fig. 2 - Transition times and propagation delay times.