Integrated Circuit Systems, Inc.

ICS951403

AMD-K7™ System Clock Chip

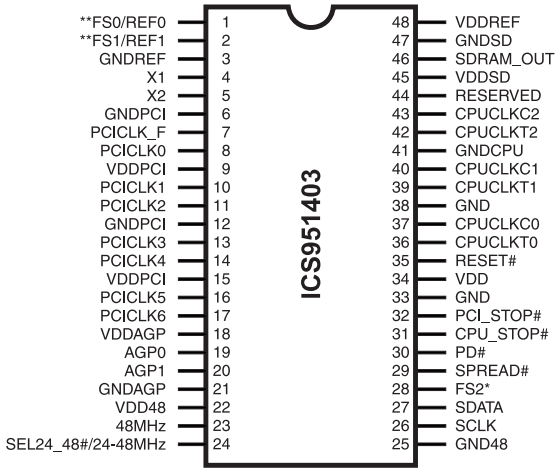
Recommended Application:
ATI chipset with K7 systems
Output Features:

- 3 differential pair open drain CPU clocks (1.5V external pull-up; up to 150MHz achieviable through I^2C)
- 2 - AGPCLK @ 3.3V
- 8 - PCI @3.3V, including 1 free running
- 1 - 48MHz @ 3.3V
- 1 - 24/48MHz @ 3.3V
- 2- REF @3.3V, 14.318MHz.

Features:

- Programmable ouput frequency
- Programmable ouput rise/fall time
- Programmable group skew
- Real time system reset output
- Spread spectrum for EMI control typically by 7dB to 8dB, with programmable spread percentage
- Watchdog timer technology to reset system if over-clocking causes malfunction
- Uses external 14.318MHz crystal
- Asyncronous CPU and SDRAM clocks
- CPU and PCI outputs are aligned
- CPU - AGP skew <500ps

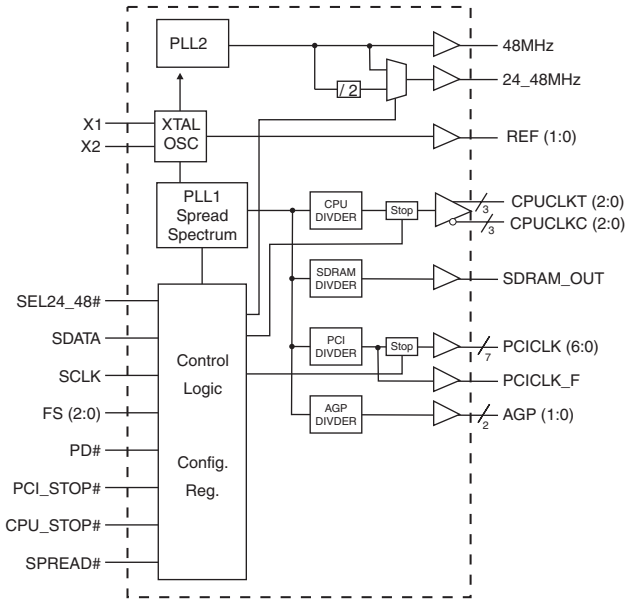
Pin Configuration



48-Pin SSOP & TSSOP

* Internal 120K pullup resistor on indicated inputs
** Internal 240K pullup resistor on indicated inputs

Block Diagram



Functionality

Bit 7	FS2	FS1	FS0	CPU	SDRAM	PCICLK	AGP SEL = 0	AGP SEL = 1
0	0	0	0	100.00	100.00	33.33	66.67	50.00
0	0	0	1	100.00	133.33	33.33	66.67	50.00
0	0	1	0	100.00	150.00	30.00	60.00	50.00
0	0	1	1	100.00	66.67	33.33	66.67	50.00
0	1	0	0	133.33	133.33	33.33	66.67	50.00
0	1	0	1	125.00	100.00	31.25	62.50	50.00
0	1	1	0	124.00	124.00	31.00	62.00	46.50
0	1	1	1	133.33	100.00	33.33	66.67	50.00
1	0	0	0	112.00	112.00	33.60	67.20	56.00
1	0	0	1	150.00	150.00	30.00	60.00	50.00
1	0	1	0	111.11	166.67	33.33	66.67	55.56
1	0	1	1	110.00	165.00	33.00	66.00	55.00
1	1	0	0	166.67	166.67	33.33	66.67	55.56
1	1	0	1	90.00	90.00	30.00	60.00	45.00
1	1	1	0	48.00	48.00	32.00	64.00	48.00
1	1	1	1	45.00	60.00	30.00	60.00	45.00

Power Groups

VDD48, GND48 = 48MHz, PLL2
VDDREF, GNDREF= REF, X1, X2
VDD, GND = PLL Core

General Description

The **ICS951403** is a main clock synthesizer chip for AMD-K7 based systems with ATI chipset. This provides all clocks required for such a system.

The **ICS951403** belongs to ICS new generation of programmable system clock generators. It employs serial programming I^2C interface as a vehicle for changing output functions, changing output frequency, configuring output strength, configuring output to output skew, changing spread spectrum amount, changing group divider ratio and dis/enabling individual clocks. This device also has ICS propriety 'Watchdog Timer' technology which will reset the frequency to a safe setting if the system become unstable from over clocking.

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
2,1	FS (1:0)	IN	Frequency Select pins, has pull-up to VDD
	REF (1:0)	OUT	14.318MHz clock output
3, 6, 21, 25, 33, 38, 41, 47	GND	PWR	Ground
4	X1	IN	XTAL_IN 14.318MHz Crystal input, has internal 33pF load cap and feed back resistor from X2
5	X2	OUT	XTAL_OUT Crystal output, has internal load cap 33pF
7	PCICLK_F	OUT	Free Running PCI output. Not affected by the PCI_STOP# input.
17, 16, 14, 13, 11, 10, 8	PCICLK (6:0)	OUT	PCI clock outputs. TTL compatible 3.3V
9, 15	VDDPCI	PWR	Power for PCICLK outputs, nominally 3.3V
18	VDDAGP	PWR	Power for AGP outputs, nominally 3.3V
20, 19	AGP (1:0)	OUT	AGP outputs defined as 2X PCI. These may not be stopped.
34	VDD	PWR	Isolated power for core, nominally 3.3V
22	VDD48	PWR	Power for 48MHz and 24MHz outputs nominally 3.3V
23	48MHz	OUT	48MHz output
24	SEL24-48#	IN	Selects 24 or 48MHz output for pin 24 Low = 48MHz High = 24MHz
	24-48MHz	OUT	Fixed clock out selectable through SEL24-48#
26	SCLK	IN	Clock pin of I^2C circuitry 5V tolerant
27	SDATA	I/O	Data pin for I^2C circuitry 5V tolerant
28	FS2	IN	Frequency Select pin, has pull-up to VDD
29	SPREAD#	IN	Enables Spread Spectrum feature when LOW. Down Spread 0.5% modulation frequency =50KHz
30	PD#	IN	Powers down chip, active low. Internal PLL & all outputs are disabled.
31	CPU_STOP#	IN	Halts CPUCLKs. CPUCLKT is driven LOW wheras CPUCLKC is driven HIGH when this pin is asserted (Active LOW).
32	PCI_STOP#	IN	Halts PCI Bus at logic "0" level when driven low. PCICLK_F is not affected by this pin
35	RESET#	OUT	Real time system reset signal for watchdog tmer timeout. This signal is active low.
46	SDRAM_OUT	OUT	Reference clock for SDRAM zero delay buffer
44	RESERVED	N/C	Future CPU power rail
42, 39, 36	CPUCLKT (2:0)	OUT	"True" clocks of differential pair CPU outputs. These open drain outputs need an external 1.5V pull-up.
43, 40, 37	CPUCLKC (2:0)	OUT	"Complementary" clocks of differental pair CPU output. These open drain outputs need an external 1.5V pull_up.
45	VDDSD	PWR	Power for SDRAM_OUT pin. Norminally 3.3V
48	VDDREF	PWR	Power for REF, X1, X2, nominally 3.3V

Bit		Description										PWD
	Bit 2	Bit 7	Bit 6	Bit 5	Bit 4	CPU	SDRAM	PCI	AGP SEL = 0	AGP SEL = 1	Spread Precentage	
			FS2	FS1	FS0							
Bit 2 Bit 7:4	0	0	0	0	0	100.00	100.00	33.33	66.67	50.00	0 to -0.5% Down Spread	0000-0 Note1
	0	0	0	0	1	100.00	133.33	33.33	66.67	50.00	0 to -0.5% Down Spread	
	0	0	0	1	0	100.00	150.00	30.00	60.00	50.00	+/- 0.25% Center Spread	
	0	0	0	1	1	100.00	66.67	33.33	66.67	50.00	0 to -0.5% Down Spread	
	0	0	1	0	0	133.33	133.33	33.33	67.67	50.00	0 to -0.5% Down Spread	
	0	0	1	0	1	125.00	100.00	31.25	62.50	50.00	+/- 0.25% Center Spread	
	0	0	1	1	0	124.00	124.00	31.00	62.00	46.50	+/- 0.25% Center Spread	
	0	0	1	1	1	133.33	100.00	33.33	66.67	50.00	0 to -0.5% Down Spread	
	0	1	0	0	0	112.00	112.00	33.60	67.20	56.00	+/- 0.25% Center Spread	
	0	1	0	0	1	150.00	150.00	30.00	60.00	50.00	+/- 0.25% Center Spread	
	0	1	0	1	0	111.11	166.67	33.33	66.67	55.56	+/- 0.25% Center Spread	
	0	1	0	1	1	110.00	165.00	33.00	66.00	55.00	+/- 0.25% Center Spread	
	0	1	1	0	0	166.67	166.67	33.33	66.67	55.56	+/- 0.25% Center Spread	
	0	1	1	0	1	90.00	90.00	30.00	60.00	45.00	+/- 0.25% Center Spread	
	0	1	1	1	0	48.00	48.00	32.00	64.00	48.00	+/- 0.25% Center Spread	
	0	1	1	1	1	45.00	60.00	30.00	60.00	45.00	+/- 0.25% Center Spread	
	1	0	0	0	0	100.30	100.30	33.43	66.87	50.15	+/- 0.25% Center Spread	
	1	0	0	0	1	100.30	133.73	33.43	66.87	50.15	+/- 0.25% Center Spread	
	1	0	0	1	0	105.00	157.50	31.50	63.00	52.50	+/- 0.25% Center Spread	
	1	0	0	1	1	100.30	66.87	33.43	66.87	50.15	+/- 0.25% Center Spread	
	1	0	1	0	0	110.00	110.00	33.00	66.00	55.00	+/- 0.25% Center Spread	
	1	0	1	0	1	103.00	103.00	34.33	68.67	51.50	+/- 0.25% Center Spread	
	1	0	1	1	0	103.00	137.33	34.33	68.67	51.50	+/- 0.25% Center Spread	
	1	0	1	1	1	133.73	100.30	33.43	66.87	50.15	+/- 0.25% Center Spread	
	1	1	0	0	0	133.73	133.73	33.43	66.87	50.15	+/- 0.25% Center Spread	
	1	1	0	0	1	140.00	140.00	35.00	70.00	52.50	+/- 0.25% Center Spread	
	1	1	0	1	0	137.33	103.00	34.33	68.67	51.50	+/- 0.25% Center Spread	
	1	1	0	1	1	137.33	137.33	34.33	68.67	51.50	+/- 0.25% Center Spread	
	1	1	1	0	0	105.00	105.00	35.00	70.00	52.50	+/- 0.25% Center Spread	
	1	1	1	0	1	138.33	138.33	34.58	69.17	51.88	+/- 0.25% Center Spread	
	1	1	1	1	0	200.00	200.00	33.33	66.67	50.00	+/- 0.25% Center Spread	
	1	1	1	1	1	104.25	139.00	34.75	69.50	52.13	+/- 0.25% Center Spread	
Bit 3	0 - Frequency is selected by hardware select, Latched Inputs 1 - Frequency is selected by Bit , 2 7:4											0
Bit 1	0 - Normal 1 - Spread Spectrum Enabled											0
Bit 0	0 - Running 1- Tristate all outputs											0

Note1:
Default at power-up will be for latched logic inputs to define frequency, as displayed by Bit 3.

Note: PWD = Power-Up Default

Byte 1: Output Control Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	24	1	SEL 24/48 0 = 24MHz 1= 48MHz
Bit 6	37	1	CPUCLKC0
Bit 5	36	1	CPUCLKT0
Bit 4	40	1	CPUCLKC1
Bit 3	39	1	CPUCLKT1
Bit 2	43	1	CPUCLKC2
Bit 1	42	1	CPUCLKT2
Bit 0	46	1	SDRAM_OUT

Byte 2: PCI Stop Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	7	1	PCICLK_F
Bit 6	17	1	PCICLK6
Bit 5	16	1	PCICLK5
Bit 4	14	1	PCICLK4
Bit 3	13	1	PCICLK3
Bit 2	11	1	PCICLK2
Bit 1	10	1	PCICLK1
Bit 0	8	1	PCICLK0

Byte 3: CPU Free Running Control Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	Reserved
Bit 6	-	X	Reserved
Bit 5	-	X	Reserved
Bit 4	-	X	Reserved
Bit 3	-	0	Reserved
Bit 2	-	0	CPU T/C 0
Bit 1	-	0	CPU T/C 1
Bit 0	-	0	CPU T/C 2

Byte 4: 24/48MHz Control Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
7	-	1	Reserved
6	24	1	24-48MHz
5	-	1	48MHz
4	-	1	Reserved
3	-	1	Reserved
2	-	1	Reserved
1	-	0	AGP frequency select 0 = 66.6MHz 1 = 50.0MHz
0	-	1	Reserved

Byte 5: Clock Enable Control Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
7	-	X	Reserved
6		X	FS2 Read-back
5		X	FS1 Read-back
4		X	FS0 Read-back
3	1	1	REF1
2	2	1	REF0
1	20	1	AGP1
0	19	1	AGP0

Notes:
1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched Frequency Selects (FS#) will be inverted logic load of the input frequency select pin conditions.

Byte 6: Control Register
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
7	-	0	REF strength 0 = 1X 1 = 2X
6	-	0	0 = CPU C1:2, T1:2 stop 1 = CPU C1:2, T1:2 free running
5	-	0	Reserved
4	-	X	SPREAD# read-back
3	-	X	CPU_STOP# read-back
2	-	X	PCI_STOP# read-back
1	-	X	Reserved
0	-	0	AGP speed toggle

Notes:
3. Bytes 7:14 not defined.

Byte 15: CPU_SDRAM Skew Register

Bit	PWD	Description
Bit 7	1	SDRAM (pdel canned)
Bit 6	0	
Bit 5	0	Reserved
Bit 4	1	
Bit 3	1	CPUC0 & T0 (pdel canned)
Bit 2	1	
Bit 1	1	CPUC 1:2 & T 1:2 (pdel canned)
Bit 0	0	

Byte 16: Slew Rate Control Register

Bit	PWD	Description
Bit 7	-	Reserved
Bit 6	-	Reserved
Bit 5	-	Reserved
Bit 4	-	Reserved
Bit 3	-	Reserved
Bit 2	-	Reserved
Bit 1	-	Reserved
Bit 0	-	Reserved

Byte 17: Slew Rate Control Register

Bit	PWD	Description
Bit 7	1	PCI (3:0) Slew Control
Bit 6	0	
Bit 5	1	PCI_F Slew Control
Bit 4	0	
Bit 3	1	CPUCLKC0 Slew Control
Bit 2	0	
Bit 1	1	CPUCLKT0 Slew Control
Bit 0	0	

Byte 18: Slew Rate Control Register

Bit	PWD	Description
Bit 7	1	PCI (4:7) Slew Control
Bit 6	0	
Bit 5	1	AGP1 Slew Control
Bit 4	0	
Bit 3	1	AGP0 Slew Control
Bit 2	0	
Bit 1	1	Reserved
Bit 0	0	

Byte 19: Slew Rate Control Register

Bit	PWD	Description
Bit 7	1	48MHz Slew Control
Bit 6	0	
Bit 5	1	24, 48MHz Slew Control
Bit 4	0	
Bit 3	1	REF0 Slew Control
Bit 2	0	REF1 Slew Control
Bit 1	1	SDRAM Slew Control
Bit 0	0	

Byte 20: Slew Rate Control Register

Bit	PWD	Description
Bit 7	1	CPUCLKC1 Slew Control
Bit 6	0	
Bit 5	1	CPUCLKT1 Slew Control
Bit 4	0	
Bit 3	1	CPUCLKC2 Slew Control
Bit 2	0	
Bit 1	1	CPUCLKT2 Slew Control
Bit 0	0	

Notes:

1. PWD = Power on Default

VCO Programming Constrains

VCO Frequency ..... 150MHz to 500MHz

VCO Divider Range ..... 8 to 519

REF Divider Range ..... 2 to 129

Phase Detector Stability ..... 0.3536 to 1.4142

Useful Formula

VCO Frequency = 14.31818 x VCO/REF divider value

Phase Detector Stabiliy = 14.038 x (VCO divider value)$^{-0.5}$

To program the VCO frequency for over-clocking.

0. Before trying to program our clock manually, consider using ICS provided software utilities for easy programming.

1. Select the frequency you want to over-clock from with the desire gear ratio (i.e. CPU:SDRAM:3V66:PCI ratio) by writing to byte 0, or using initial hardware power up frequency.

2. Write 0001, 1001 (19_H) to byte 8 for readback of 21 bytes (byte 0-20).

3. Read back byte 11-20 and copy values in these registers.

4. Re-initialize the write sequence.

5. Write a '1' to byte 9 bit 7 and write to byte 11 & 12 with the desired VCO & REF divider values.

6. Write to byte 13 to 20 with the values you copy from step 3. This maintains the output spread, skew and slew rate.

7. The above procedure is only needed when changing the VCO for the 1st pass. If VCO frequency needed to be changed again, user only needs to write to byte 11 and 12 unless the system is to reboot.

Note:

1. User needs to ensure step 3 & 7 is carried out. Systems with wrong spread percentage and/or group to group skew relation programmed into bytes 13-16 could be unstable. Step 3 & 7 assure the correct spread and skew relationship.

2. If VCO, REF divider values or phase detector stability are out of range, the device may fail to function correctly.

3. Follow min and max VCO frequency range provided. Internal PLL could be unstable if VCO frequency is too fast or too slow. Use 14.31818MHz x VCO/REF divider values to calculate the VCO frequency (MHz).

4. ICS recommends users, to utilize the software utility provided by ICS Application Engineering to program the VCO frequency.

5. Spread percent needs to be calculated based on VCO frequency, spread modulation frequency and spreadamount desired. See Application note for software support.

Absolute Maximum Ratings

Supply Voltage . . . . . 5.5 V

Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature . . . . . 0°C to +70°C

Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

TA = 0 - 70°C; Supply Volt age VDD = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD} + 0.3	V
Input Low Voltage	V_{IL}		V_{SS} - 0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = VDD			5	A
Input Low Current	I_{IL1}	V_{IN}=0 V; Inputs with no pull-up resistors	-5			uA
Input Low Current	I_{IL2}	V_{IN}=0 V; Inputs with pull-up resistors	-200			uA
Supply Current	$I_{DD3.3OP}$	C_L = Full load		213	240	mA
Power Down	PD			0.07	0.6	mA
Input frequency	Fi	V_{DD} = 3.3 V;	12	14.318	16	MHz
	C_{IN}	Logic Inputs			5	pF
Input Capacitance1	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Clk Stabilization[1]	T_{STAB}	From V_{DD}= 3.3 V to 1% target Freq.			3	ms
Skew[1]	$t_{CPU-SDRAM}$	CPU Xover to SDRAM 1.5V		68	250	ps
Skew[1]	$t_{CPU-PCI}$	CPU Xover to PCI 1.5V		186	250	ps
Skew[1]	$t_{CPU-AGP}$	CPU Xover to AGP 1.5V		138	500	ps

[1] Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -18mA	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = 18mA			0.4	V
Output High Current	I_{OH5}	V OH = 2.0 V,			-19	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8V	19			mA
Rise Time	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V		0.85	4	ns
Fall Time	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.03	4	ns
Duty Cycle	d_{t1}[1]	V_T = 50%	45	54	55	%
Jitter	$t_{jcyc-cyc5}$	V_T = 1.5 V		521	1000	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPU (Open Drain)

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 2pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	Zo	$V_O = V_x$				Ω
Output High Voltage	V_{OH2B}	Termination to Vpull_up (external)	1		1.2	V
Output Low Voltage	V_{OL2B}	Termination to Vpull_up (external)			0.4	
Output Low Current	I_{OL2B}	V_{OL} = 0.3V	18			mA
Fall Time	t_{f2B}	V_{OH} = 1.2V V_{OL} = 0.3V		0.8	0.9	ps
Differential voltage_AC	V_{DIF}	Note 2			Vtpullup (external)+0.6	ps
Differential voltage_DC	V_{DIF}	Note 2			Vtpullup (external)+0.6	ps
Differential Crossover Voltage	V_X	True rise to compl. Fall		1.37	1.5	V
Duty Cycle	d_{t2B}	V_T = 50%	45	49.3	55	%
Skew	t_{sk2B}	V_T = 50%		48	200	ps
Jitter, Cycle to cycle	$t_{jcyc-cyc}$[1]	V_T = Vx		130	250	ps

[1]Guaranteed by design, not 100% tested in production.

[2] V_{DIF} specifies the minimum input differential voltages (VTR-VCP) required for switching, where VTR is the "true" input level and VCP is the "complement" input level.

Electrical Characteristics - PCICLK

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH}[1]	I_{OH} = -11mA	2.6			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 9.4mA			0.4	V
Output High Current	I_{OH}[1]	V OH = 2.0 V,			-19	mA
Output Low Current	I_{OL}[1]	V_{OL} = 0.8V	19			mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		1.29	2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		1.02	2	ns
Duty Cycle	d_{t1}[1]	V_T = 50%	45	51.5	55	%
Skew	t_{sk1}[1]	V_T = 50%		54	200	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		104	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 24MHz,48MHz

TA = 0 - 70°C; VDD = 3.3 V +/-5%; CL = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -18mA	2.4			V
Output Low Voltage	V_{OL5}	I_{OL} = 18mA			0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16			mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, VOH = 2.4 V		1.2	4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, VOL = 0.4 V		1.3	4	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5V	45	50.5	55	%
Jitter, Cycle to cycle	t_{jcyc_cyc2B}	V_T = 1.5V		130	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - AGP [1:0]

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH}[1]	I_{OH} = -18mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 18mA			0.4	V
Output High Current	I_{OH}[1]	V OH = 2.0 V,			-19	mA
Output Low Current	I_{OL}[1]	V_{OL} = 0.8V	19			mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		0.98	1.6	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		0.85	1.6	ns
Duty Cycle	d_{t1}[1]	V_T = 50%	45	48.5	55	%
Skew	t_{sk1}[1]	V_T = 50%		4	250	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		235	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM_OUT

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH3}	I_{OH} = -11mA	2			V
Output Low Voltage	V_{OL3}	I_{OL} = 11mA			0.4	V
Output High Current	I_{OH3}	V OH = 2.0 V,			-12	mA
Output Low Current	I_{OL3}	V_{OL} = 0.8V	12			mA
Rise Time	t_{r3}[3]	V_{OL} = 0.4 V, V_{OH} = 2.4 V		0.96	1.6	ns
Fall Time	tf_3[3]	V_{OH} = 2.4 V, V_{OL} = 0.4 V		0.75	1.6	ns
Duty Cycle	d_{t3}[3]	V_T = 50%	45	49.5	55	%
Jitter	$t_{jcyc-cyc}$[3]	V_T = 1.5 V		235	250	ps

[1]Guaranteed by design, not 100% tested in production.

General I²C serial interface information for the ICS951403

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte 0 through Byte 20*** (see Note)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D2(H)	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Byte 6	
	ACK
○	
○	○
○	○
	○
Byte 18	
	ACK
Byte 19	
	ACK
Byte 20	
	ACK
Stop Bit	

*See notes on the following page.

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends ***Byte 0 through byte 8 (default)***
- ICS clock sends ***Byte 0 through byte X (if $X_{(H)}$ was written to byte 8).***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D3(H)	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
	Byte 6
ACK	
If 7_H has been written to B6	***Byte 7***
ACK	
○	○
○	○
○	○
If 12_H has been written to B6	***Byte18***
ACK	
If 13_H has been written to B6	***Byte 19***
ACK	
If 14_H has been written to B6	***Byte 20***
ACK	
Stop Bit	

Brief I²C registers description for ICS951403 Programmable System Frequency Generator

Register Name	Byte	Description	PWD Default
Functionality & Frequency Select Register	0	Output frequency, hardware / I²C frequency select, spread spectrum & output enable control register.	See individual byte description
Output Control Registers	1-6	Active / inactive output control registers/latch inputs read back.	See individual byte description
Vendor ID & Revision ID Registers	7	Byte 11 bit[7:4] is ICS vendor id - 1001. Other bits in this register designate device revision ID of this part.	See individual byte description
Byte Count Read Back Register	8	Writing to this register will configure byte count and how many byte will be read back. Do not write 00_H to this byte.	08_H
Watchdog Timer Count Register	9	Writing to this register will configure the number of seconds for the watchdog timer to reset.	10_H
Watchdog Control Registers	10 Bit [6:0]	Watchdog enable, watchdog status and programmable 'safe' frequency' can be configured in this register.	000,0000
VCO Control Selection Bit	10 Bit [7]	This bit select whether the output frequency is control by hardware/byte 0 configurations or byte 11&12 programming.	0
VCO Frequency Control Registers	11-12	These registers control the dividers ratio into the phase detector and thus control the VCO output frequency.	Depended on hardware/byte 0 configuration
Spread Spectrum Control Registers	13-14	These registers control the spread percentage amount.	Depended on hardware/byte 0 configuration
Group Skews Control Registers	15-16	Increment or decrement the group skew amount as compared to the initial skew.	See individual byte description
Output Rise/Fall Time Select Registers	17-20	These registers will control the output rise and fall time.	See individual byte description

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. Readback will support standard SMBUS controller protocol. **The number of bytes to readback is defined by writing to byte 8.**
2. **When writing to byte 11 - 12, and byte 13 - 14, they must be written as a set.** If for example, only byte 14 is written but not 15, neither byte 14 or 15 will load into the receiver.
3. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
4. The input is operating at 3.3V logic levels.
5. The data byte format is 8 bit bytes.
6. To simplify the clock generator I²C interface, the protocol is set to use only Block-Writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
7. At power-on, all registers are set to a default condition, as shown.

0486B—02/23/04

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

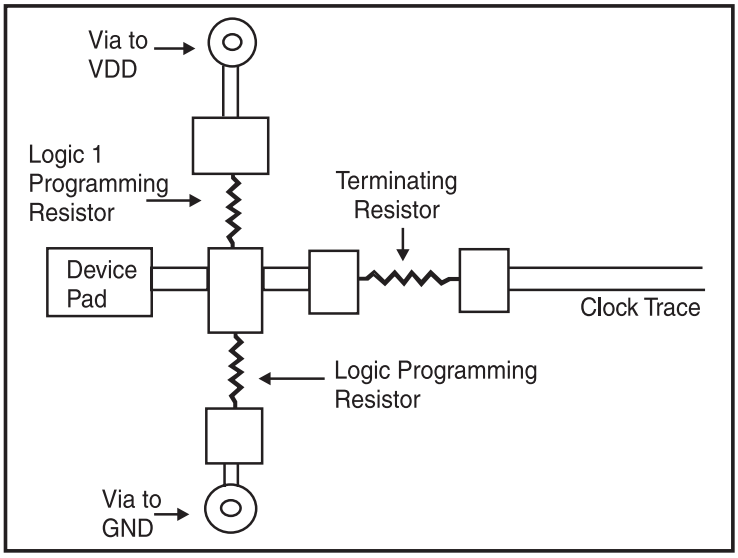
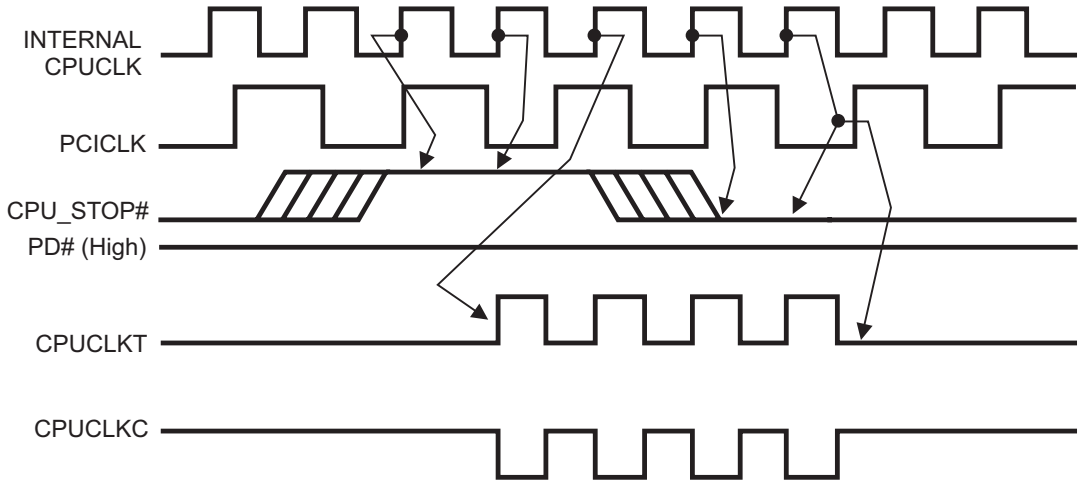


Fig. 1

CPU_STOP# Timing Diagram

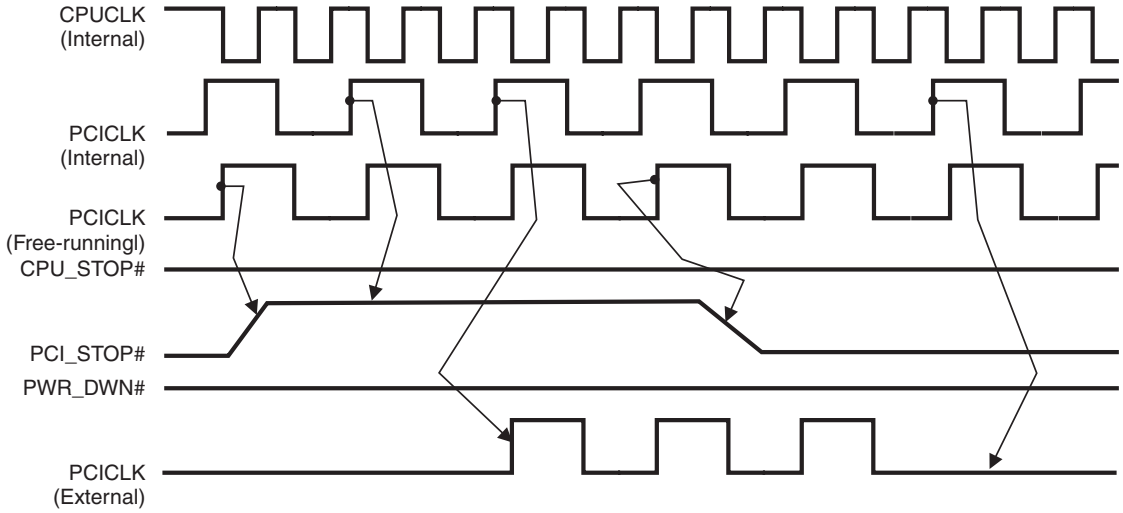
CPU_STOP# is an asychronous input to the clock synthesizer. It is used to turn off the CPUCLKs for low power operation. CPU_STOP# is synchronized by the **ICS951403**. All other clocks will continue to run while the CPUCLKs clocks are disabled. The CPUCLKs will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPUCLK on latency is less than 4 CPUCLKs and CPUCLK off latency is less than 4 CPUCLKs.



Notes:
1. All timing is referenced to the internal CPUCLK.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPUCLKs inside the **ICS951403**.
3. All other clocks continue to run undisturbed.
4. PD# and PCI_STOP# are shown in a high (true) state.

PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS951403**. It is used to turn off the PCICLK clocks for low power operation. PCI_STOP# is synchronized by the **ICS951403** internally. PCICLK clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



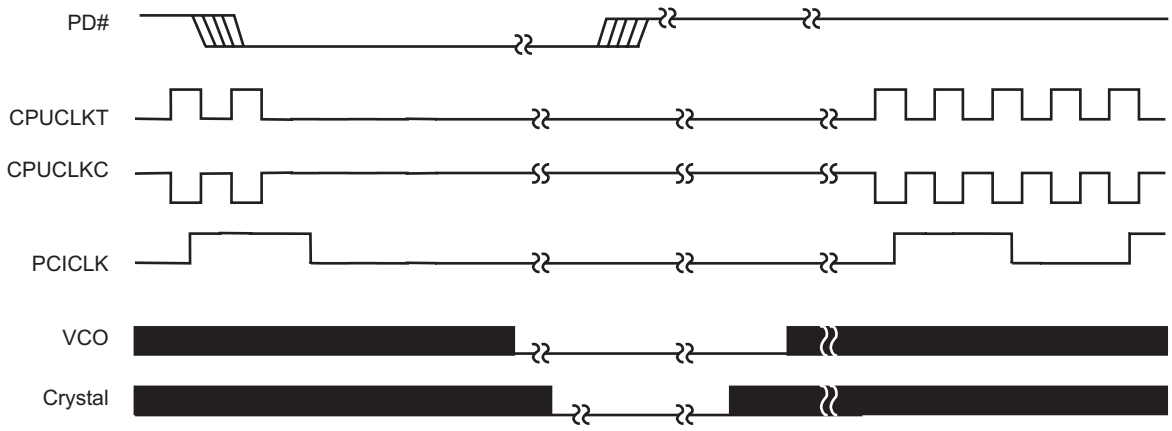
Notes:

1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS951403 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS951403.
3. All other clocks continue to run undisturbed.
4. PD# and CPU_STOP# are shown in a high (true) state.

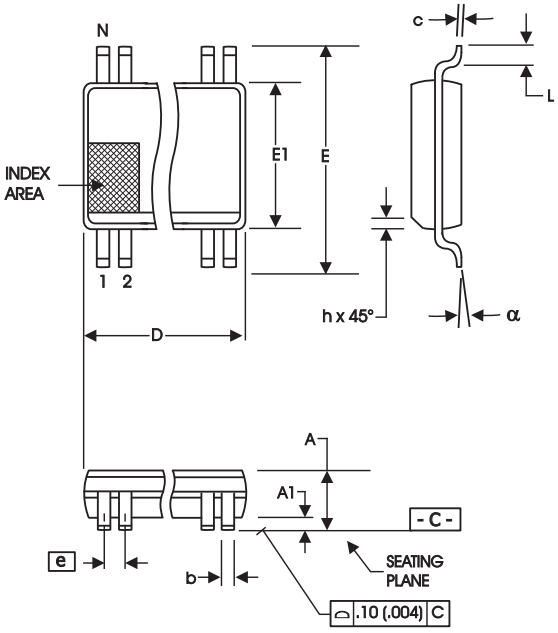
PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal needs to be synchronized internal to the device prior to powering down the clock synthesizer.

Internal clocks are not running after the device is put in power down. When PD# is active low all clocks need to be driven to a low value and held prior to turning off the VCOs and crystal. The power up latency needs to be less than 3 mS. The power down latency should be as short as possible but conforming to the sequence requirements shown below. PCI_STOP# and CPU_STOP# are considered to be don't cares during the power down operations. The REF and 48MHz clocks are expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.



Notes:
1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS951403 device).
2. As shown, the outputs Stop Low on the next falling edge after PD# goes low.
3. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside this part.
4. The shaded sections on the VCO and the Crystal signals indicate an active clock.
5. Diagrams shown with respect to 133MHz. Similar operation when CPU is 100MHz.



300 mil SSOP Package

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

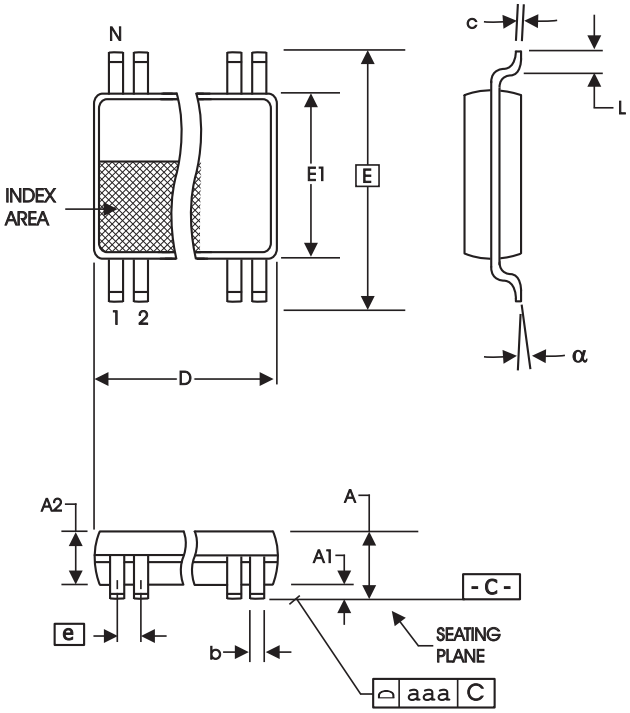
ICS951403yFLF-T

Example:

ICS XXXX y F LF- T

- **Designation for tape and reel packaging**
- **Lead Free (Optional)**
- **Package Type**
  F = SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

0486B—02/23/04



6.10 mm. Body, 0.50 mm. Pitch TSSOP
(240 mil) (20 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	12.40	12.60	.488	.496

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

ICS951403yGLF-T

Example:

ICS XXXX y G LF- T

- **Designation for tape and reel packaging**
- **Lead Free (Optional)**
- **Package Type**
  G = TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

0486B—02/23/04