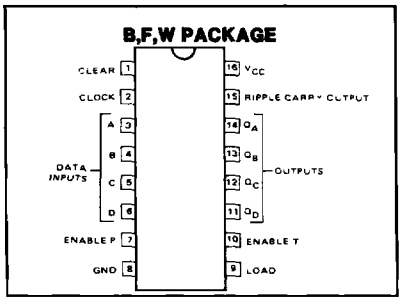
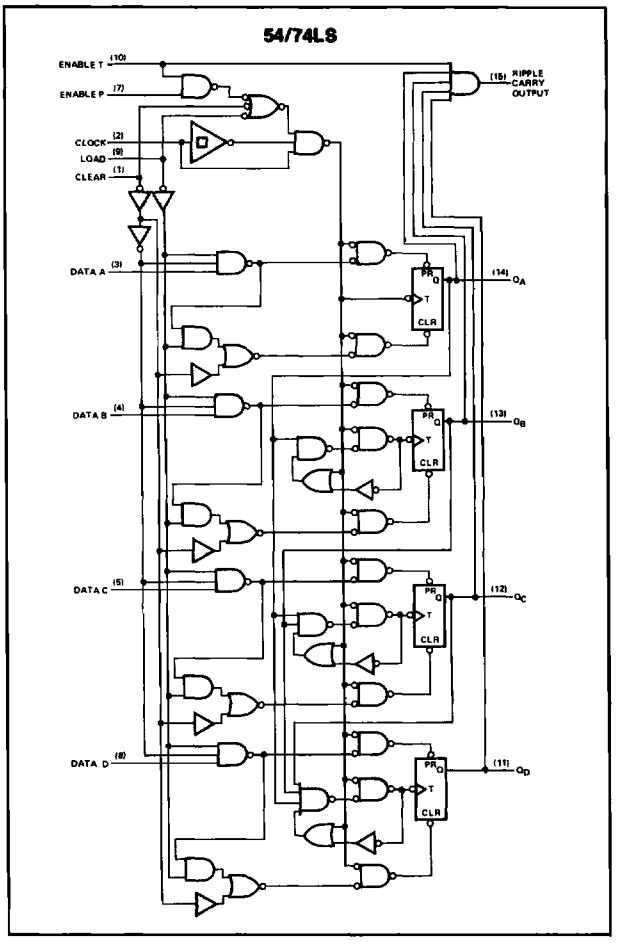
SPEED/PACKAGE AVAILABILITY

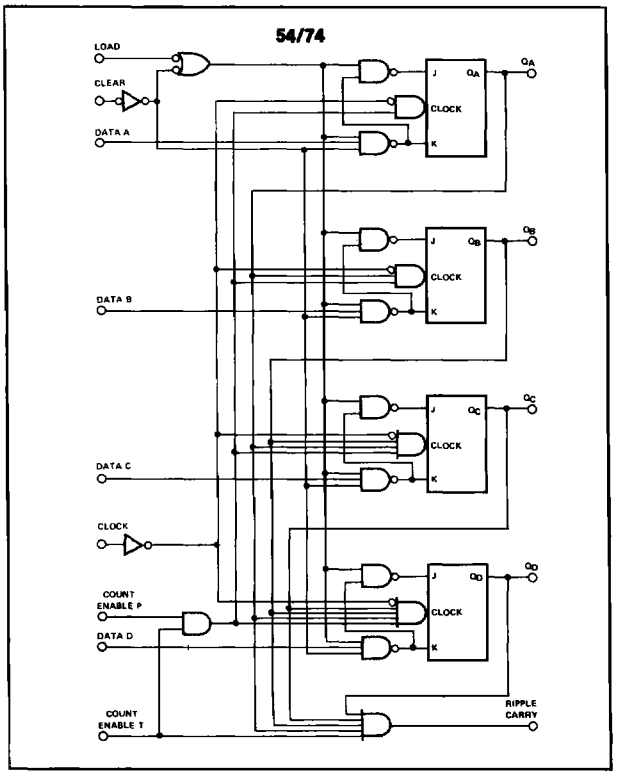
54	F,W	74	B,F
54LS	F,W	74LS	B,F

PIN CONFIGURATION





BLOCK DIAGRAM



DESCRIPTION

This synchronous presettable binary counter features an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveforms.

This counter is fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. The clear function for the 54/74LS163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the enable P or T inputs are allowed regardless of the level of the clock input.

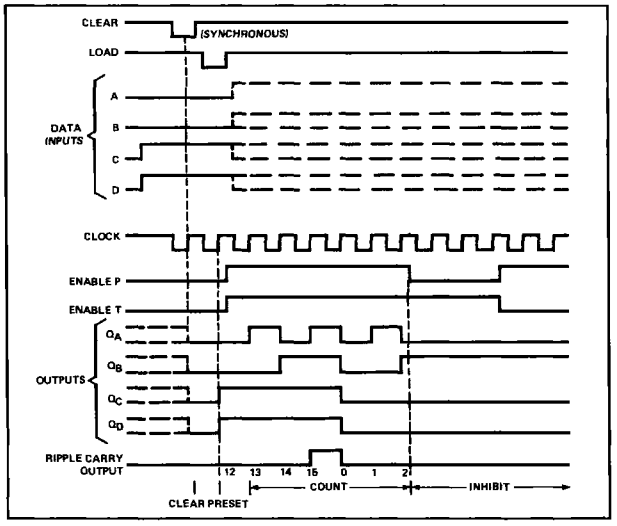
The 54/74LS163 features a fully independent clock circuit. Changes made to control inputs (enable P or T, load or clear) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

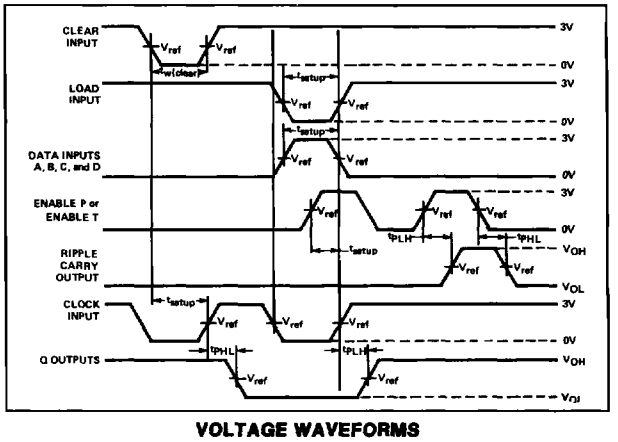
PARAMETER MEASUREMENT INFORMATION

TYPICAL CLEAR, PRESET, COUNT, AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Preset to binary twelve
3. Count to thirteen, fourteen, fifteen, zero, one, and two
4. Inhibit





VOLTAGE WAVEFORMS

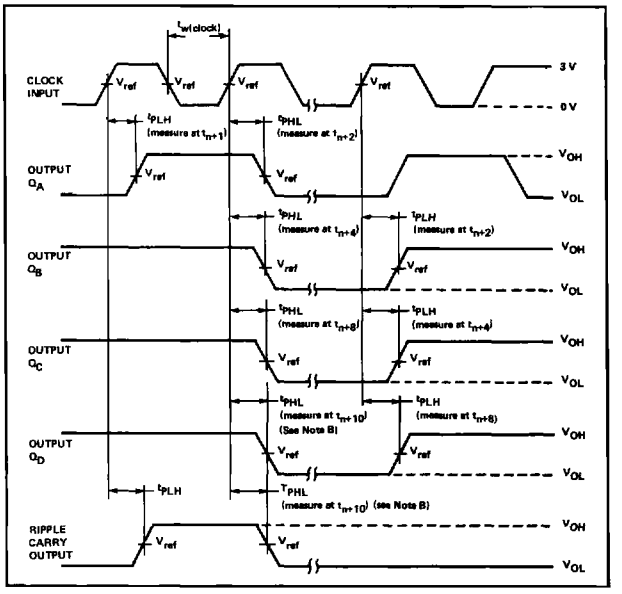
NOTES:

A. The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_{out} ≈ 50 Ω; '163, t_r ≤ 10 ns, t_f ≤ 10 ns; and for 'LS160 thru 'LS163, t_r ≤ 15 ns, t_f ≤ 6 ns.

B. Enable P and enable T setup times are measured at t_{n+0}.

C. V_{ref} = 1.3 V.

FIGURE 2—SWITCHING TIMES



VOLTAGE WAVEFORMS

NOTES:

A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_{out} ≈ 50 Ω; t_r ≤ 15 ns, t_f ≤ 6 ns. Vary PRR to measure f_{max}.

B. Outputs Q_D and carry are tested at t_n+16 where t_n is the bit time when all outputs are low.

C. V_{ref} = 1.3 V.

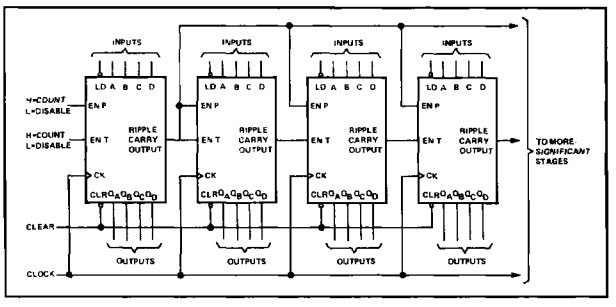
Load circuit is shown at the front of the book.

FIGURE 1—SWITCHING TIMES

TYPICAL APPLICATION DATA

N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 54/74LS163, will count in binary. Virtually any count mode (modulo-N, N_1-toN_2, N_1-to-maximum) can be used with this fast look-ahead circuit.



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2KΩ			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency			25	32		25	32		MHz
$t_{w(Clock)}$	Width of clock input pulse			25			25			ns
$t_{w(Clear)}$	Width of clear input pulse			20			20			
t_{Setup}	Input setup time	$D_A - D_D$		15						
		Enable P		20						
		Load		25						
		Clear		20						
		A,B,C,D	Q				0↑			
		Enable P	Q				20↑			
		Enable T					20↑			
		Load	Q				20↑			
		Clear	Q				20↑			
t_{Hold}	Input hold time	Any		0						
		A,B,C,D					25↑			
		Others					10↑			
Propagation delay time										
t_{PLH}	Low-to-high	Clock	Carry		23	35		23	35	ns
t_{PHL}	High-to-low				23	35		23	35	
t_{PLH}	Low-to-high	Clock	Q		13	20		16	24	
		(load input high)								
t_{PHL}	High-to-low				15	23		18	27	
t_{PLH}	Low-to-high	Clock	Q		17	25		17	25	
		(load input low)								
t_{PHL}	High-to-low				19	29		19	29	
t_{PLH}	Low-to-high	Enable T	Carry		10	14		15	23	
t_{PHL}	High-to-low				10	14		15	23	
t_{PHL}	High-to-low	Clear	Q		20	30		26	38	

Load circuit and typical waveforms are shown at the front of section.

8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER 54/74164

SPEED/PACKAGE AVAILABILITY

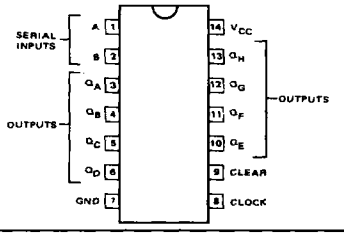
54 F,W 74 A
54LS F,W 74LS A

DESCRIPTION

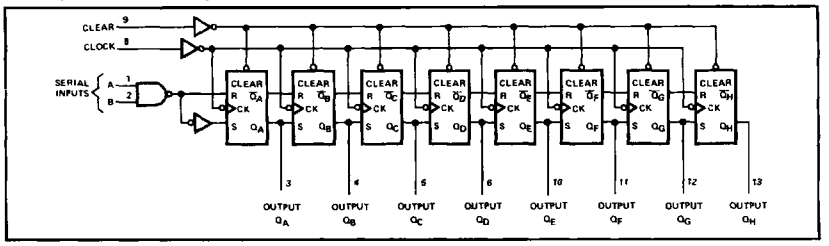
This 8-bit shift register features gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but the only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

PIN CONFIGURATION

A,F,W PACKAGE



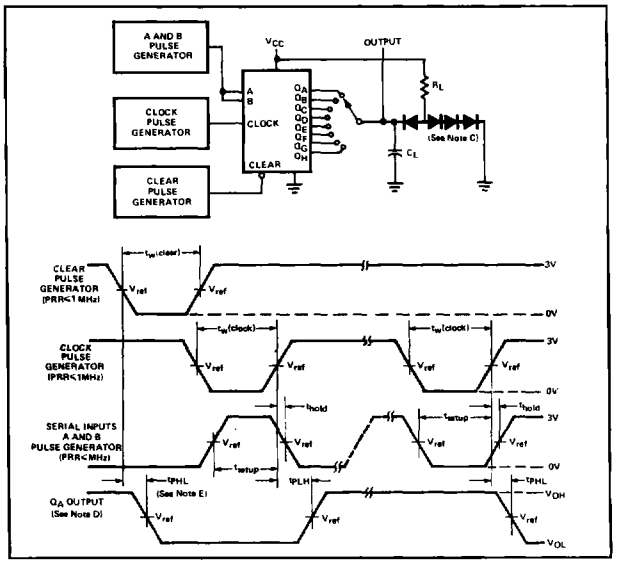
FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

54/74		
SERIAL INPUTS A AND B		
INPUTS ATt_n		OUTPUT ATt_{n+1}
A	B	Q_A
H	H	H
L	H	L
H	L	L
L	L	L

PARAMETER MEASUREMENT INFORMATION



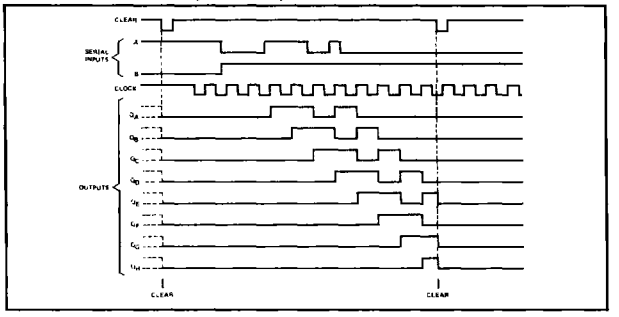
NOTES:

A. The pulse generators have the following characteristics: duty cycle ≤50%, $Z_{out} \approx 50\Omega$, $t_r \leq 15$ ns, $t_f \leq 6$ ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or 1N916.
D. Q_A output is illustrated. Relationship of serial input A and B data to other Q outputs is illustrated in the typical shift sequence.
E. Outputs are set to the high level prior to the measure of t_{PHL} from the clear input.
F. V_{ref} = 1.3V.

54/74LS						
INPUTS				OUTPUTS		
CLEAR	CLOCK	A	B	Q_A	Q_B	Q_H
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level.
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most-recent ↑ transition of the clock; indicates a one-bit shift.

TYPICAL CLEAR, SHIFT, AND CLEAR SEQUENCES



LOGIC

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L=15pF R_L=800Ω			54/74LS C_L=15pF R_L=2k			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Count} Count frequency			25	36		25	36		MHz
t_w Width of pulse			20			20			ns
t_{Setup} Input setup time			15			15↑			ns
t_{Hold} Input hold time			0			5↑			ns
Propagation delay time									
t_{PLH} Low-to-high	Clock		8	17	27		17	27	ns
			C_L=50pF						
			10	20	30				
t_{PHL} High-to-low			10	21	32		21	32	
			C_L=50pF						
			10	25	37				
t_{PHL} High-to-low	Clear			24	36		24	36	
			C_L=50pF						
				28	42				

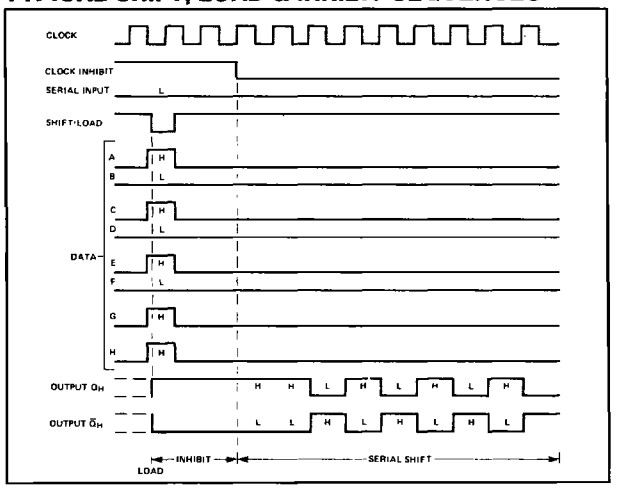
Load circuit and typical waveforms are shown at the front of section.

PARALLEL-LOAD 8-BIT SHIFT REGISTER 54/74165

SPEED/PACKAGE AVAILABILITY

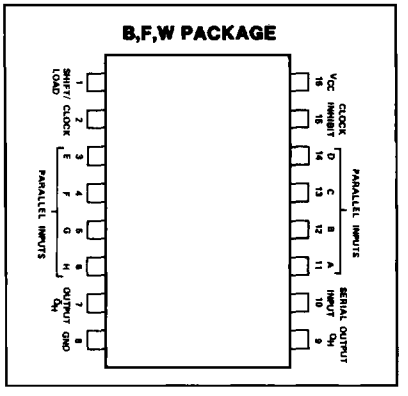
54 F,W 74 B

TYPICAL SHIFT, LOAD & INHIBIT SEQUENCES



PIN CONFIGURATION

B,F,W PACKAGE

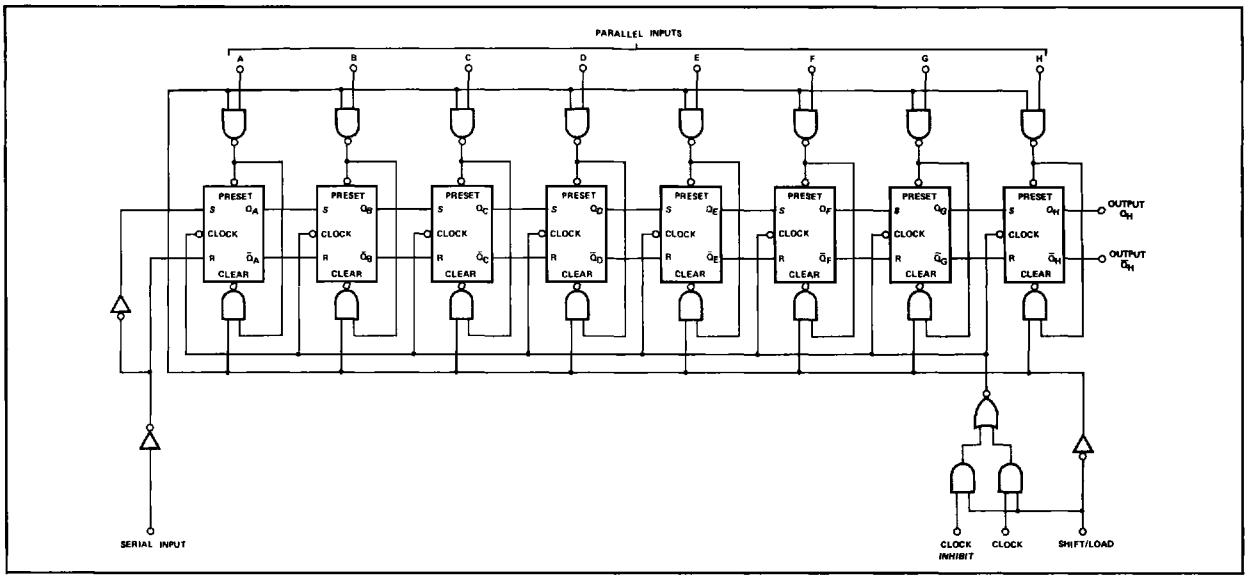


TRUTH TABLE

INPUTS					INTERNAL OUTPUTS		OUTPUT
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A...H	Q_A	Q_B	Q_H
L	X	X	X	a...h	a	b	h
H	L	L	X	X	Q_{AO}	Q_{BO}	Q_{HO}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	↑	X	X	Q_{AO}	Q_{BO}	Q_{HO}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a...h = the level of steady-state input at inputs A thru H, respectively.
Q_{AO}, Q_{BO}, Q_{HO} = the level of Q_A, A_B, or Q_H, respectively, before the indicated steady-state input conditions were established. Q_{An}, Q_{On} = the level of Q_A or Q_G, respectively, before the most recent ↑ transition of the clock.

LOGIC DIAGRAM

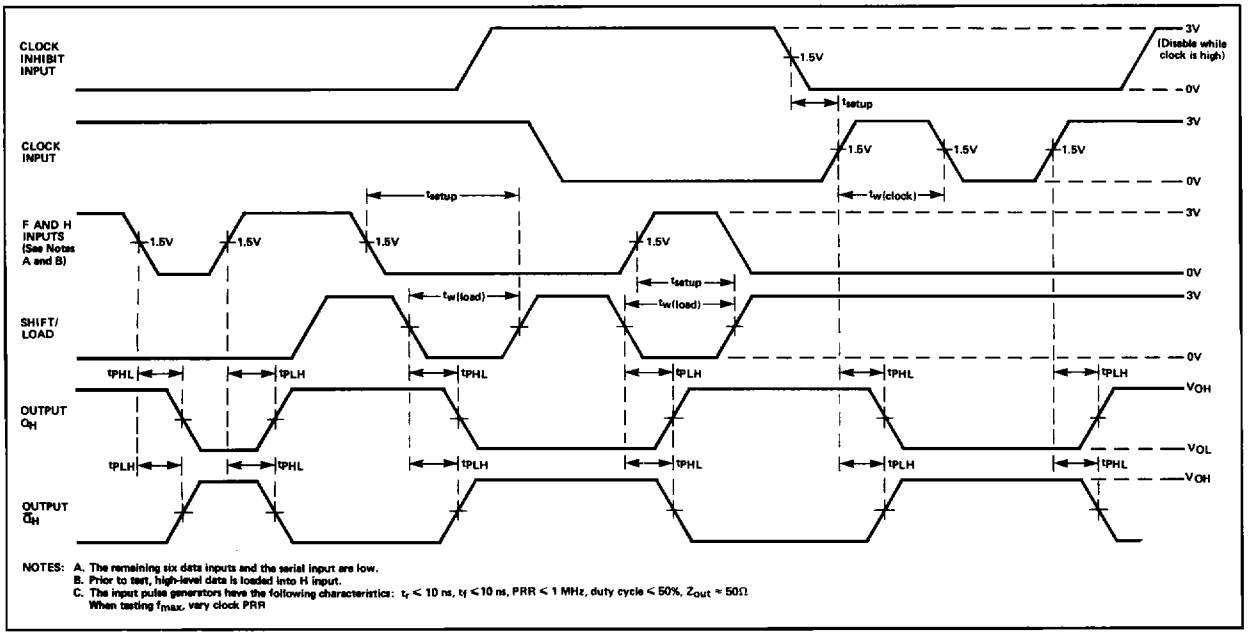


SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

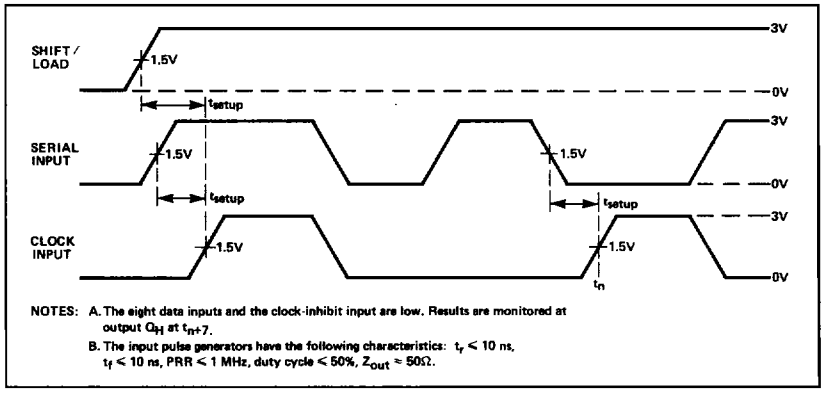
TEST CONDITIONS				54/74 C_L = 15pF R_L = 400Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
f_{max}				20	26		MHz
t_w	Width of pulse	Clock		25			ns
		Load		15			
t_{Setup}	Input setup time						ns
		Clock Enable		30			
		Parallel		10			
		Serial		20			
		Shift		45			
t_{Hold}	Input hold time			0			ns
Propagation delay time							
t_{PLH}	Low-to-high	Load	Any		21	31	ns
t_{PHL}	High-to-low				27	40	
t_{PLH}	Low-to-high	Clock	Any		16	27	
t_{PHL}	High-to-low				21	34	
t_{PLH}	Low-to-high	H	Q_H		11	20	
t_{PHL}	High-to-low				24	36	
t_{PLH}	Low-to-high	H	$\overline{Q}_H$		18	27	
t_{PHL}	High-to-low				18	27	

Load circuit and typical waveforms are shown at the front of section.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The remaining six data inputs and the serial input are low.
B. Prior to test, high-level data is loaded into H input.
C. The input pulse generators have the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR ≤ 1 MHz, duty cycle $\leq 50\%$, $Z_{out} \approx 50\Omega$
When testing f_{max}, vary clock PRR



NOTES: A. The eight data inputs and the clock-inhibit input are low. Results are monitored at output Q_H at t_{n+7}.
B. The input pulse generators have the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR ≤ 1 MHz, duty cycle $\leq 50\%$, $Z_{out} \approx 50\Omega$.