

54AC/74AC845 • 54ACT/74ACT845
54AC/74AC846 • 54ACT/74ACT846

8-Bit Transparent Latch

Description

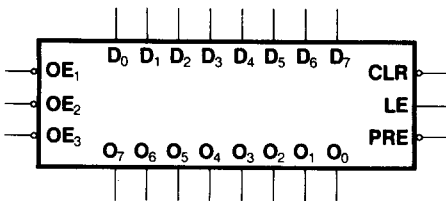
The 'AC'/ACT845 and 'AC'/ACT846 bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide easy expansion through multiple \overline{OE} controls.

The 'AC'/ACT845 is functionally and pin compatible with AMD's AM29845.

- 'ACT845 and 'ACT846 have TTL-Compatible inputs

Ordering Code: See Section 6

Logic Symbol ('AC'/ACT845)*

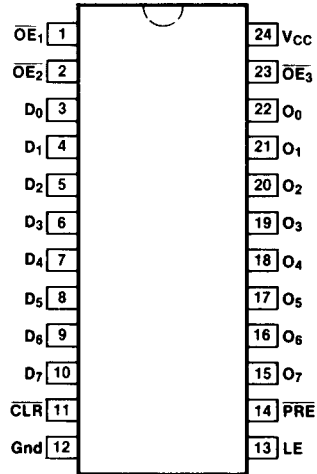


*The 'AC'/ACT846 has inverting outputs.

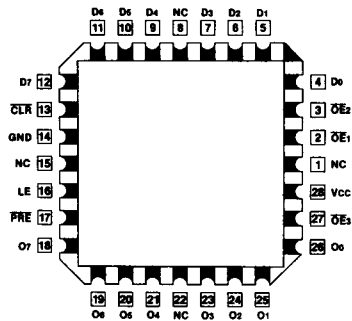
Pin Names

- D₀ - D₇ Data Inputs
- O₀ - O₇ Data Outputs ('AC'/ACT845)
- \overline{O}_0 - \overline{O}_7 Data Outputs ('AC'/ACT846)
- \overline{OE}_1 - \overline{OE}_3 Output Enables
- LE Latch Enable
- \overline{CLR} Clear
- PRE Preset

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

Functional Description

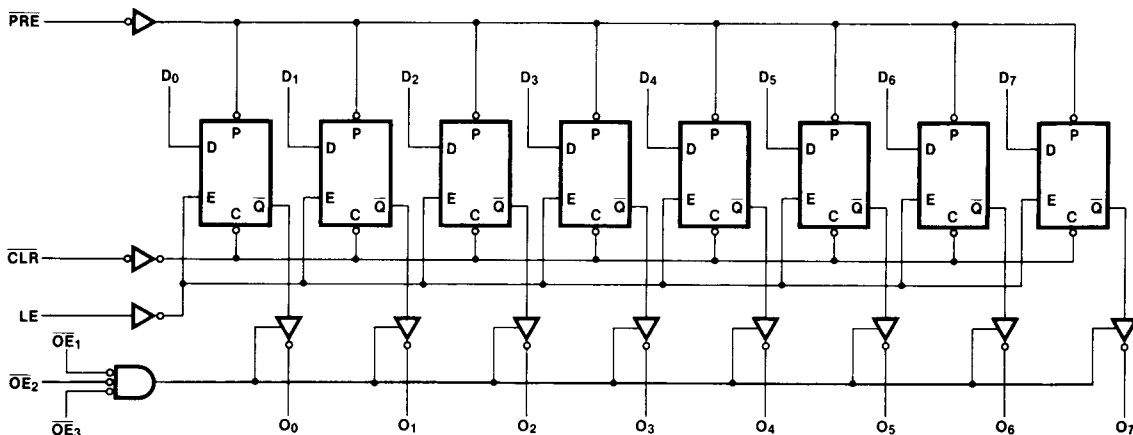
The 'AC/ACT845 and 'AC/ACT846 consist of eight D-type latches with 3-state outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation as the output transition follows the data in transition. On the LE HIGH-to-LOW transition, the data that meets the setup times is latched. Data appears on the bus when the Output Enables (\overline{OE}_1 , \overline{OE}_2 , \overline{OE}_3) are LOW. When any one of \overline{OE}_1 , \overline{OE}_2 or \overline{OE}_3 is HIGH, the bus output is in the high impedance state.

Function Table

Inputs					Internal	Outputs		Function
CLR	PRE	\overline{OE}_1 - \overline{OE}_3	LE	D	Q	O ('845)	\overline{O} ('846)	
H	H	H	H	L	L	Z	Z	High Z
H	H	H	H	H	H	Z	Z	High Z
H	H	H	L	X	NC	Z	Z	Latched
H	H	L	H	L	L	L	H	Transparent
H	H	L	H	H	H	H	L	Transparent
H	H	L	L	X	NC	NC	NC	Latched
H	L	L	X	X	H	H	L	Preset
L	H	L	X	X	L	L	H	Clear
L	L	L	X	X	H	H	L	Preset
L	H	H	L	X	L	Z	Z	Clear/High Z
H	L	H	L	X	H	Z	Z	Preset/High Z

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance
 NC = No Change

Logic Diagram ('AC/ACT845)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays. The 'AC/ACT846 has the same logic diagram with inverting outputs.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5 V$, $T_A = \text{Worst Case}$
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5 V$, $T_A = 25^\circ C$
I_{CCT}	Maximum Additional I_{CC} /Input ('ACT845/846)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1 V$, $V_{CC} = 5.5 V$, $T_A = \text{Worst Case}$

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC			54AC		74AC		Units	Fig. No.
			TA = + 25°C CL = 50 pF			TA = - 55°C to + 125°C CL = 50 pF		TA = - 40°C to + 85°C CL = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
tPLH	Propagation Delay Dn to On	3.3	17.0							ns	3-5
		5.0	12.0								
tPHL	Propagation Delay Dn to On	3.3	16.5							ns	3-5
		5.0	11.0								
tPLH	Propagation Delay LE to On	3.3	18.5							ns	3-6
		5.0	13.0								
tPHL	Propagation Delay LE to On	3.3	17.0							ns	3-6
		5.0	12.0								
tPLH	Propagation Delay PRE to On	3.3	17.0							ns	3-6
		5.0	12.0								
tPHL	Propagation Delay CLR to On	3.3	17.0							ns	3-6
		5.0	12.0								
tPZH	Output Enable Time OE to On	3.3	14.5							ns	3-7
		5.0	10.0								
tPZL	Output Enable Time OE to On	3.3	11.5							ns	3-8
		5.0	8.0								
tPHZ	Output Disable Time OE to On	3.3	13.0							ns	3-7
		5.0	9.0								
tPLZ	Output Disable Time OE to On	3.3	13.0							ns	3-8
		5.0	9.0								

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC	54AC	74AC	Units	Fig. No.
			TA = +25°C CL = 50 pF	TA = -55°C to +125°C CL = 50 pF	TA = -40°C to +85°C CL = 50 pF		
			Typ	Guaranteed Minimum			
ts	Setup Time, HIGH or LOW Dn to LE	3.3 5.0	4.0 2.5			ns	3-9
th	Hold Time, HIGH or LOW Dn to LE	3.3 5.0	4.0 0			ns	3-9
tw	LE Pulse Width, HIGH	3.3 5.0	4.0 2.5			ns	3-6
tw	PRE Pulse Width, LOW	3.3 5.0	4.0 2.5			ns	3-6
tw	CLR Pulse Width, LOW	3.3 5.0	4.0 2.5			ns	3-6
trec	PRE Recovery Time	3.3 5.0	5.0 4.0			ns	3-9
trec	CLR Recovery Time	3.3 5.0	5.0 4.0			ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	V _{CC} * (V)	74ACT			54ACT		74ACT		Units	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -55°C to +125°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
t _{PLH}	Propagation Delay D _n to O _n	5.0		12.0					ns	3-5	
t _{PHL}	Propagation Delay D _n to O _n	5.0		11.0					ns	3-5	
t _{PLH}	Propagation Delay LE to O _n	5.0		13.5					ns	3-6	
t _{PHL}	Propagation Delay LE to O _n	5.0		12.0					ns	3-6	
t _{PLH}	Propagation Delay PRE to O _n	5.0		12.0					ns	3-6	
t _{PHL}	Propagation Delay CLR to O _n	5.0		12.0					ns	3-6	
t _{PZH}	Output Enable Time OE to O _n	5.0		10.0					ns	3-7	
t _{PZL}	Output Enable Time OE to O _n	5.0		18.0					ns	3-8	
t _{PHZ}	Output Disable Time OE to O _n	5.0		9.0					ns	3-7	
t _{PLZ}	Output Disable Time OE to O _n	5.0		9.0					ns	3-8	

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT		54ACT		74ACT		Units	Fig. No.
			TA = +25°C CL = 50 pF		TA = -55°C to +125°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Typ	Guaranteed Minimum						
ts	Setup Time, HIGH or LOW Dn to LE	5.0	2.5						ns	3-9
th	Hold Time, HIGH or LOW Dn to LE	5.0	0						ns	3-9
tw	LE Pulse Width, HIGH	5.0	2.5						ns	3-6
tw	PRE Pulse Width, LOW	5.0	2.5						ns	3-6
tw	CLR Pulse Width, LOW	5.0	2.5						ns	3-6
trec	PRE Recovery Time	5.0	5.0						ns	3-9
trec	CLR Recovery Time	5.0	5.0						ns	3-9

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
CIN	Input Capacitance	4.5	pF	Vcc = 5.5 V
CPD	Power Dissipation Capacitance		pF	Vcc = 5.5 V