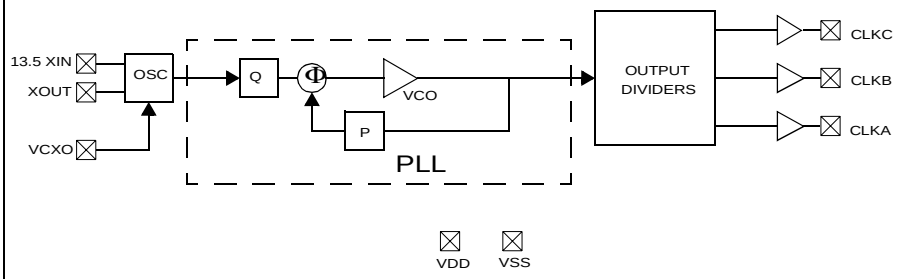
CY2412

MPEG Clock Generator with VCXO

Features	Benefits
• Integrated phase-locked loop (PLL)	Highest-performance PLL tailored for multimedia applications
• Low-jitter, high-accuracy outputs	Meets critical timing requirements in complex system designs
• VCXO with analog adjust	Large ±150-ppm range, better linearity
• 3.3V operation	Enables application compatibility

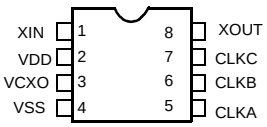
Part Number	Outputs	Input Frequency Range	Output Frequencies	VCXO Profile
CY2412	3	13.5-MHz pullable crystal input per Cypress specification	Two 27-MHz outputs, one 54-MHz output (3.3V)	Linear
CY2412-3	3	13.5-MHz pullable crystal input per Cypress specification	27 MHz, 13.5 MHz, 54 MHz (3.3V)	Linear

Logic Block Diagram



Pin Configuration

CY2412,-3
8-pin SOIC



Pin Summary

Pin Name	Pin Number	Pin Description
X_{IN}	1	Reference Crystal Input
V_{DD}	2	Voltage Supply
VCXO	3	Input Analog Control for VCXO
V_{SS}	4	Ground
CLKA	5	54-MHz clock output
CLKB	6	27-MHz clock output (-1)
CLKB	6	13.5-MHz clock output (-3)
CLKC	7	27-MHz clock output
X_{OUT}[1]	8	Reference Crystal Output

Pullable Crystal Specifications

Parameter	Description	Min.	Typ.	Max.	Unit
CR_{load}	Crystal Load Capacitance		14		pF
C0/C1				240	
ESR	Equivalent Series Resistance		35	50	Ω
T_o	Operating Temperature	0		70	°C
Crystal Accuracy	Crystal Accuracy			± 20	ppm
TT_s	Stability over Temperature and Aging			± 50	ppm

Absolute Maximum Conditions

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	–0.5	7.0	V
T_S	Storage Temperature[2]	–65	125	°C
T_J	Junction Temperature		125	°C
	Digital Inputs	V_{SS} – 0.3	V_{DD} + 0.3	V
	Digital Outputs referred to V_{DD}	V_{SS} – 0.3	V_{DD} + 0.3	V
	Electrostatic Discharge	2		kV

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage	3.14	3.3	3.47	V
T_A	Ambient Temperature	0		70	°C
C_{LOAD}	Max. Load Capacitance			15	pF
f_{REF}	Reference Frequency		13.5		MHz
t_{PU}	Power-up time for all VDD's to reach minimum specified voltage (power ramps must be monotonic)	0.05		500	ms

Notes:
1. Float X_{OUT} if X_{IN} is externally driven.
2. Rated for ten years.

DC Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{OH}	Output High Current	$V_{OH} = V_{DD} – 0.5$, $V_{DD} = 3.3V$	12	24		mA
I_{OL}	Output Low Current	$V_{OL} = 0.5$, $V_{DD} = 3.3V$	12	24		mA
C_{IN}	Input Capacitance				7	pF
I_{IZ}	Input Leakage Current			5		µA
$f_{\Delta XO}$	VCXO pullability range		±150			ppm
V_{VCXO}	VCXO input range		0		V_{DD}	V
f_{VBW}	VCXO input bandwidth			DC to 200		kHz
I_{DD}	Supply Current	Sum of Core and Output Current			35	mA

AC Electrical Characteristics

Parameter[3]	Description	Test Conditions	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	Duty Cycle is defined in *Figure 1*, 50% of V_{DD}	45	50	55	%
ER	Rising Edge Rate	Clock Edge Rate, Measured from 20% to 80% of $V_{DD,}$ C_{LOAD} = 15pF See figure 2.	0.8	1.4		V/ns
EF	Falling Edge Rate	Output Clock Edge Rate, Measured from 80% to 20% of $V_{DD,}$ C_{LOAD} = 15 pF See figure 2.	0.8	1.4		V/ns
t_9	Clock Jitter	Peak to Peak period jitter		100	200	ps
t_{10}	PLL Lock Time				3	ms

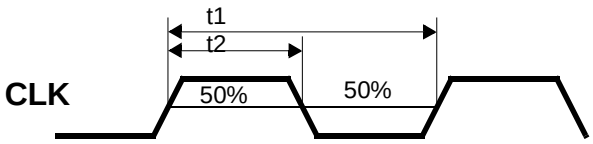


Figure 1. Duty Cycle Definition; DC = t2/t1

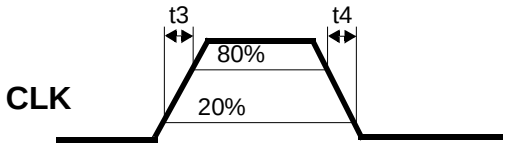
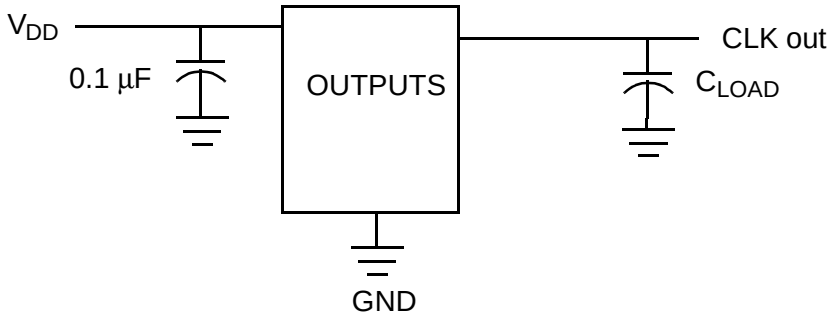


Figure 2. Rise and Fall Time Definitions: ER = 0.6 x VDD / t3 , EF = 0.6 x VDD / t4

Note:
3. Not 100% tested.

Test Circuit

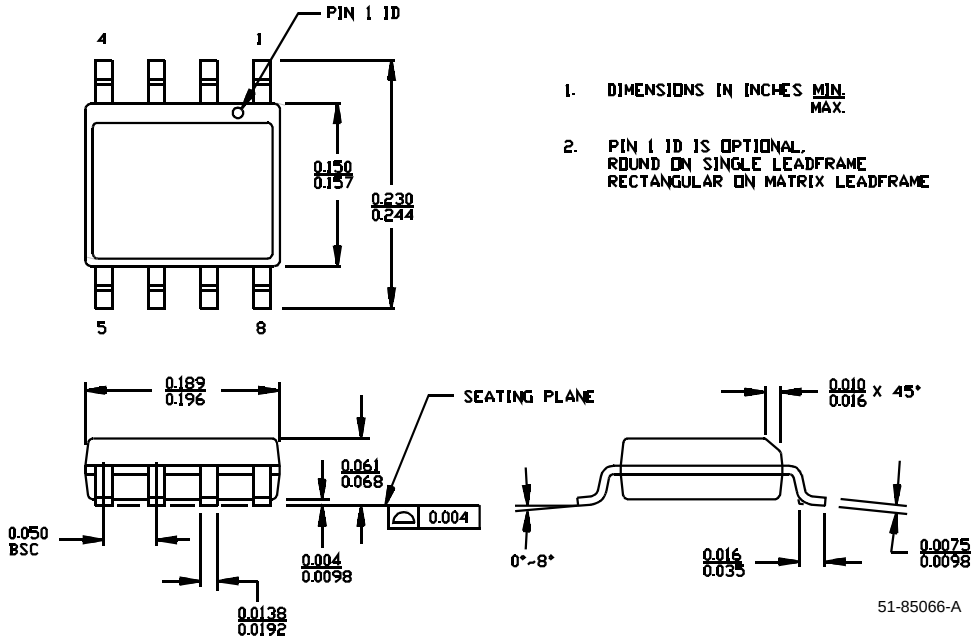


Ordering Information

Ordering Code	Package Name	Package Type	Operating Range	Operating Voltage
CY2412SC	S8	8-pin SOIC	Commercial	3.3V
CY2412SCT	S8	8-pin SOIC–Tape and Reel	Commercial	3.3V
CY2412SC-3	S8	8-pin SOIC	Commercial	3.3V
CY2412SC-3T	S8	8-pin SOIC–Tape and Reel	Commercial	3.3V

Package Diagram

8-lead (150-mil) SOIC S8



Document Title: CY2412 MPEG Clock Generator with VCXO Document Number: 38-07227				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110492	10/28/01	SZV	Change from Spec number: 38-00898 to 38-07227
*A	112457	03/14/02	CKN	Added CY2412-2 to data sheet
*B	116961	08/06/02	CKN	Removed CY2412-2 from the datasheet. Added CY2412-3 to data sheet.
*C	121879	12/12/02	RBI	Power up requirements added to Operating Conditions Information