T-46-23-14 ADVANCE

MICRON

MT5LC1008
128K x 8 SRAM

NEW 3.3 VOLT SRAM

SRAM

128K x 8 SRAM

LOW VOLTAGE WITH OUTPUT ENABLE

FEATURES

- High speed: 20, 25, 35 and 45ns
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3V power supply
- Easy memory expansion with $\overline{CE1}$, CE2 and $\overline{OE}$ options
- All inputs and outputs are TTL compatible
- Fast $\overline{OE}$ access time: 8ns

OPTIONS MARKING

- Timing

20ns access	-20
25ns access	-25
35ns access	-35
45ns access	-45

- Packages

Plastic DIP (400 mil)	None
Plastic DIP (600 mil)	W
Plastic SOJ (400 mil)	DJ

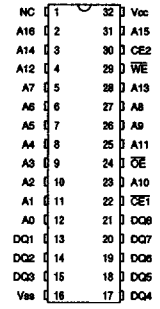
- 2V data retention — L
- 2V data retention, low power — LP
- Temperature

Industrial	(-40°C to +85°C)	IT
Automotive	(-40°C to +125°C)	AT
Extended	(-55°C to +125°C)	XT

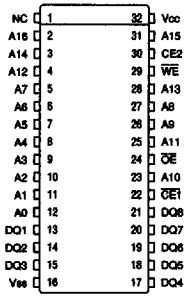
- Part Number Example: MT5LC1008DJ-35 LP IT

PIN ASSIGNMENT (Top View)

32-Pin DIP
(SA-7, SA-8)



32-Pin SOJ
(SD-5)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers dual chip enables ($\overline{CE1}$, CE2). This enhancement can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE1}$ inputs are both LOW and CE2 is HIGH. Reading is accomplished when $\overline{WE}$ and CE2 remain HIGH and $\overline{CE1}$ goes LOW. The device offers reduced power standby modes when disabled. These modes allow system designers to meet low standby power requirements.

The "LP" version provides a reduction in both CMOS standby current (I_{SB2}) and TTL standby current (I_{SB1}) over the standard part. This is achieved through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines. The gated inputs also facilitate the design of battery-backed systems where the designer needs to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +3.3V power supply and all inputs and outputs are fully TTL compatible.

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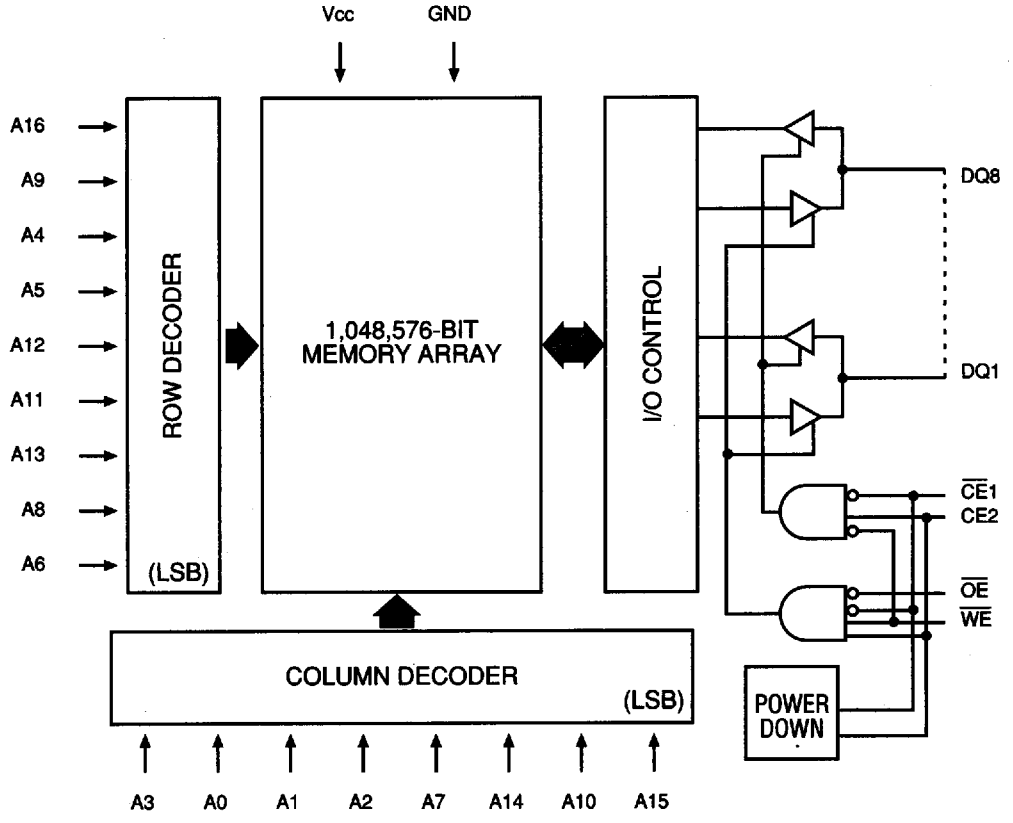
T-46-23-14

FUNCTIONAL BLOCK DIAGRAM



NOTE: The two least significant row address bits (A8 and A6) are encoded using a Gray code.

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE1}$	CE2	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	X	HIGH-Z	STANDBY
STANDBY	X	X	L	X	HIGH-Z	STANDBY
READ	L	L	H	H	Q	ACTIVE
READ	H	L	H	H	HIGH-Z	ACTIVE
WRITE	X	L	H	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .....-0.5V to +4.6V
VIN.....-0.5V to Vcc + 0.5V (+4.6V MAX)
Storage Temperature (Plastic) .....-55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		VIH	2.0	Vcc+0.3	V	1
Input Low (Logic 0) Voltage		VIL	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ VIN ≤ Vcc	ILI	-1	1	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ VOUT ≤ Vcc	ILO	-1	1	µA	
Output High Voltage	IOH = -2.0mA	VOH	2.4		V	1
	IOH = -100µA	VOH	Vcc-0.2		V	1
Output Low Voltage	IOL = 2.0mA	VOL		0.4	V	1
	IOL = 100µA	VOL		0.2	V	1
Supply Voltage		Vcc	3.0	3.6	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	VER	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE1}$ ≤ VIL AND CE2 ≥ VIH; Vcc = MAX; Outputs Open f = MAX = 1/tRC	ICC	ALL	65	55	45	40	mA	3, 15, 16
Power Supply Current: Standby	$\overline{CE1}$ ≥ VIH OR CE2 ≤ VIL; Vcc = MAX; Outputs Open f = MAX = 1/tRC	ISB1	STD	14	12	8	6	mA	15, 16, 17
			LP	500	500	500	500	µA	15, 16, 17
	$\overline{CE1}$ ≥ Vcc - 0.2V or CE2 ≤ Vss + 0.2V Vcc = MAX VIN ≥ Vcc - 0.2V or VIN ≤ Vss + 0.2V	ISB2	STD	300	300	300	300	µA	15, 16, 18
			LP	100	100	100	100	µA	15, 16, 18

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	CI	8	pF	4
Output Capacitance	Vcc = 3.3V	CO	8	pF	4

T-46-23-14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 14) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

DESCRIPTION		-20		-25		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^tRC	20		25		35		45		ns	
Address access time	^tAA		20		25		35		45	ns	
Chip Enable access time	^tACE		20		25		35		45	ns	
Output hold from address change	^tOH	3		5		5		5		ns	
Chip Enable to output in Low-Z	^tLZCE	3		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		8		10		15		18	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	
Chip disable to power-down time	^tPD	20			25		35		45	ns	
Output Enable access time	^tAOE		4		8		12		15	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		4		10		12		15	ns	6
WRITE Cycle											
WRITE cycle time	^tWC	20		25		35		45		ns	
Chip Enable to end of write	^tCW	12		15		20		25		ns	
Address valid to end of write	^tAW	12		15		20		25		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	$^tWP1$	12		15		20		25		ns	
WRITE pulse width	$^tWP2$	15		15		20		25		ns	
Data setup time	^tDS	8		10		15		20		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	3		5		5		5		ns	7
Write Enable to output in High-Z	^tHZWE		8		10		15		18	ns	6, 7

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T-46-23-14

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AC TEST CONDITIONS

Input pulse levels	Vss to 2.8V
Input rise and fall times	3ns
Input timing reference levels	1.4V
Output reference levels	1.4V
Output load	See Figures 1 and 2

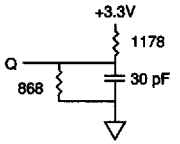


Fig. 1 OUTPUT LOAD EQUIVALENT

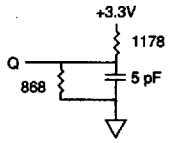


Fig. 2 OUTPUT LOAD EQUIVALENT

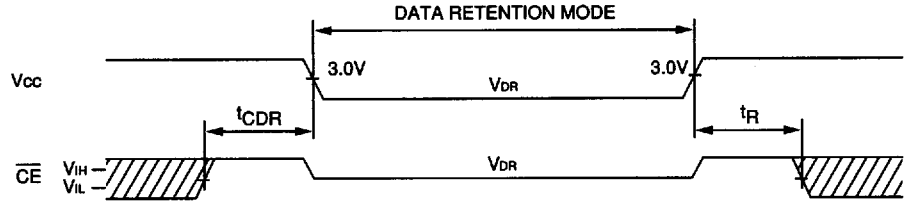
NOTES

1. All voltages referenced to Vss (GND).
2. -1V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables and output enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. CE2 timing is the same as $\overline{CE1}$ timing. The wave form is inverted.
13. Chip enable and write enable can initiate and terminate a WRITE cycle.
14. Refer to the IT/XT/AT section of Micron's *SRAM Data Book* for applicable non-commercial temperature range specifications.
15. Typical values are measured at 3.3V, 25°C and 25ns cycle time.
16. Vcc = MAX.
17. One chip enable must be inactive; the other may be ≥ V_{IH} or ≤ V_{IL}.
18. One chip enable must be inactive; the other may be ≤ Vss +0.2or ≥ Vcc -0.2.

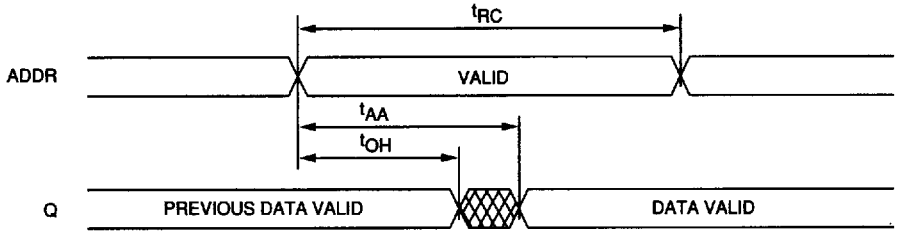
DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP Versions Only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data		V_{DR}	2			V	
Data Retention Current	$\overline{CE1}$ ≥ Vcc -0.2V or CE2 ≤ Vss +0.2V Other Inputs: V_{IN} ≥ Vcc -0.2V or V_{IN} ≤ Vss +0.2V Vcc = 2V	I_{CCDR}		TBD	50	µA	18
Chip Deselect to Data Retention Time		^{t}CDR	0			ns	4
Operation Recovery Time		^{t}R	^{t}RC			ns	4, 11

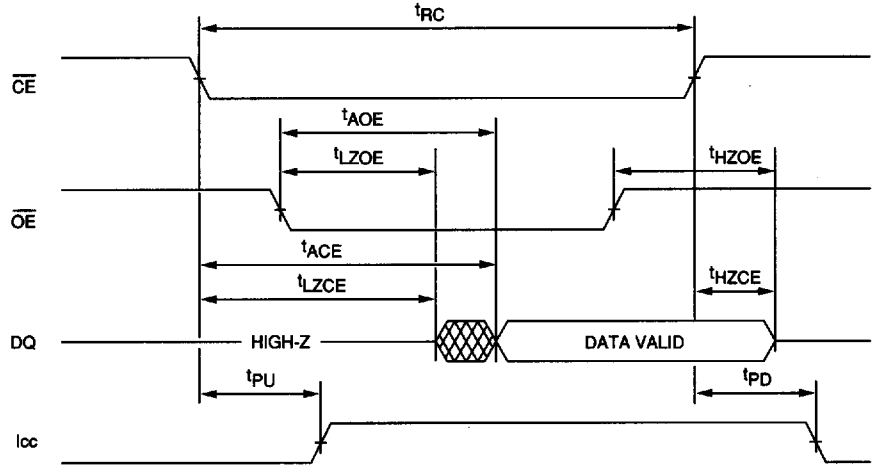
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [8, 9]



READ CYCLE NO. 2 [7, 8, 10, 12]

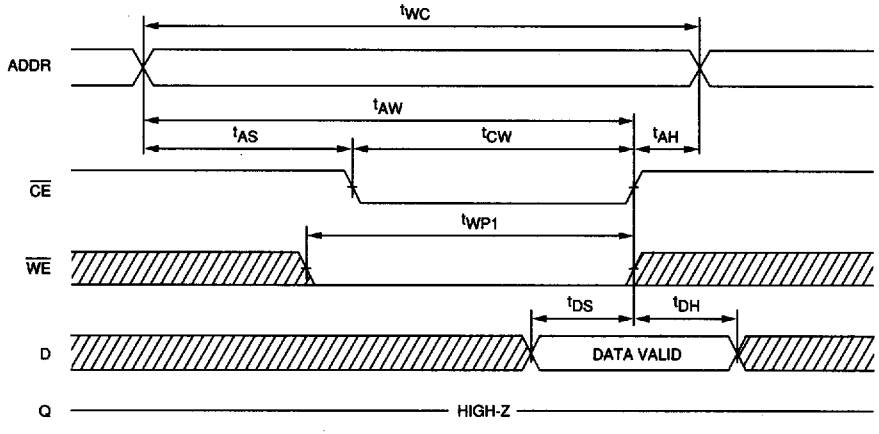


DON'T CARE

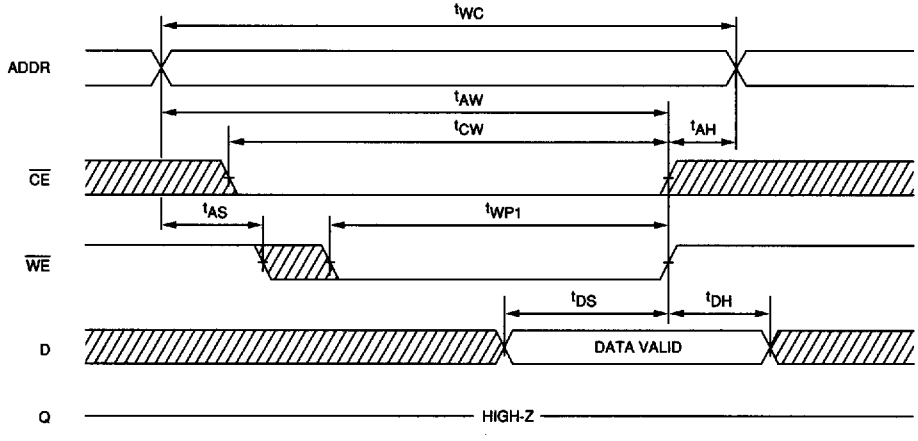
UNDEFINED

T-46-23-14

WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [12, 13]
(Write Enable Controlled)



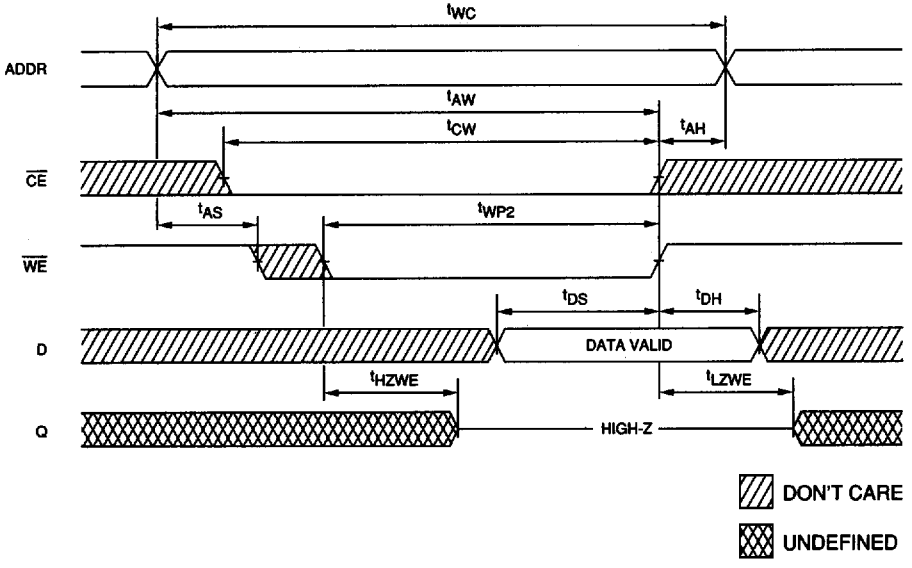
DON'T CARE

UNDEFINED

NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

T-46-23-14

WRITE CYCLE NO. 3 [7, 12, 13]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).