

**512K x 32 SRAM**  
**SRAM MEMORY ARRAY**

**AVAILABLE AS MILITARY SPECIFICATIONS**

- SMD 5962-94611 & 5962-95624 (Military Pinout)
- MIL-STD-883

**FEATURES**

- Operation with single 5V supply
- Vastly improved Icc Specs
- High speed: 12, 15, 17, 20, 25, 35, 45 & 55ns
- Low power CMOS
- Built in decoupling caps for low noise
- Organized as 512Kx32, byte selectable
- TTL Compatible Inputs and Outputs

**GENERAL DESCRIPTION**

The AS8S512K32 and AS8S512K32A are 16 Megabit CMOS SRAM Modules organized as 512Kx32 bits. These devices achieve high speed access, low power consumption and high reliability by employing advanced CMOS memory technology.

This military temperature grade product is ideally suited for military applications.

**OPTIONS**

<b>Operating Temp. Ranges</b>	<b>Markings</b>
Full Military (-55°C to +125°C)	Q & 883
Military (-55°C to +125°C)	XT
Industrial (-40°C to +85°C)	IT

<b>Timing</b>	<b>Markings</b>	<b>Timing</b>	<b>Markings</b>
12ns	-12	25ns	-25
15ns	-15	35ns	-35
17ns	-17	45ns	-45
20ns	-20	55ns	-55

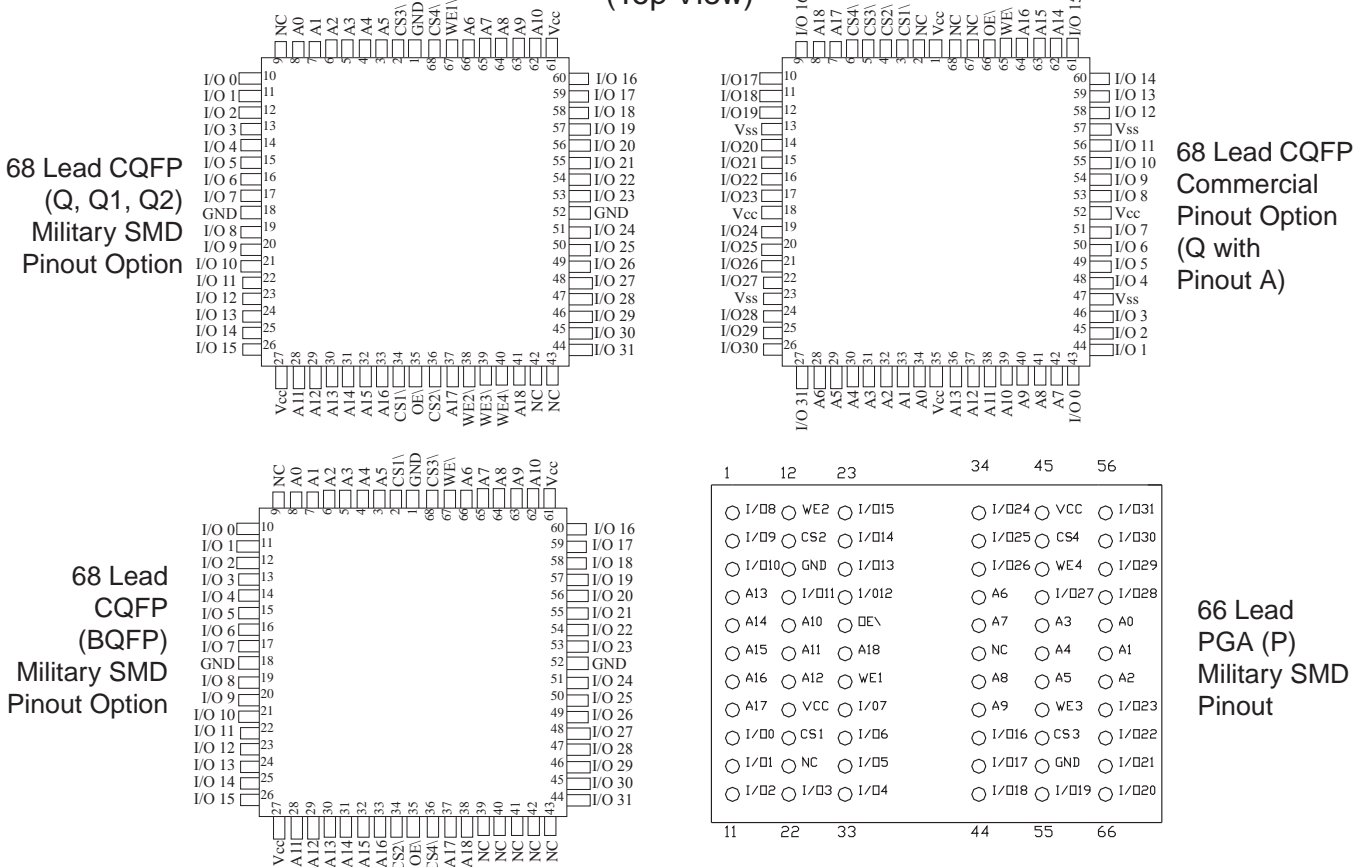
<b>Package</b>	<b>Markings</b>
Ceramic Quad Flatpack	Q, Q1, Q2, BQFP
Pin Grid Array	P

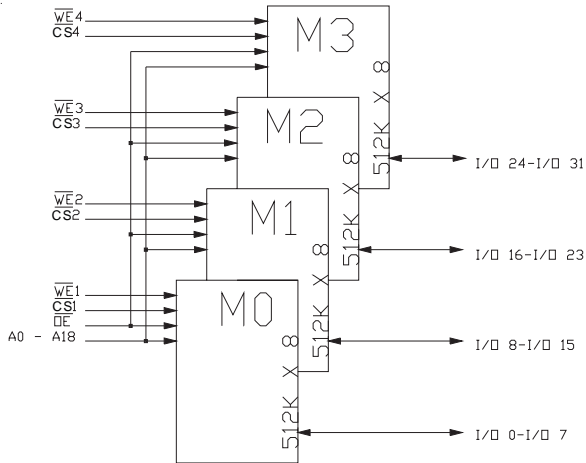
<b>Low Power Data Retention Mode</b>	L
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<b>Pinout</b>	<b>Markings</b>
Military	(no indicator)
Commercial	A*

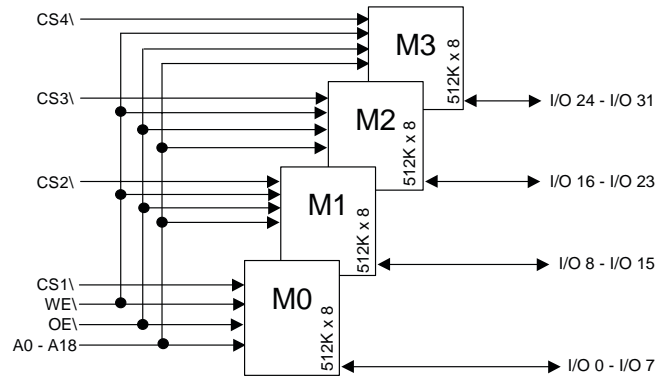
*\*(available with Q package only)*

**PIN ASSIGNMENT**  
(Top View)





MILITARY PINOUT/BLOCK DIAGRAM



COMMERCIAL PINOUT/BLOCK DIAGRAM

**TRUTH TABLE**

MODE	OE\	CS\	WE\	I/O	POWER
Read	L	L	H	D <sub>OUT</sub>	ACTIVE
Write	X	L	L	D <sub>IN</sub>	ACTIVE
Standby	X	H	X	High Z	STANDBY

### ABSOLUTE MAXIMUM RATINGS\*

Voltage of V<sub>CC</sub> Supply Relative to V<sub>SS</sub>.....-5V to +7V  
Storage Temperature.....-65°C to +150°C  
Short Circuit Output Current(per I/O).....20mA  
Voltage on Any Pin Relative to V<sub>SS</sub>.....-5V to V<sub>CC</sub>+1V  
Maximum Junction Temperature\*\*.....+150°C

\*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.

This is a stress rating only and functional operation on the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

\*\*Junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See the Application Information section at the end of this datasheet for more information.

### ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-55°C ≤ T<sub>A</sub> ≤ 125°C and -40°C to +85°C; V<sub>CC</sub> = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (logic 1) Voltage		V <sub>IH</sub>	2.2	V <sub>CC</sub> +0.5	V	1
Input Low (logic 0) Voltage		V <sub>IL</sub>	-0.5	0.8	V	1,2
Input Leakage Current <sub>ADD,OE</sub>	0V < V <sub>IN</sub> < V <sub>CC</sub>	I <sub>LI1</sub>	-10	10	μA	
Input Leakage Current <sub>WE, CE</sub>		I <sub>LI2</sub>	-10	10	μA	
Output Leakage Current <sub>I/O</sub>	Output(s) Disabled 0V < V <sub>OUT</sub> < V <sub>CC</sub>	I <sub>LO</sub>	-10	10	μA	
Output High Voltage	I <sub>OH</sub> = -4.0mA	V <sub>OH</sub>	2.4		V	1
Output Low Voltage	I <sub>OL</sub> = 8.0mA	V <sub>OL</sub>		0.4	V	1
Supply Voltage		V <sub>CC</sub>	4.5	5.5	V	1

DESCRIPTION	CONDITIONS	SYMBOL	MAX								UNITS	NOTES
			-12	-15	-17	-20	-25	-35	-45	-55		
Power Supply Current: Operating	CS < V <sub>IL</sub> ; V <sub>CC</sub> = MAX f = MAX = 1/ t <sub>RC</sub> (MIN) Outputs Open	I <sub>CC</sub>	250	200	175	150	140	130	120	110	mA	3,13
Power Supply Current: Standby	CS > V <sub>IH</sub> ; V <sub>CC</sub> = MAX f = MAX = 1/ t <sub>RC</sub> (MIN) Outputs Open	I <sub>SBT1</sub>	40	40	40	35	35	30	30	30	mA	3, 13
CMOS Standby	V <sub>IN</sub> = V <sub>CC</sub> - 0.2V, or V <sub>SS</sub> + 0.2V V <sub>CC</sub> =Max; f = 0Hz	I <sub>SBT2</sub>	20	20	20	20	20	20	20	20	mA	

**CAPACITANCE** ( $V_{IN} = 0V, f = 1MHz, T_A = 25^{\circ}C$ )<sup>1</sup>

SYMBOL	PARAMETER	MAX	UNITS
$C_{ADD}$	A0 - A18 Capacitance	50	pF
$C_{OE}$	OE\ Capacitance	50	pF
$C_{WE}, C_{CS}$	WE\ and CS\ Capacitance	20	pF
$C_{IO}$	I/O 0- I/O 31 Capacitance	20	pF
$C_{WE}$ ("A" version)	WE\ Capacitance	50	pF

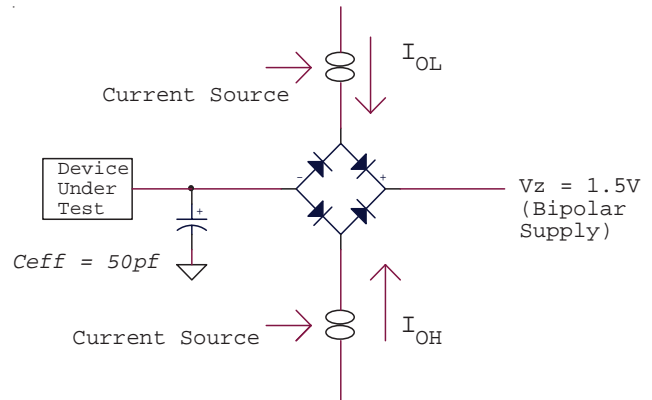
**NOTE:**

1. This parameter is sampled.

**AC TEST CONDITIONS**

**Test Specifications**

Input pulse levels.....VSS to 3V  
 Input rise and fall times.....5ns  
 Input timing reference levels.....1.5V  
 Output reference levels.....1.5V  
 Output load.....See Figure 1



**Figure 1**

**NOTES:**

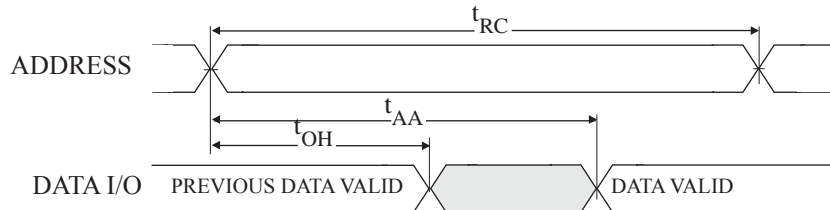
- $V_z$  is programmable from -2V to +7V.
- $I_{OL}$  and  $I_{OH}$  programmable from 0 to 16 mA.
- $V_z$  is typically the midpoint of  $V_{OH}$  and  $V_{OL}$ .
- $I_{OL}$  and  $I_{OH}$  are adjusted to simulate a typical resistive load circuit.

**Figure 1**

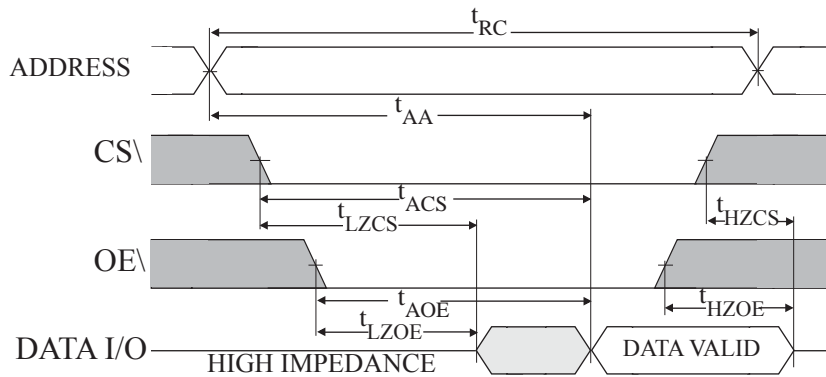
**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**  
(NOTE 5) (-55°C ≤ T<sub>A</sub> ≤ 125°C and -40°C to +85°C; V<sub>CC</sub> = 5V ±10%)

DESCRIPTION	SYMBOL	-12		-15		-17		-20		-25		-35		-45		-55		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
<b>READ CYCLE</b>																			
READ cycle time	<sup>t</sup> RC	12		15		17		20		25		35		45		55		ns	
Address access time	<sup>t</sup> AA		12		15		17		20		25		35		45		55		ns
Chip select access time	<sup>t</sup> ACS		12		15		17		20		25		35		45		55		ns
Output hold from address change	<sup>t</sup> OH	2		2		2		2		2		2		2		2		ns	
Chip select to output in Low-Z	<sup>t</sup> LZCS	2		2		2		2		2		2		2		2		ns	4,6,7
Chip select to output in High-Z	<sup>t</sup> HZCS		7		8		9		10		12		15		20		20		ns
Output enable access time	<sup>t</sup> AOE		7		8		9		10		12		15		20		20		ns
Output enable to output in Low-Z	<sup>t</sup> LZOE	0		0		0		0		0		0		0		0		ns	4,6
Output disable to output in High-Z	<sup>t</sup> HZOE		7		9		12		12		12		15		20		20		ns
<b>WRITE CYCLE</b>																			
WRITE cycle time	<sup>t</sup> WC	12		15		17		20		25		35		45		55		ns	
Chip select to end of write	<sup>t</sup> CW	10		12		15		15		17		20		25		25		ns	
Address valid to end of write	<sup>t</sup> AW	10		12		15		15		17		20		25		25		ns	
Address setup time	<sup>t</sup> AS	2		2		2		2		2		2		2		2		ns	
Address hold from end of write	<sup>t</sup> AH	1		1		1		1		1		1		1		1		ns	
WRITE pulse width	<sup>t</sup> WP1	10		12		15		15		17		20		25		25		ns	
WRITE pulse width	<sup>t</sup> WP2	10		12		15		15		17		20		25		25		ns	
Data setup time	<sup>t</sup> DS	8		10		12		10		12		15		20		20		ns	
Data hold time	<sup>t</sup> DH	0		0		0		0		0		0		0		0		ns	
Write disable to output in Low-z	<sup>t</sup> LZWE	2		2		2		2		2		2		2		2		ns	4,6,7
Write enable to output in High-Z	<sup>t</sup> HZWE	7		8			9		11		13		15		15		15		ns

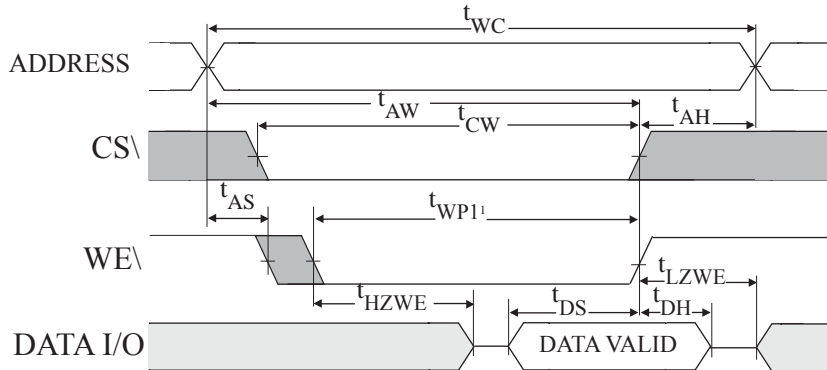
### READ CYCLE NO. 1



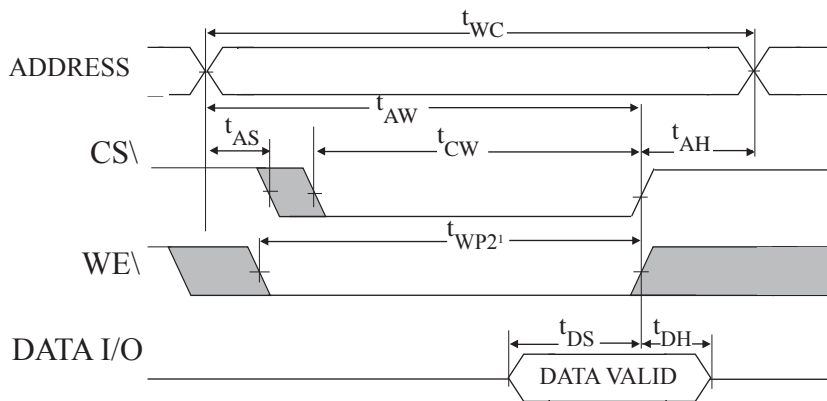
### READ CYCLE NO. 2



**WRITE CYCLE NO. 1**  
 (Chip Select Controlled)



**WRITE CYCLE NO. 2**  
 (Write Enable Controlled)



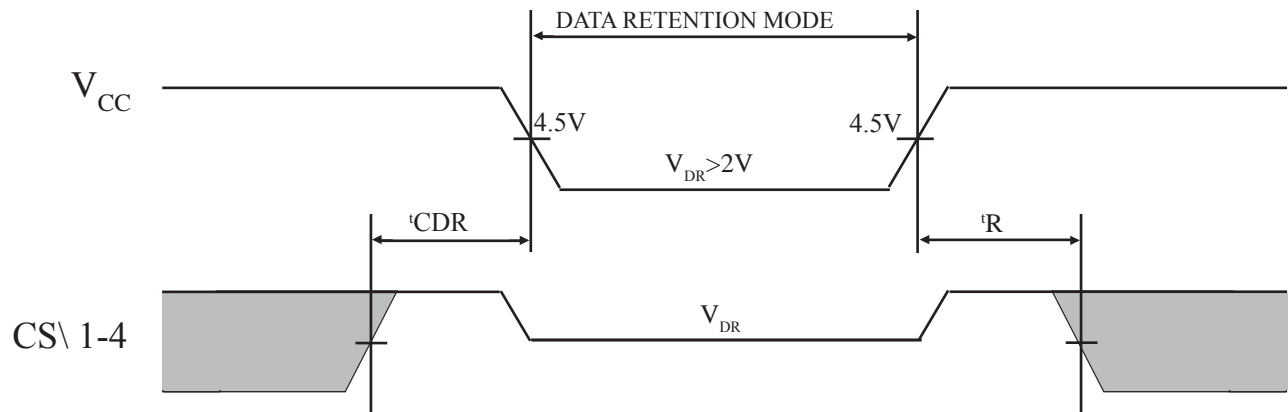
### NOTES

- All voltages referenced to  $V_{SS}$  (GND).
- 2V for pulse width <20ns.
- ICC is dependent on output loading and cycle rates.  
The specified value applies with the outputs unloaded, and  $f = \frac{1}{t_{RC(MIN)}} \text{ Hz}$ .
- This parameter guaranteed but not tested.
- Test conditions as specified with output loading as shown in Fig. 1 unless otherwise noted.
- $t_{HZCS}$ ,  $t_{HZOE}$  and  $t_{HZWE}$  are specified with  $C_L = 5\text{pF}$  as in Fig. 2. Transition is measured +/- 200 mV typical from steady state voltage, allowing for actual tester RC time constant.
- At any given temperature and voltage condition,  $t_{HZCS}$ , is less than  $t_{LZCS}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$ .
- WE\ is HIGH for READ cycle.
- Device is continuously selected. Chip selects and output enable are held in their active state.
- Address valid prior to or coincident with latest occurring chip enable.
- $t_{RC}$  = READ cycle time.
- Chip enable (CS\ ) and write enable (WE\ ) can initiate and terminate a WRITE cycle.
- $I_{CC}$  is for 32 bit mode.

### LOW POWER CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
$V_{CC}$ for Retention Data		$V_{DR}$	2		V	
Data Retention Current	All Inputs @ $V_{CC} \pm 0.2\text{V}$ or $V_{SS} \pm 0.2\text{V}$ , $CS\ = V_{CC} \pm 0.2\text{V}$	$V_{CC} = 2\text{V}$		10	mA	
		$V_{CC} = 3\text{V}$		12	mA	
Chip Deselect to Data Retention Time		$t_{CDR}$	0		ns	4
Operation Recovery Time		$t_R$	$t_{RC}$		ns	4, 11

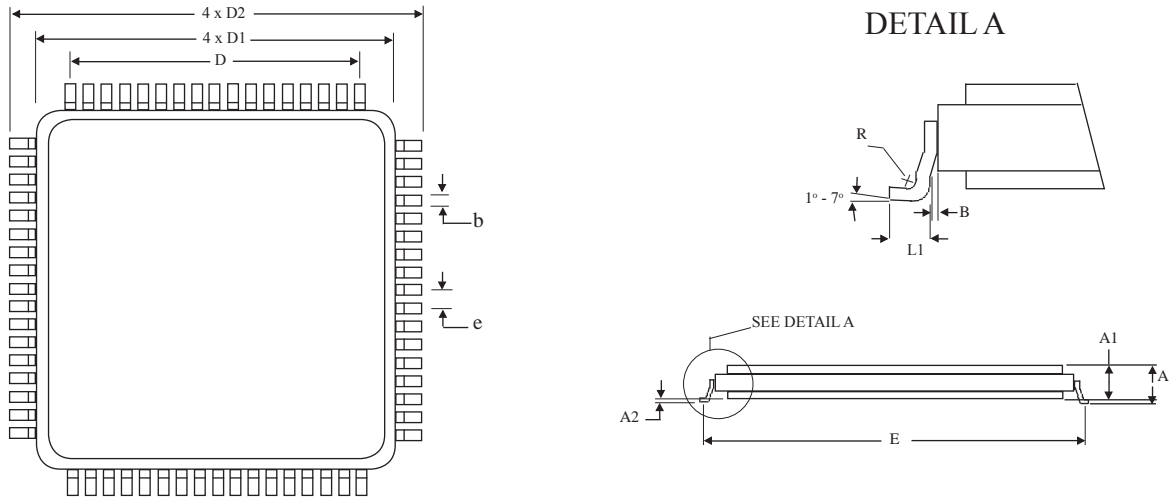
### LOW $V_{CC}$ DATA RETENTION WAVEFORM





## MECHANICAL DEFINITIONS\*

Micross Case #702 (Package Designator Q)  
SMD 5962-94611, Case Outline M

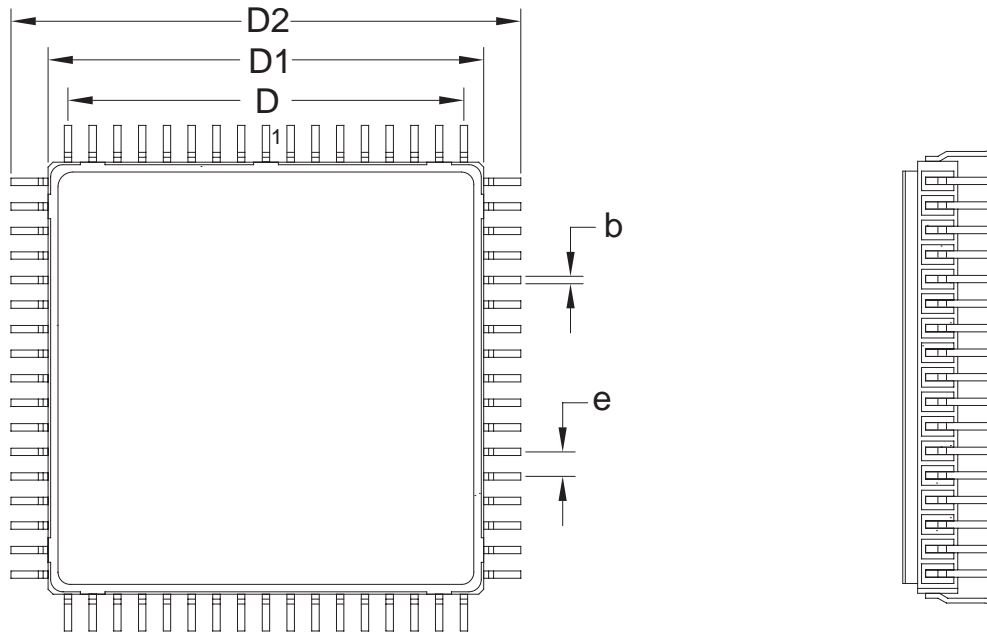


SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	0.123	0.200
A1	0.118	0.186
A2	0.000	0.020
B	0.010 REF	
b	0.013	0.017
D	0.800 BSC	
D1	0.870	0.890
D2	0.980	1.000
E	0.936	0.956
e	0.050 BSC	
R	0.005	---
L1	0.035	0.045

\*All measurements are in inches.

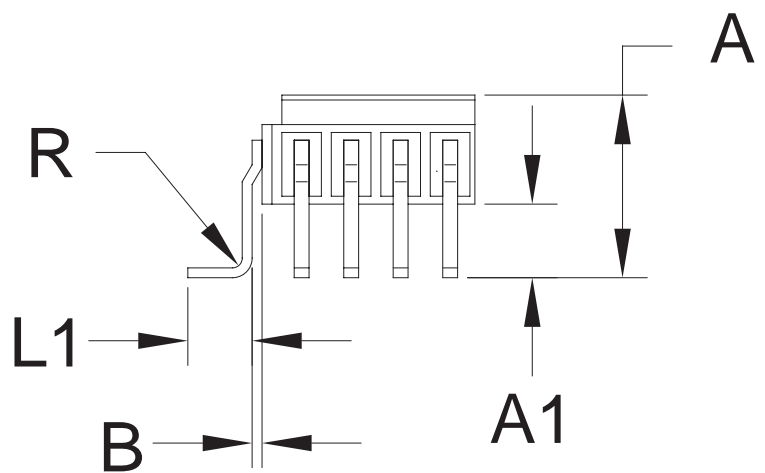
## MECHANICAL DEFINITIONS\*

Microcross Package Designator Q2



PACKAGE SPECIFICATION		
Symbol	Min	Max
A		.200
A1	.070	.080
B	.013	.017
b	.010 REF	
D	.800 BSC	
D1	.870	.890
D2	.980	1.00
e	.050 BSC	
R	.010 TYP	
L1	.035	.045

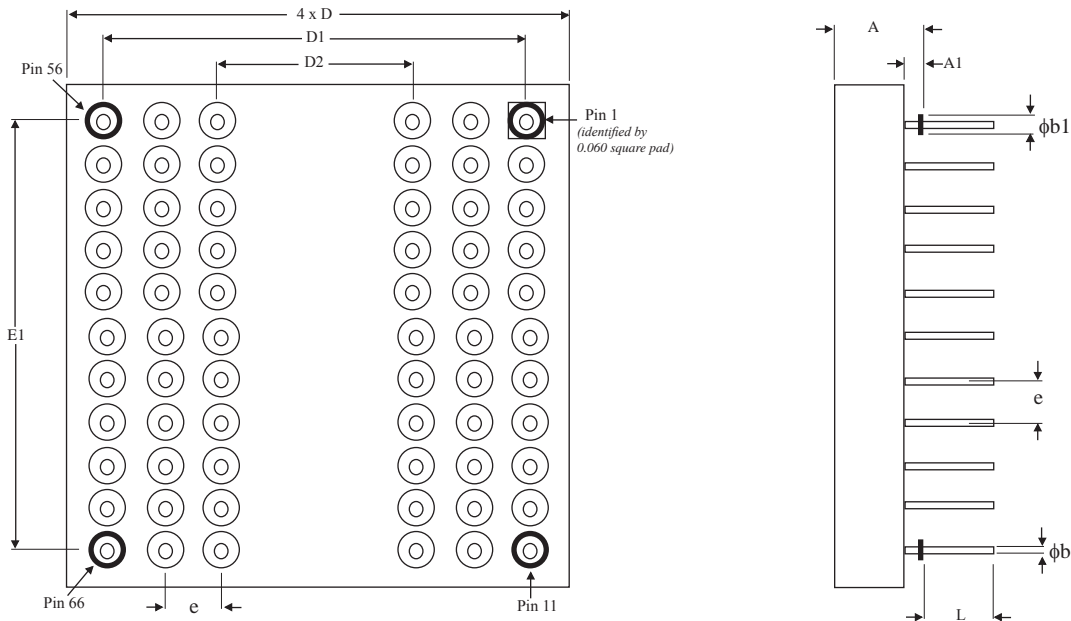
Dimensions are in inches.



\*All measurements are in inches.

## MECHANICAL DEFINITIONS\*

Micross Case #904 (Package Designator P )  
SMD 5962-94611, Case Outline T

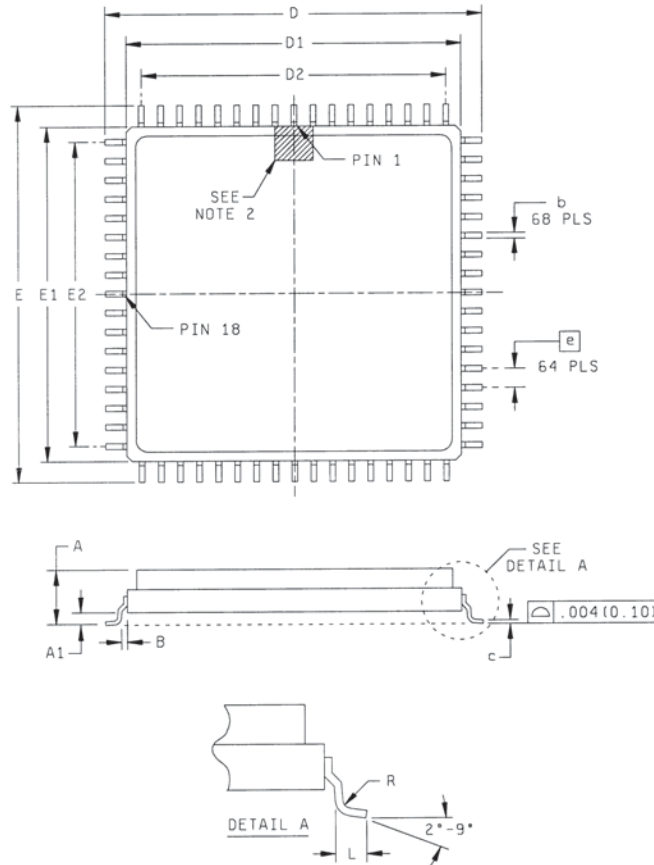


SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	0.144	0.181
A1	0.025	0.035
$\phi b$	0.016	0.020
$\phi b1$	0.045	0.055
D	1.065	1.085
D1/E1	1.000 TYP	
D2	0.600 TYP	
e	0.100 TYP	
L	0.145	0.155

\*All measurements are in inches.

## MECHANICAL DEFINITIONS\*

Micross Case (Package Designator Q1)  
SMD 5962-94611, Case Outline A

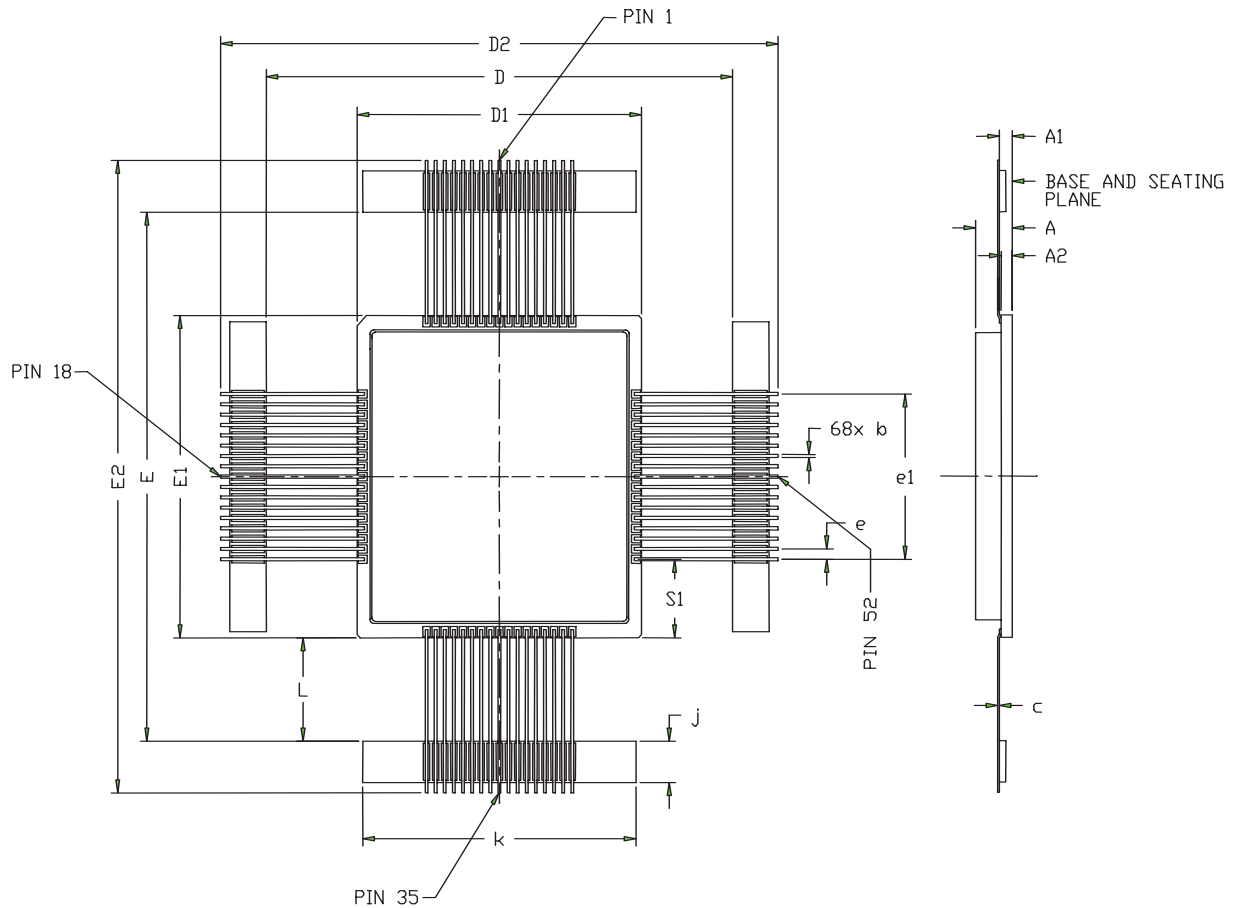


SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	---	0.200
A1	0.054	---
b	0.013	0.017
B	0.010 TYP	
c	0.009	0.012
D/E	0.980	1.000
D1/E1	0.870	0.890
D2/E2	0.800 BSC	
e	0.050 BSC	
L	0.035	0.045
R	0.010 TYP	

\*All measurements are in inches.

## MECHANICAL DEFINITIONS\*

Micross Case (Package Designator BQFP)  
SMD 5962-95624, Case Outline N



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.92	5.10	.115	.200
A1	1.40	1.65	.055	.065
A2	1.14	1.40	.045	.055
b	0.30	0.46	.012	.018
C	0.23	0.31	.009	.012
D/E	63.63	66.42	2.505	2.615
D1/E1	39.24	40.01	1.545	1.575
D2/E2	71.25	84.20	2.805	3.315
e	1.14	1.40	.045	.055
e1	20.19	20.45	.795	.805
j	4.83	5.33	.190	.210
k	37.72	38.48	1.485	1.515
L	12.19	13.21	.480	.520
S1	9.45	9.86	.372	.388

## ORDERING INFORMATION

Device Number	Package Type	Speed (ns)	Power Option	Process
AS8S512K32	Q, Q1, Q2, P or BQFP	-12, -15, -17, -20, -25, -35, -45 or -55	L (Low Power) Blank (Std power)	/*

**Examples:**

AS8S512K32Q-15/Q  
AS8S512K32P-17L/Q  
AS8S512K32P-25/XT  
AS8S512K32Q1-55/IT  
AS8S512K32BQFP-55/883C

**\*Available Processes**

IT = Industrial Temperature Range      -40<sup>0</sup>C to +85<sup>0</sup>C  
XT = Military Temperature Range        -55<sup>0</sup>C to +125<sup>0</sup>C  
Q & 883C = Full Military Processing      -55<sup>0</sup>C to +125<sup>0</sup>C

## MICROSS TO DSCC PART NUMBER CROSS REFERENCE

### Package Designator Q

<u>Micross Part#</u>	<u>SMD Part#</u>
AS8S512K32Q-12/Q	5962-9461118HMA
AS8S512K32Q-12/Q	5962-9461118HMC
AS8S512K32Q-12L/Q	5962-9461120HMA
AS8S512K32Q-12L/Q	5962-9461120HMC
AS8S512K32Q-15/Q	5962-9461117HMA
AS8S512K32Q-15/Q	5962-9461117HMC
AS8S512K32Q-15L/Q	5962-9461119HMA
AS8S512K32Q-15L/Q	5962-9461119HMC
AS8S512K32Q-17/Q	5962-9461116HMA
AS8S512K32Q-17/Q	5962-9461116HMC
AS8S512K32Q-17L/Q	5962-9461110HMA
AS8S512K32Q-17L/Q	5962-9461110HMC
AS8S512K32Q-20/Q	5962-9461115HMA
AS8S512K32Q-20/Q	5962-9461115HMC
AS8S512K32Q-20L/Q	5962-9461109HMA
AS8S512K32Q-20L/Q	5962-9461109HMC
AS8S512K32Q-25/Q	5962-9461114HMA
AS8S512K32Q-25/Q	5962-9461114HMC
AS8S512K32Q-25L/Q	5962-9461108HMA
AS8S512K32Q-25L/Q	5962-9461108HMC
AS8S512K32Q-35/Q	5962-9461113HMA
AS8S512K32Q-35/Q	5962-9461113HMC
AS8S512K32Q-35L/Q	5962-9461107HMA
AS8S512K32Q-35L/Q	5962-9461107HMC
AS8S512K32Q-45/Q	5962-9461112HMA
AS8S512K32Q-45/Q	5962-9461112HMC
AS8S512K32Q-45L/Q	5962-9461106HMA
AS8S512K32Q-45L/Q	5962-9461106HMC
AS8S512K32Q-55/Q	5962-9461111HMA
AS8S512K32Q-55/Q	5962-9461111HMC
AS8S512K32Q-55L/Q	5962-9461105HMA
AS8S512K32Q-55L/Q	5962-9461105HMC

### Package Designator Q1

<u>Micross Part#</u>	<u>SMD Part#</u>
AS8S512K32Q1-12/883C	5962-9461118HAA
AS8S512K32Q1-12/883C	5962-9461118HAC
AS8S512K32Q1-12L/883	5962-9461120HAA
AS8S512K32Q1-12L/883	5962-9461120HAC
AS8S512K32Q1-15/883C	5962-9461117HAA
AS8S512K32Q1-15/883C	5962-9461117HAC
AS8S512K32Q1-15L/883	5962-9461119HAA
AS8S512K32Q1-15L/883	5962-9461119HAC
AS8S512K32Q1-17/883C	5962-9461116HAA
AS8S512K32Q1-17/883C	5962-9461116HAC
AS8S512K32Q1-17L/883	5962-9461110HAA
AS8S512K32Q1-17L/883	5962-9461110HAC
AS8S512K32Q1-20/883C	5962-9461115HAA
AS8S512K32Q1-20/883C	5962-9461115HAC
AS8S512K32Q1-20L/883	5962-9461109HAA
AS8S512K32Q1-20L/883	5962-9461109HAC
AS8S512K32Q1-25/883C	5962-9461114HAA
AS8S512K32Q1-25/883C	5962-9461114HAC
AS8S512K32Q1-25L/883	5962-9461108HAA
AS8S512K32Q1-25L/883	5962-9461108HAC
AS8S512K32Q1-35/883C	5962-9461113HAA
AS8S512K32Q1-35/883C	5962-9461113HAC
AS8S512K32Q1-35L/883	5962-9461107HAA
AS8S512K32Q1-35L/883	5962-9461107HAC
AS8S512K32Q1-45/883C	5962-9461112HAA
AS8S512K32Q1-45/883C	5962-9461112HAC
AS8S512K32Q1-45L/883	5962-9461106HAA
AS8S512K32Q1-45L/883	5962-9461106HAC
AS8S512K32Q1-55/883C	5962-9461111HAA
AS8S512K32Q1-55/883C	5962-9461111HAC
AS8S512K32Q1-55L/883	5962-9461105HAA
AS8S512K32Q1-55L/883	5962-9461105HAC

### Package Designator P

<u>Micross Part#</u>	<u>SMD Part#</u>
AS8S512K32P-12/Q	5962-9461118HTA
AS8S512K32P-12/Q	5962-9461118HTC
AS8S512K32P-12L/Q	5962-9461120HTA
AS8S512K32P-12L/Q	5962-9461120HTC
AS8S512K32P-15/Q	5962-9461117HTA
AS8S512K32P-15/Q	5962-9461117HTC
AS8S512K32P-15L/Q	5962-9461119HTA
AS8S512K32P-15L/Q	5962-9461119HTC
AS8S512K32P-17/Q	5962-9461116HTA
AS8S512K32P-17/Q	5962-9461116HTC
AS8S512K32P-17L/Q	5962-9461110HTA
AS8S512K32P-17L/Q	5962-9461110HTC
AS8S512K32P-20/Q	5962-9461115HTA
AS8S512K32P-20/Q	5962-9461115HTC
AS8S512K32P-20L/Q	5962-9461109HTA
AS8S512K32P-20L/Q	5962-9461109HTC
AS8S512K32P-25/Q	5962-9461114HTA
AS8S512K32P-25/Q	5962-9461114HTC
AS8S512K32P-25L/Q	5962-9461108HTA
AS8S512K32P-25L/Q	5962-9461108HTC
AS8S512K32P-35/Q	5962-9461113HTA
AS8S512K32P-35/Q	5962-9461113HTC
AS8S512K32P-35L/Q	5962-9461107HTA
AS8S512K32P-35L/Q	5962-9461107HTC
AS8S512K32P-45/Q	5962-9461112HTA
AS8S512K32P-45/Q	5962-9461112HTC
AS8S512K32P-45L/Q	5962-9461106HTA
AS8S512K32P-45L/Q	5962-9461106HTC
AS8S512K32P-55/Q	5962-9461111HTA
AS8S512K32P-55/Q	5962-9461111HTC
AS8S512K32P-55L/Q	5962-9461105HTA
AS8S512K32P-55L/Q	5962-9461105HTC

### Package Designator BQFP

<u>Micross Part#</u>	<u>SMD Part#</u>
AS8S512K32BQFP-20/883C	5962-9562409HNC
AS8S512K32BQFP-25/883C	5962-9562408HNC
AS8S512K32BQFP-25/883C	5962-9562412HNC
AS8S512K32BQFP-35/883C	5962-9562407HNC
AS8S512K32BQFP-35/883C	5962-9562411HNC
AS8S512K32BQFP-45/883C	5962-9562406HNC
AS8S512K32BQFP-45/883C	5962-9562410HNC
AS8S512K32BQFP-55/883C	5962-9562405HNC

**DOCUMENT TITLE**

512K x 32 SRAM MEMORY ARRAY

<u>Rev #</u>	<u>History</u>	<u>Release Date</u>	<u>Status</u>																																																												
6.5	Updated Features, Temp Range & General Description - Page 1, Updated Order Chart - Page 13, Removed Space Processing - Page 13	April 2010	Release																																																												
6.6	Updated Ordering Table, Page 14 Updated DSCC Cross Reference, Page 15 Added SMD 5962-95624, Page 1 Added BQFP Package, Page 1 and added BQFP drawing on page 13 (BQFP package is listed on SMD 5962-95624)	June 2010	Release																																																												
6.7	Updated Q2 Spec, Page 10	July 2010	Release																																																												
6.8	Page 3 Changes:	June 2011	Release																																																												
	<table border="1"> <thead> <tr> <th></th> <th><u>From</u></th> <th><u>To</u></th> </tr> </thead> <tbody> <tr> <td>•<math>I_{CC}</math> (mA)</td> <td></td> <td></td> </tr> <tr> <td>-17</td> <td>700</td> <td>175</td> </tr> <tr> <td>-20</td> <td>650</td> <td>150</td> </tr> <tr> <td>-25</td> <td>600</td> <td>140</td> </tr> <tr> <td>-35</td> <td>570</td> <td>130</td> </tr> <tr> <td>-45</td> <td>570</td> <td>120</td> </tr> <tr> <td>-55</td> <td>550</td> <td>110</td> </tr> <tr> <td>•<math>I_{SBT1}</math> (mA)</td> <td></td> <td></td> </tr> <tr> <td>-12</td> <td>80</td> <td>40</td> </tr> <tr> <td>-15</td> <td>80</td> <td>40</td> </tr> <tr> <td>-17</td> <td>240</td> <td>40</td> </tr> <tr> <td>-20</td> <td>240</td> <td>35</td> </tr> <tr> <td>-25</td> <td>190</td> <td>35</td> </tr> <tr> <td>-35</td> <td>190</td> <td>30</td> </tr> <tr> <td>-45</td> <td>150</td> <td>30</td> </tr> <tr> <td>-55</td> <td>150</td> <td>30</td> </tr> <tr> <td>•<math>I_{SBT2}</math> (mA)</td> <td>80</td> <td>20</td> </tr> <tr> <td>•2V <math>I_{CCDR}</math> (mA)</td> <td>20</td> <td>10</td> </tr> <tr> <td>•3V <math>I_{CCDR}</math> (mA)</td> <td>28</td> <td>12</td> </tr> </tbody> </table>		<u>From</u>	<u>To</u>	• $I_{CC}$ (mA)			-17	700	175	-20	650	150	-25	600	140	-35	570	130	-45	570	120	-55	550	110	• $I_{SBT1}$ (mA)			-12	80	40	-15	80	40	-17	240	40	-20	240	35	-25	190	35	-35	190	30	-45	150	30	-55	150	30	• $I_{SBT2}$ (mA)	80	20	•2V $I_{CCDR}$ (mA)	20	10	•3V $I_{CCDR}$ (mA)	28	12		
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	•Removed note from page 8 "-12 &-15 have a 32mA limit".																																																														



<u>Rev #</u>	<u>History</u>	<u>Release Date</u>	<u>Status</u>
6.9	Added 68 Lead CQFP (BQFP) Military SMD Pinout Option	August 2013	Release