

**256K x 4 Static RAM**

**Features**

- High speed
  - $t_{AA} = 15 \text{ ns}$
- CMOS for optimum speed/power
- Low active power
  - 495 mW
- Low standby power
  - 275 mW
- 2.0V data retention (optional)
- Automatic power-down when deselected
- TTL-compatible inputs and outputs

**Functional Description**

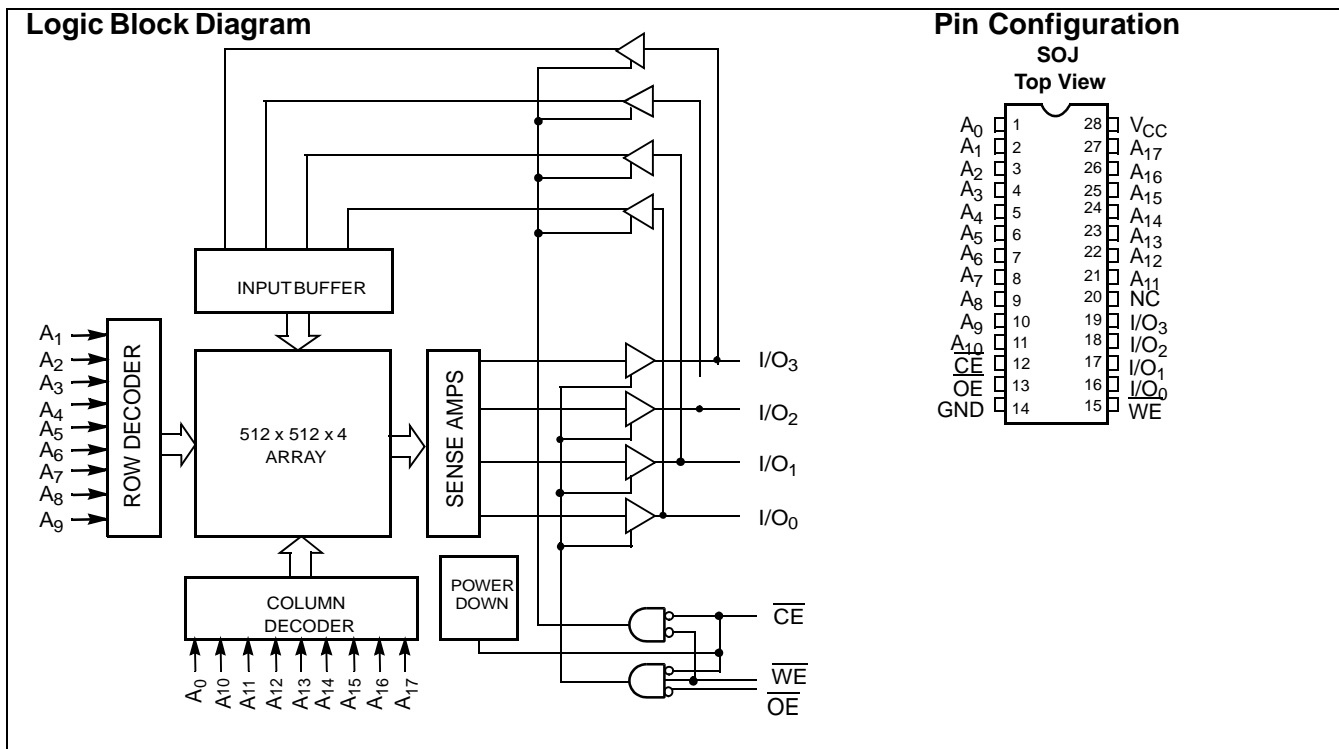
The CY7C106BN and CY7C1006BN are high-performance CMOS static RAMs organized as 262,144 words by 4 bits. Easy memory expansion is provided by an active **LOW** Chip Enable ( $\overline{CE}$ ), an active **LOW** Output Enable ( $\overline{OE}$ ), and three-state drivers. These devices have an automatic power-down feature that reduces power consumption by more than 65% when the devices are deselected.

Writing to the devices is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Write Enable ( $\overline{WE}$ ) inputs **LOW**. Data on the four I/O pins ( $I/O_0$  through  $I/O_3$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{17}$ ).

Reading from the devices is accomplished by taking Chip Enable ( $\overline{CE}$ ) and Output Enable ( $\overline{OE}$ ) **LOW** while forcing Write Enable ( $\overline{WE}$ ) **HIGH**. Under these conditions, the contents of the memory location specified by the address pins will appear on the four I/O pins.

The four input/output pins ( $I/O_0$  through  $I/O_3$ ) are placed in a high-impedance state when the devices are deselected ( $\overline{CE}$  **HIGH**), the outputs are disabled ( $\overline{OE}$  **HIGH**), or during a write operation ( $\overline{CE}$  and  $\overline{WE}$  **LOW**).

The CY7C106BN is available in a standard 400-mil-wide SOJ; the CY7C1006BN is available in a standard 300-mil-wide SOJ.



### Selection Guide

	7C106BN-15 7C1006BN-15	7C106BN-20 7C1006BN-20
Maximum Access Time (ns)	15	20
Maximum Operating Current (mA)	80	75
Maximum Standby Current (mA)	30	30

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....-65°C to +150°C  
 Ambient Temperature with  
 Power Applied .....-55°C to +125°C  
 Supply Voltage on V<sub>CC</sub> Relative to GND<sup>[1]</sup> .... -0.5V to +7.0V  
 DC Voltage Applied to Outputs  
 in High Z State<sup>[1]</sup> .....-0.5V to V<sub>CC</sub> + 0.5V  
 DC Input Voltage<sup>[1]</sup> .....-0.5V to V<sub>CC</sub> + 0.5V

Current into Outputs (LOW)..... 20 mA  
 Static Discharge Voltage ..... >2001V  
 (per MIL-STD-883, Method 3015)  
 Latch-Up Current ..... >200 mA

### Operating Range

Range	Ambient Temperature <sup>[2]</sup>	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 10%
Industrial	-45°C to +85°C	

### Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	7C106BN-15 7C1006BN-15		7C106BN-20 7C1006BN-20		Unit
			Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3	2.2	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage <sup>[1]</sup>		-0.3	0.8	-0.3	0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1	+1	-1	+1	mA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	mA
I <sub>OS</sub>	Output Short Circuit Current <sup>[3]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-300		-300	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>RC</sub>		80		75	mA
I <sub>SB1</sub>	Automatic CE Power-Down Current —TTL Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>IH</sub> , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		30		30	mA
I <sub>SB2</sub>	Automatic CE Power-Down Current —CMOS Inputs	Max. V <sub>CC</sub> , CE ≥ V <sub>CC</sub> - 0.3V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f=0	Com'l	10		10	mA

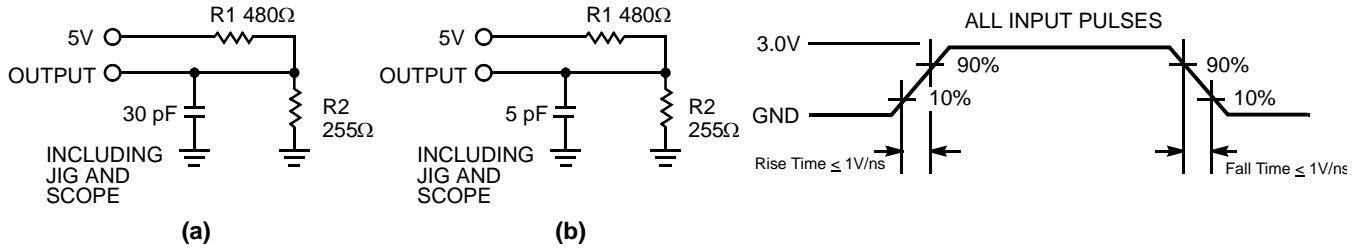
### Capacitance<sup>[4]</sup>

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub> : Addresses	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	7	pF
C <sub>IN</sub> : Controls			10	pF
C <sub>OUT</sub>	Output Capacitance		10	pF

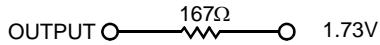
#### Notes:

- V<sub>IL</sub> (min.) = -2.0V for pulse durations of less than 20 ns.
- T<sub>A</sub> is the "instant on" case temperature.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- Tested initially and after any design or process changes that may affect these parameters.

### AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



### Switching Characteristics Over the Operating Range<sup>[5]</sup>

Parameter	Description	7C106B-15 7C1006B-15		7C106B-20 7C1006B-20		Unit
		Min.	Max.	Min.	Max.	
<b>READ CYCLE</b>						
$t_{RC}$	Read Cycle Time	15		20		ns
$t_{AA}$	Address to Data Valid		15		20	ns
$t_{OHA}$	Data Hold from Address Change	3		3		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		15		20	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		7		8	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z	0		0		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[6, 7]</sup>		7		8	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[7]</sup>	3		3		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[6, 7]</sup>		7		8	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up	0		0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down		15		20	ns
<b>WRITE CYCLE<sup>[8, 9]</sup></b>						
$t_{WC}$	Write Cycle Time	15		20		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	12		15		ns
$t_{AW}$	Address Set-Up to Write End	12		15		ns
$t_{HA}$	Address Hold from Write End	0		0		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	12		15		ns
$t_{SD}$	Data Set-Up to Write End	8		10		ns
$t_{HD}$	Data Hold from Write End	0		0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[7]</sup>	3		3		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[6, 7]</sup>		7		8	ns

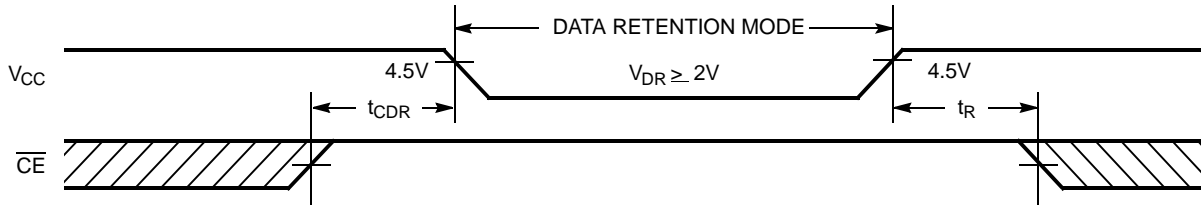
**Notes:**

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

**Data Retention Characteristics** Over the Operating Range

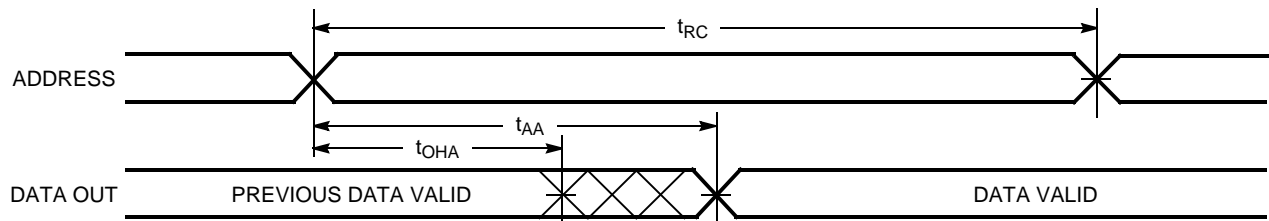
Parameter	Description	Conditions <sup>[10]</sup>	Min.	Max.	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		2.0		V
$I_{CCDR}$	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$ , $CE \geq V_{CC} - 0.3V$ ,		250	$\mu A$
$t_{CDR}^{[4]}$	Chip Deselect to Data Retention Time	$V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	0		ns
$t_R^{[4]}$	Operation Recovery Time		200		ms

**Data Retention Waveform**

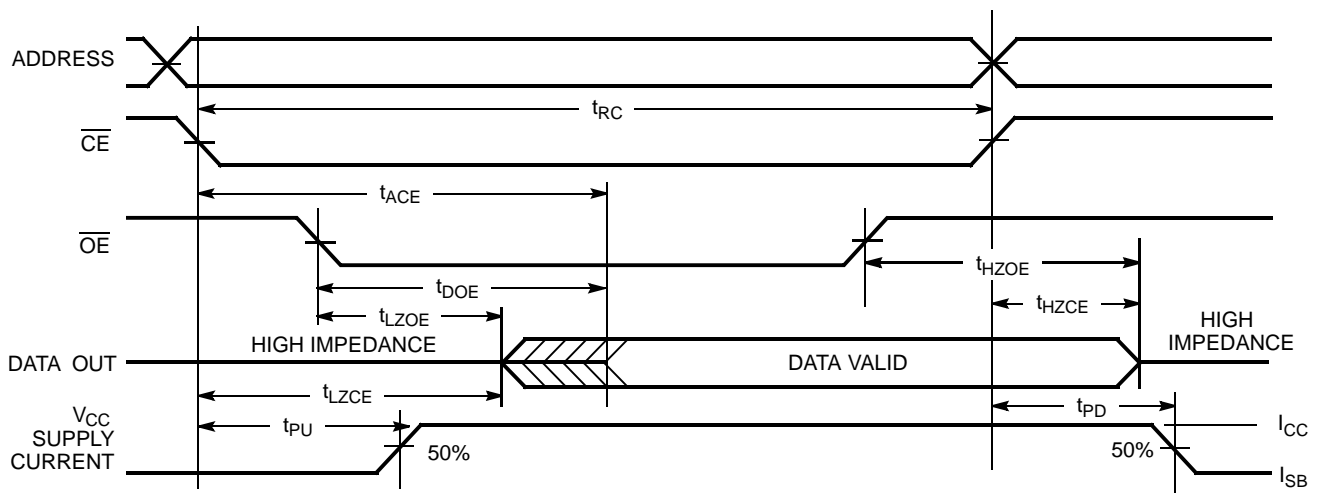


**Switching Waveforms**

**Read Cycle No.1<sup>[11, 12]</sup>**



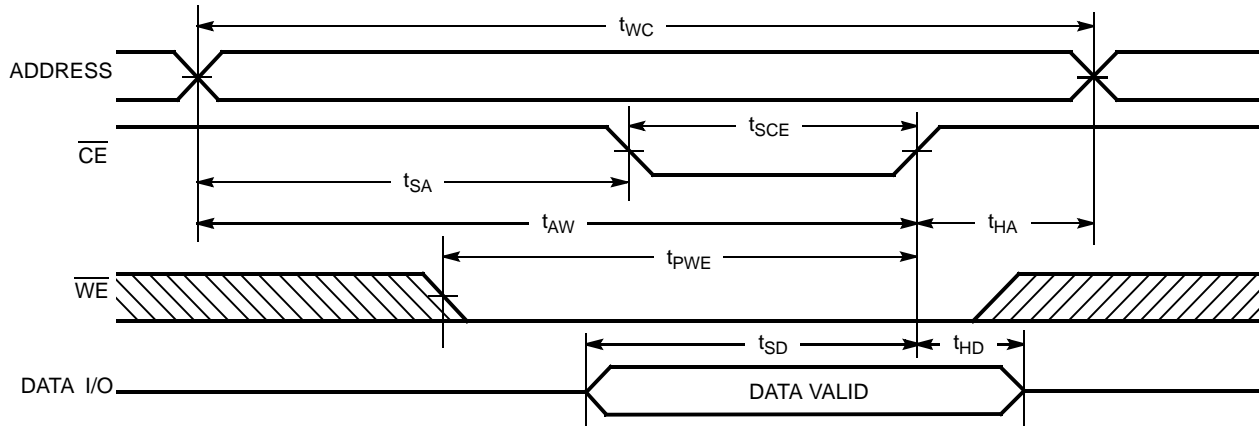
**Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[12, 13]</sup>**



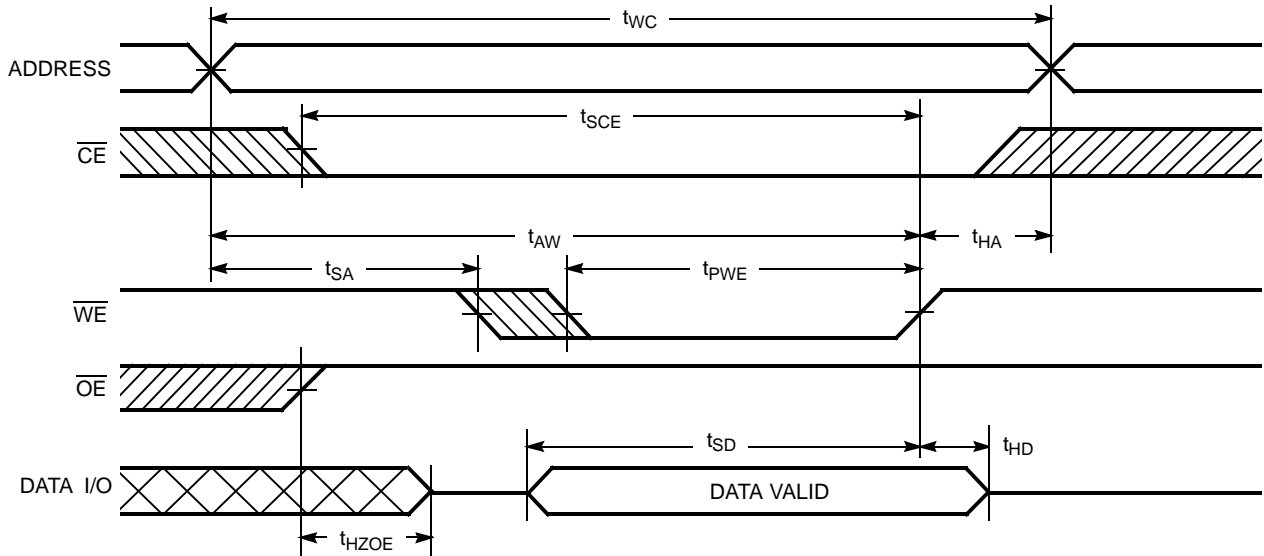
**Notes:**

- 10. No input may exceed  $V_{CC} + 0.5V$ .
- 11. Device is continuously selected,  $\overline{OE}$  and  $\overline{CE} = V_{IL}$ .
- 12.  $\overline{WE}$  is HIGH for read cycle.
- 13. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

**Switching Waveforms** (continued)  
**Write Cycle No. 1 ( $\overline{CE}$  Controlled)**<sup>[14, 15]</sup>



**Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write)**<sup>[14, 15]</sup>

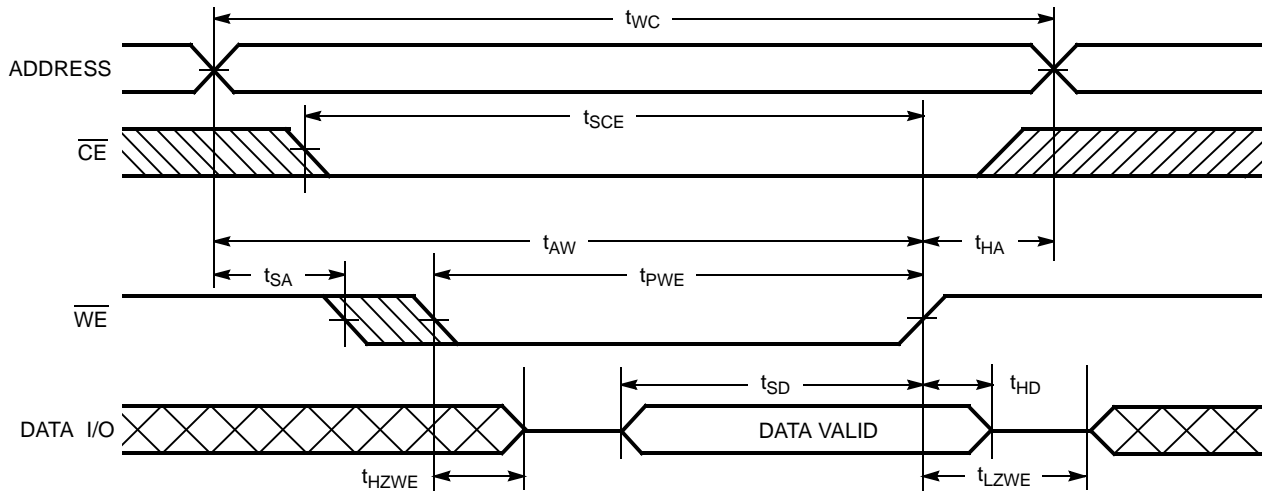


**Notes:**

- 14. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.
- 15. Data I/O is high impedance if  $\overline{OE} = V_{IH}$ .

**Switching Waveforms (continued)**

**Write Cycle No. 3 (WE Controlled, OE LOW)<sup>[9, 15]</sup>**



**Truth Table**

CE	OE	WE	Input/Output	Mode	Power
H	X	X	High Z	Power-Down	Standby ( $I_{SB}$ )
L	L	H	Data Out	Read	Active ( $I_{CC}$ )
L	X	L	Data In	Write	Active ( $I_{CC}$ )
L	H	H	High Z	Selected, Outputs Disabled	Active ( $I_{CC}$ )

**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
15	CY7C106BN-15VC	51-85032	28-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1006BN-15VC	51-85031	28-Lead (300-Mil) Molded SOJ	
20	CY7C106BN-20VC	51-85032	28-Lead (400-Mil) Molded SOJ	Commercial

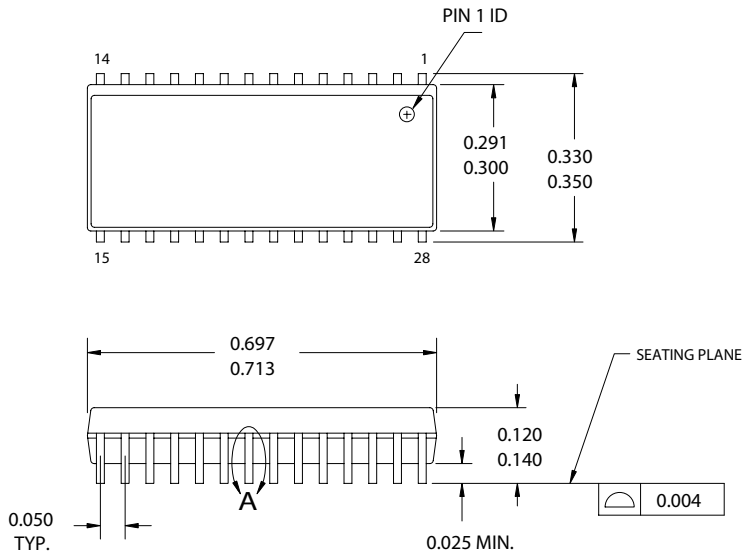
Please contact local sales representative regarding availability of these parts.

**Package Diagrams**

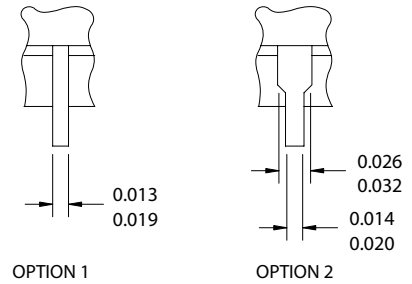
**28-pin (300-Mil) Molded SOJ (51-85031)**

NOTE:

1. JEDEC STD REF MO088
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH  
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.006 in (0.152 mm) PER SIDE
3. DIMENSIONS IN INCHES  
MIN.  
MAX.

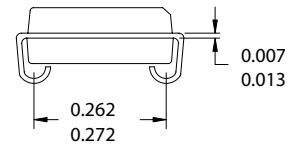


**DETAIL A**  
**EXTERNAL LEAD DESIGN**



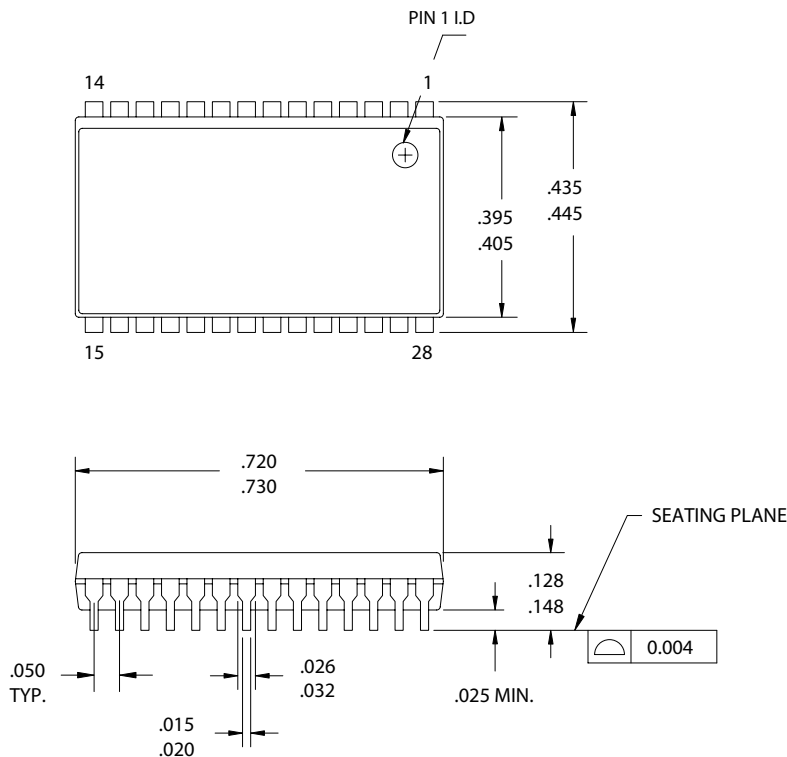
OPTION 1

OPTION 2

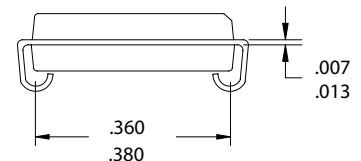


51-85031-°C

**28-Lead (400-Mil) Molded SOJ (51-85032)**



DIMENSIONS IN INCHES  
MIN.  
MAX.



51-85032-°B

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## Document History Page

<b>Document Title: CY7C106BN/CY7C1006BN 256K x 4 Static RAM</b> <b>Document Number: 001-06429</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	423847	See ECN	NXR	New Data sheet