PRELIMINARY
Notice: This is not a final specification
Some parametric limits are subject to change.

M5M4V18167CTP-5,-6,-7, -5S,-6S,-7S

PIPELINE BURST MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

The M5M4V18167CTP is pipeline burst dynamic RAM organized 1048574-words by 16-bits. This is fablicated with the high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low cost are essential.

The use of double-layer metal process combined with twin-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M4V18167CTP-5,-5S	50	10	25	10	90	540
M5M4V18167CTP-6,-6S	60	11.6	30	12	110	450
M5M4V18167CTP-7,-7S	70	15	35	15	130	390

- Standard 50 pin TSOP
- Single 3.3V +0.3V, -0.15V supply (3.15V~3.6V)
- Low stand-by power dissipation
  1.8mW (Max) ·····CMOS input level
- Low operating power dissipation
  M5M4V18167CTP- 5,-5S ·····650.0mW (Max)
  M5M4V18167CTP- 6,-6S ·····540.0mW (Max)
  M5M4V18167CTP- 7,-7S ·····470.0mW (Max)
- Pipeline Burst mode , $\overline{RAS}$-only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write mode and $\overline{OE}$ to control output buffer impedance
  All inputs, output LVTTL compatible and low capacitance
- 1024 refresh cycles every 16.4ms (A_0~A_9)
  *: Applicable to self refresh version (M5M4V18167CTP-5S,-6S, -7S: option) only

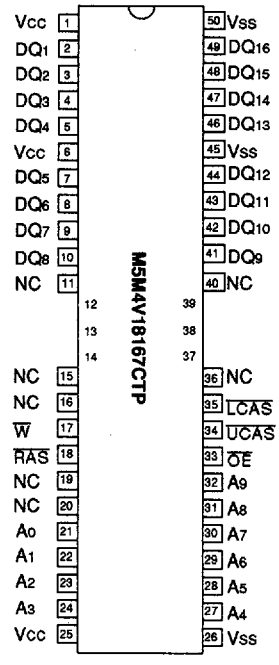
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN DESCRIPTION

Pin name	Function
A_0~A_9	Address inputs
DQ_1~DQ_{16}	Data inputs / outputs
$\overline{RAS}$	Row address strobe input
$\overline{UCAS}$	Upper byte control column address strobe input
$\overline{LCAS}$	Lower byte control column address strobe input
$\overline{W}$	Write control input
$\overline{OE}$	Output enable input
Vcc	Power supply (+3.3V)
Vss	Ground (0V)

PIN CONFIGURATION (TOP VIEW)



Outline 50P3G-F (400mil TSOP Normal Bend)

NC:NO CONNECTION

PRELIMINARY

Notice: This is not a final specification
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M5M4V18167CTP-5,-6,-7,-5S,-6S,-7S

PIPELINE BURST MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

FUNCTION

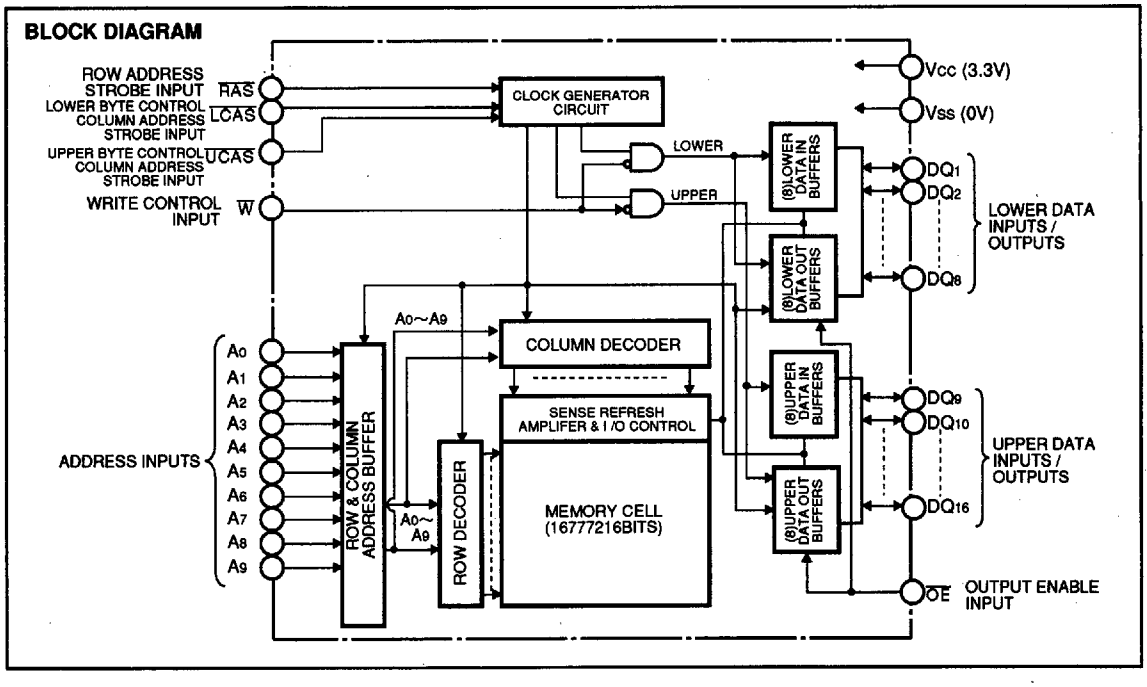
The M5M4V18167CTP provide, in addtion to normal read, write, and read-modify-write operations, a number of other functions, e.g., pipeline burst mode, $\overline{RAS}$ only refresh. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ_1~DQ_8	DQ_9~DQ_{16}
Lower byte read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower byte write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper byte write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
$\overline{RAS}$-only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Stand-by	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : Invalid, APD : applied, OPN : open

BLOCK DIAGRAM

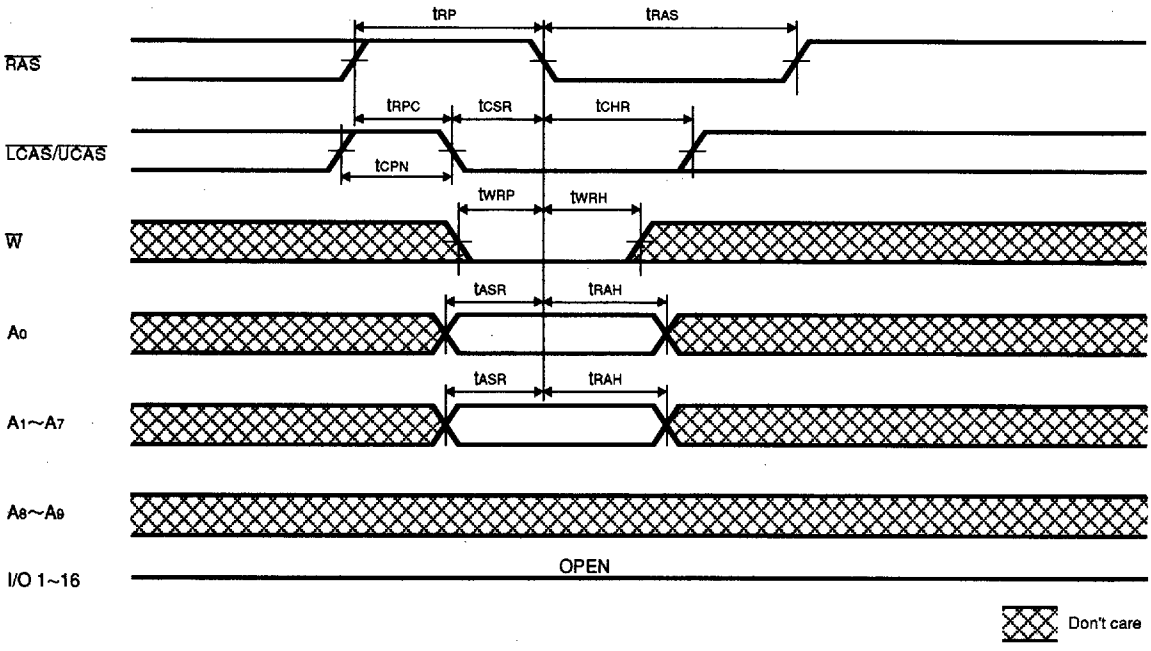


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change

Burst Address Sequence Table

	INTERLEAVE				LINEAR			
1st	X..X00	X..X01	X..X10	X..X11	X..X00	X..X01	X..X10	X..X11
2nd	X..X01	X..X00	X..X11	X..X10	X..X01	X..X10	X..X11	X..X00
3rd	X..X10	X..X11	X..X00	X..X01	X..X10	X..X11	X..X00	X..X01
4th	X..X11	X..X10	X..X01	X..X00	X..X11	X..X00	X..X01	X..X10

Burst Address Sequence Set Cycle



Note 1: Address Table for Burst address sequence setting cycle.

	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Linear	X	X	L	L	H	L	L	L	L	L
Interleave	X	X	L	L	H	L	L	L	L	H

2: The burst sequence will remain set untill the device power is interrupted or another Burst address sequence setting cycle.
3: A $\overline{RAS}$ only or CBR refresh cycle must follow the Burst address setting cycle to exit the programming mode.

PRELIMINARY

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M5M4V18167CTP-5,-6,-7,-5S,-6S,-7S

PIPELINE BURST MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to Vss	−0.5～4.6	V
V_I	Input voltage		−0.5～4.6	V
V_O	Output voltage		−0.5～4.6	V
I_O	Output current		50	mA
P_d	Power dissipation	Ta=25℃	1000	mW
T_{opr}	Operating temperature		0～70	℃
T_{stg}	Storage temperature		−65～150	℃

RECOMMENDED OPERATING CONDITIONS (Ta=0～70℃, unless otherwise noted) (Note 4)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	3.15	3.3	3.6	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.0		Vcc+0.3	V
V_{IL}	Low-level input voltage, all inputs	−0.3		0.8	V

Note 4 : All voltage values are with respect to Vss.

ELECTRICAL CHARACTERISTICS (Ta=0～70 ℃, Vcc=3.15V～3.6V, Vss=0V, unless otherwise noted) (Note 5)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=−2.0mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=2.0mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦3.3V	−10		10	μA
I_I	Input current		0V≦V_{IN}≦3.6V, Other inputs pins=0V	−10		10	μA
I_{CC1} (AV)	Average supply current from Vcc, operating (Note 6,7,8)	M5M4V18167C-5,-5S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			180	mA
		M5M4V18167C-6,-6S				150	
		M5M4V18167C-7,-7S				130	
I_{CC2}	Supply current from Vcc, stand-by (Note 8)		$\overline{RAS}$=$\overline{CAS}$=V_{IH}, output open			2	mA
			$\overline{RAS}$=$\overline{CAS}$≧Vcc −0.2 V			0.5	
I_{CC2}*	Supply current from Vcc, stand-by (Note 9)		$\overline{RAS}$=$\overline{CAS}$≧Vcc −0.2 V			150	μA
I_{CC3} (AV)	Average supply current from Vcc, refreshing (Note 6,8)	M5M4V18167C-5,-5S	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH} t_{RC}=min. output open			180	mA
		M5M4V18167C-6,-6S				150	
		M5M4V18167C-7,-7S				130	
I_{CC4}(AV)	Average supply current from Vcc Pipeline-Burst-Mode (Note 6,7)	M5M4V18167C-5,-5S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			150	mA
		M5M4V18167C-6,-6S				140	
		M5M4V18167C-7,-7S				120	
I_{CC6}(AV)	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 6)	M5M4V18167C-5,-5S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			180	mA
		M5M4V18167C-6,-6S				150	
		M5M4V18167C-7,-7S				130	
I_{CC8}(AV) *	Average supply current from Vcc Extended-Refresh-Mode (Note 9)		$\overline{RAS}$ cycling $\overline{CAS}$≦0.2V or $\overline{CAS}$ before $\overline{RAS}$ refresh cycling ($\overline{W}$,$\overline{OE}$,A_0～A_9 ≦0.2V or ≧Vcc−0.2V) DQ=open,t_{RC}=125 μs,t_{RAS}=t_{RAS} min.～1 μs			300	μA
I_{CC9}(AV) *	Average supply current from Vcc Self-Refresh-Mode (Note 9)		$\overline{RAS}$=$\overline{CAS}$ ≦0.2V, output open			200	μA

Note 5: Current flowing into an IC is positive, out is negative.

6: I_{CC1} (AV), I_{CC3} (AV) and I_{CC4} (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

7: I_{CC1} (AV) and I_{CC4} (AV) are dependent on output loading. Specified values are obtained with the output open.

8: Column Address can be changed once or less while $\overline{RAS}$=V_{IL} and $\overline{LCAS}$/$\overline{UCAS}$=V_{IH}.

9: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods (greater than 16.4 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change

PIPELINE BURST MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

CAPACITANCE (Ta=0~70 °C, Vcc=3.15V~3.6V, Vss=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=Vss f=1MHZ V_I=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input				7	pF
$C_{I(W)}$	Input capacitance, write control input				7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				7	pF
$C_{I/O}$	Input/Output capacitance, data ports				7	pF

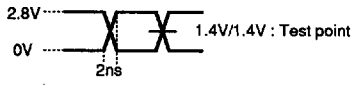
SWITCHING CHARACTERISTICS (Ta=0~70°C, Vcc=3.15V~3.6V, Vss=0V, unless otherwise noted, see notes 10,11)

Symbol	Parameter		Limits						Unit
			M5M4V18167C-5,-5S		M5M4V18167C-6,-6S		M5M4V18167C-7,-7S		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 12)		10		11.6		15	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 13)		50		60		70	ns
t_{AA}	Column address access time	(Note 14)		25		30		35	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 15)		30		35		40	ns
t_{OEA}	Access time from $\overline{OE}$			10		12		15	ns
t_{DOH}	Data hold time from $\overline{CAS}$ Low		3		3		3		ns
t_{OLZ}	Output low impedance time from $\overline{OE}$ low		3		3		3		ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low		3		3		3		ns
t_{OEZ}	Output disable time after $\overline{OE}$ high	(Note 16)	4	10	4	10	4	15	ns
t_{WEZ}	Output disable time after $\overline{WE}$ low	(Note 16)	4	10	4	10	4	15	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 16,17)	4	10	4	10	4	15	ns
t_{REZ}	Output disable time after $\overline{RAS}$ high	(Note 16,17)	4	10	4	10	4	15	ns

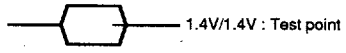
Note 10: AC Measurments t_T=2ns.

11: AC Characteristics test condition

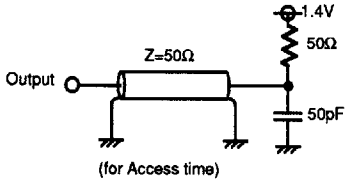
(1) Input timing Specification

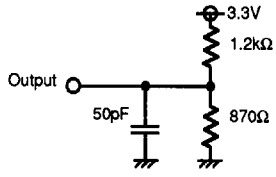


(2) Output timing Specification



(3) Output Load





Note 12: Assumes that $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$ and $t_{CP} \geq t_{CP(max)}$.

13: Assumes that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

14: Assumes that $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$.

15: Assumes that $t_{CP} \leq t_{CP(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

16: t_{OEZ} (max), t_{WEZ}(max), t_{OFF}(max) and t_{REZ}(max)defines the time at which the output achieves the high impedance state ($I_{OUT} \leq | \pm 10 \mu A |$) and is not reference to V_{OH}(min) or V_{OL}(max).

17: Output is disabled after both $\overline{RAS}$ and $\overline{CAS}$ go to high.

PRELIMINARY
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TIMING REQUIREMENTS (for Read, Write, and Refresh Cycles)

(Ta=0~70℃, Vcc = 3.15V~3.6V, Vss=0V, unless otherwise noted, See notes 10,11)

Symbol	Parameter		Limits						Unit
			M5M4V18167C-5,-5S		M5M4V18167C-6,-6S		M5M4V18167C-7,-7S		
			Min	Max	Min	Max	Min	Max	
tRP	$\overline{RAS}$ high pulse width		30		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note18)	18	25	20	31.8	20	40	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		10		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		5		5		5		ns
tCPN	$\overline{CAS}$ high pulse width		10		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note19)	15	25	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		1.5		1.5		1.5		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note20)	1.5		1.5		1.5		ns
tRAH	Row address hold time after $\overline{RAS}$ low		8.5		8.5		8.5		ns
tCAH	Column address hold time after $\overline{CAS}$ low		8.5		8.5		8.5		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note21)	0		0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note21)	0		0		0		ns
tRDD	Delay time, $\overline{RAS}$ high to data	(Note22)	13		15		20		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note22)	13		15		20		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note22)	13		15		20		ns
tRC	Read cycle time		90		110		130		ns
tRAS	$\overline{RAS}$ low pulse width		50	10000	60	10000	70	10000	ns
tCAS	$\overline{CAS}$ low pulse width		5	10000	5	10000	5	10000	ns
tRCS	Read Setup time before $\overline{CAS}$ low		3		3		3		ns
tRCH	Read hold time after $\overline{CAS}$ high	(Note 23)	5		5		5		ns
tRRH	Read hold time after $\overline{RAS}$ high	(Note 23)	10		10		10		ns
tORH	$\overline{RAS}$ hold time after $\overline{OE}$ low		13		15		20		ns
tOCH	$\overline{CAS}$ hold time after $\overline{OE}$ low		13		15		20		ns
tWCS	Write setup time before $\overline{CAS}$ low		3		3		3		ns
tWCH	Write hold time after $\overline{CAS}$ low		5		5		5		ns
tWEP	Write pulse width		7		7		7		ns
tCRW	$\overline{CAS}$ Low to$\overline{RAS}$ High (Required only for Write Cycle)		15		15		15		ns
tDS	Data setup time before $\overline{CAS}$ low or $\overline{W}$ low		3		3		3		ns
tDH	Data hold time after $\overline{CAS}$ low or $\overline{W}$ low		5		5		5		ns
tT	Transition time		1.5	50	1.5	50	1.5	50	ns
tREF	Refresh cycle time			16.4		16.4		16.4	ms
tREF*	Refresh cycle time			128		128		128	ms

Note 18: tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA.

19: tRAD(max) is specified as a reference point only. If tRAD ≧ tRAD(max) and tASC ≦ tASC(max), access time is controlled exclusively by tAA.

20: tASC(max) is specified as a reference point only. If tRCD ≧ tRCD(max) and tASC ≧ tASC(max), access time is controlled exclusively by tCAC.

21: Either tDZC or tDZO must be satisfied.

22: Either tRDD or tCDD or tODD must be satisfied.

23: Either tRCH or tRRH must be satisfied for a read cycle.

PRELIMINARY
Notice: This is not a final specification
Some parametric limits are subject to change

Pipeline Burst Mode Cycle (Read,Read terminated Read,Write,Write terminated Write,Read-Write,Write-Read) (Note 24)

Symbol	Parameter	Limits						Unit
		M5M4V18167C-5,-5S		M5M4V18167C-6,-6S		M5M4V18167C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tPC	Pipeline Burst EDO Cycle	15		16.6		20		ns
tDOH	Output hold time from $\overline{CAS}$ low	3		3		3		ns
tRAS	$\overline{RAS}$ low pulse width for read write cycle (Note25)	50	125000	60	125000	70	125000	ns
tCP	$\overline{CAS}$ high pulse width (Note26)	5		5		5		ns
tCHOL	Hold time to maintain the data Hi -Z until $\overline{CAS}$ access	7		7		7		ns
tOEP	$\overline{OE}$ Pulse Width	7		7		7		ns
tWEP	$\overline{W}$ Pulse Width	7		7		7		ns
tWET	$\overline{W}$ Pulse Width (for Write comand termination)	7		7		7		ns
tWLC	$\overline{W}$ Lock out from $\overline{CAS}$ High	3		3		3		ns

Note 24: All previously specified timing requirements and switching characteristics are applicable to their respective Hyper page mode cycle.

25: tRAS(min) is specified as two cycles of $\overline{CAS}$ input are performed.

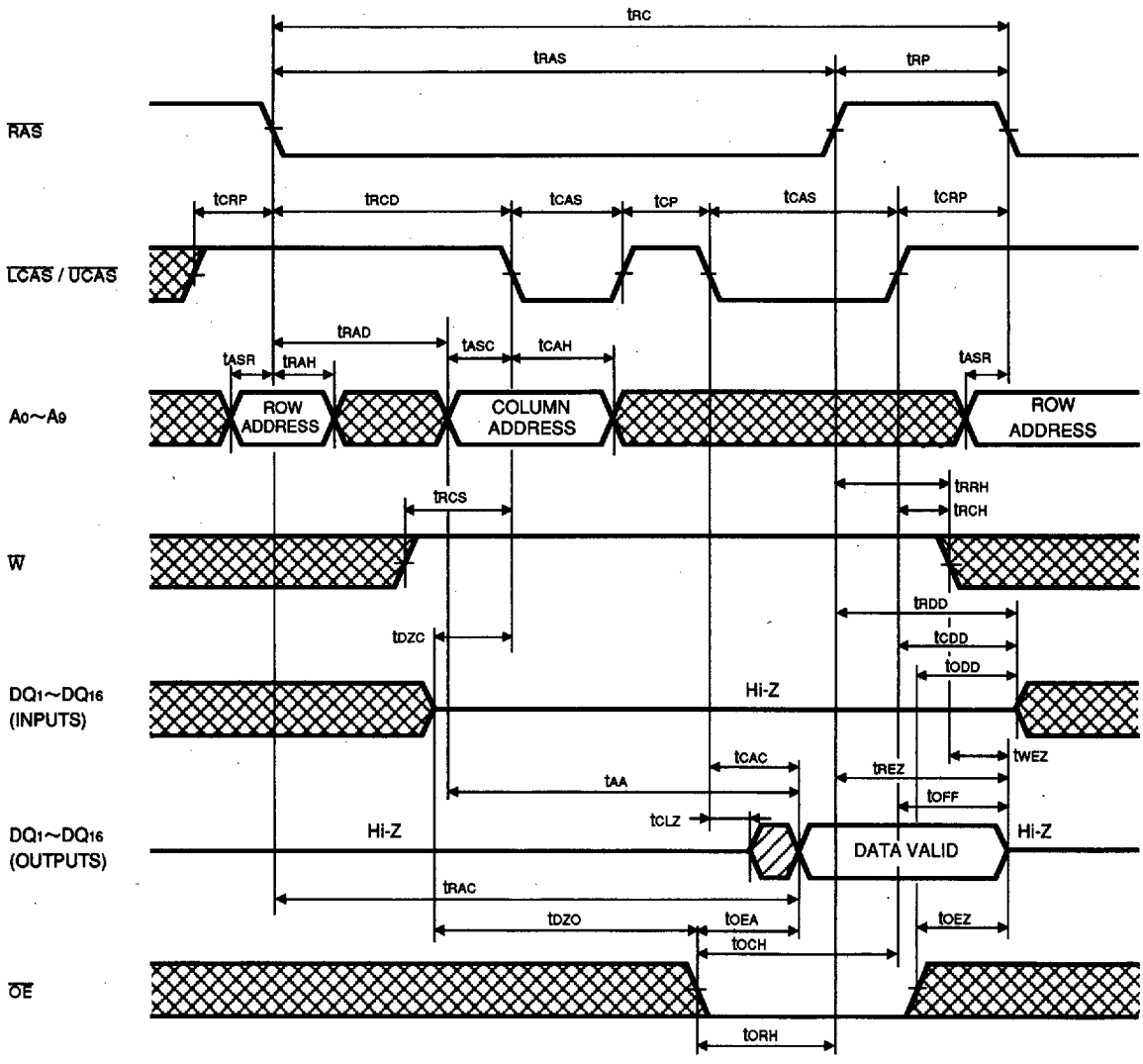
26: tCP(max) is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh, and WCBR Cycle (Note 27)

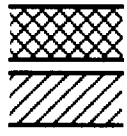
Symbol	Parameter	Limits						Unit
		M5M4V18167C-5,-5S		M5M4V18167C-6,-6S		M5M4V18167C-7,-7S		
		Min	Max	Min	Max	Min	Max	
tCSR	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		10		ns
tCHR	$\overline{CAS}$ hold time after $\overline{RAS}$ low	15		15		15		ns
tWRP	$\overline{WE}$ setup time before $\overline{RAS}$ low	10		10		10		ns
tWRH	$\overline{WE}$ hold time after $\overline{RAS}$ low	10		10		10		ns

Note 27: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Timing Diagrams (Note 28)
Read Cycle



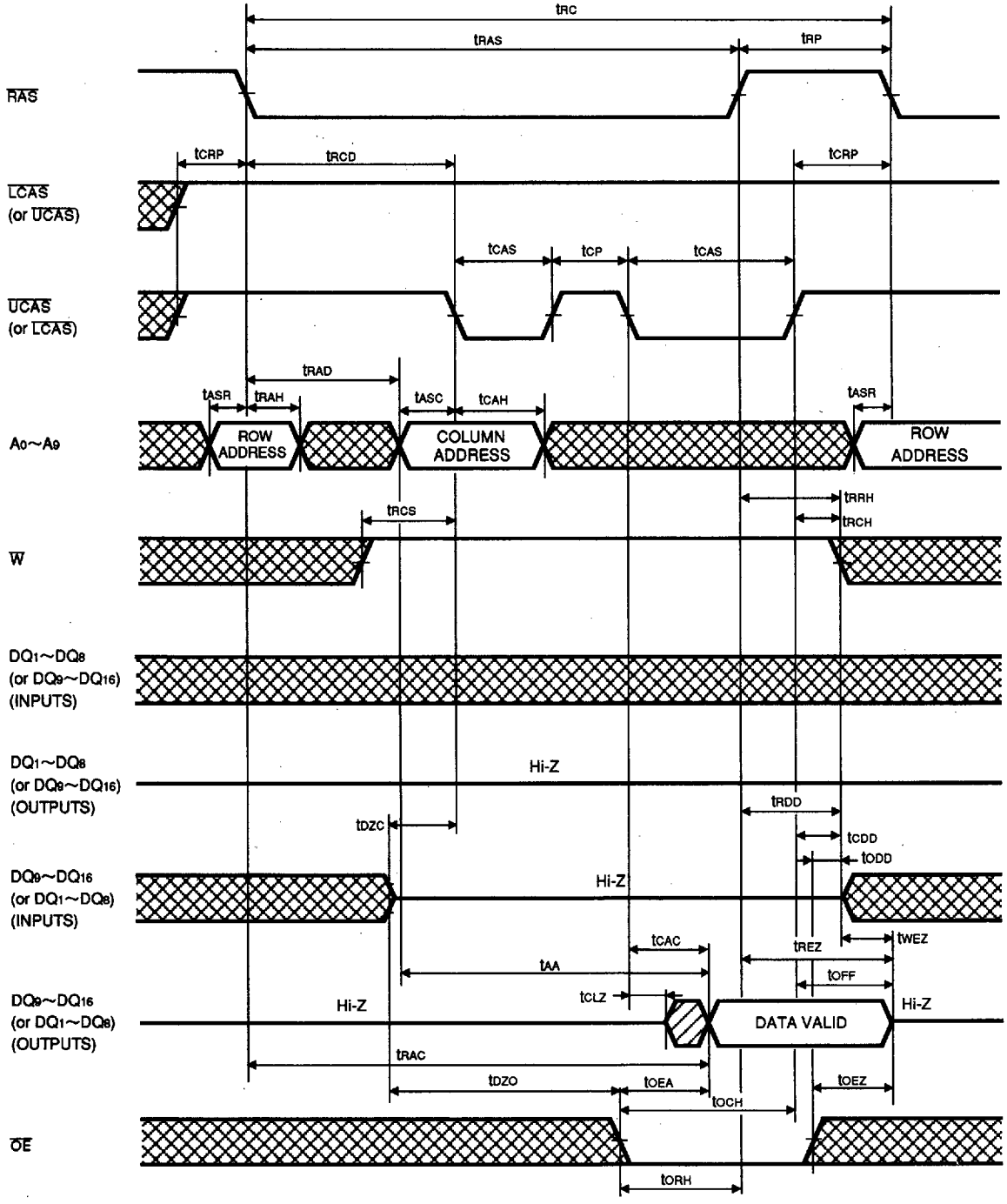
Note 28



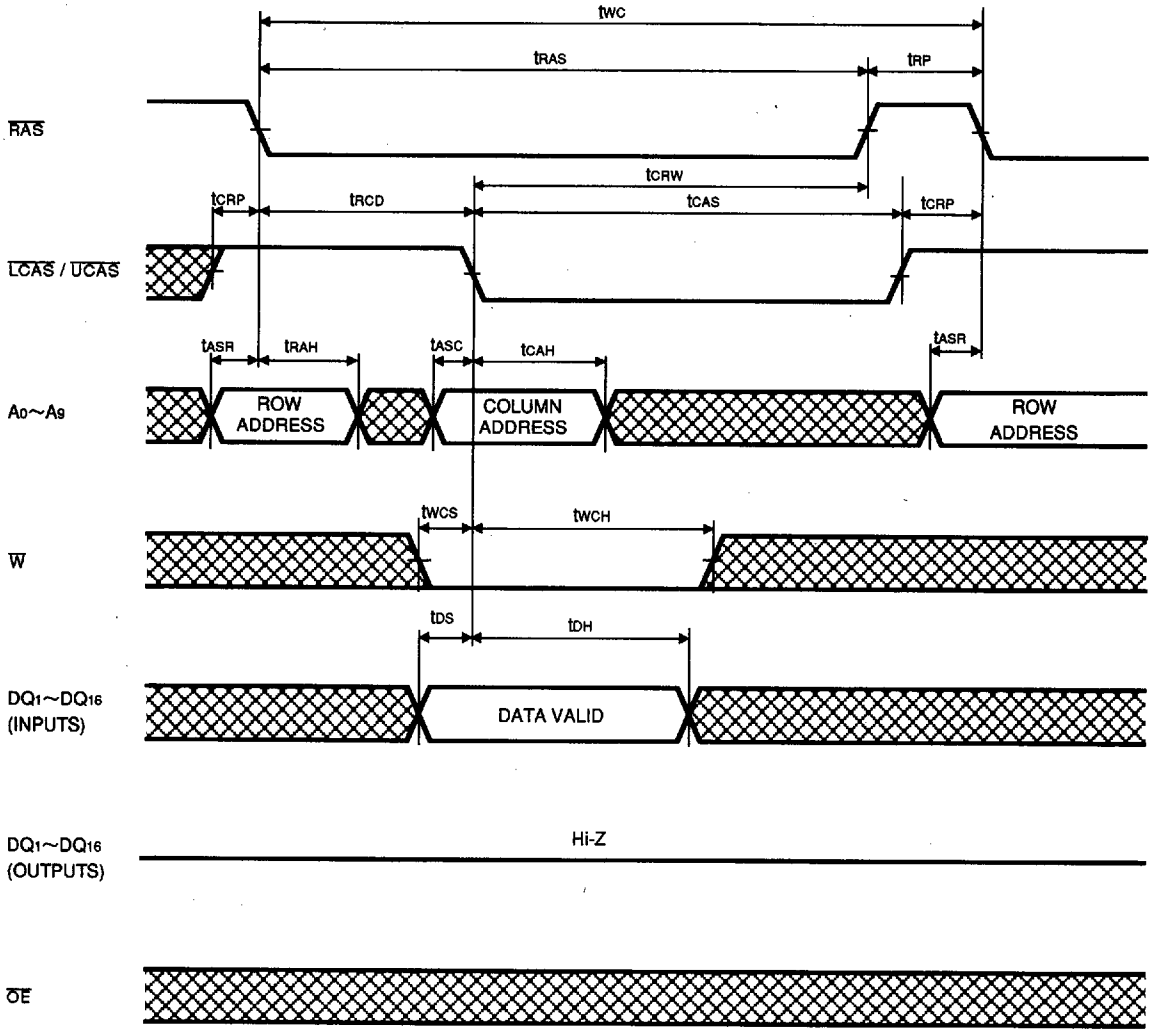
Indicates the don't care input.

Indicates the invalid output.

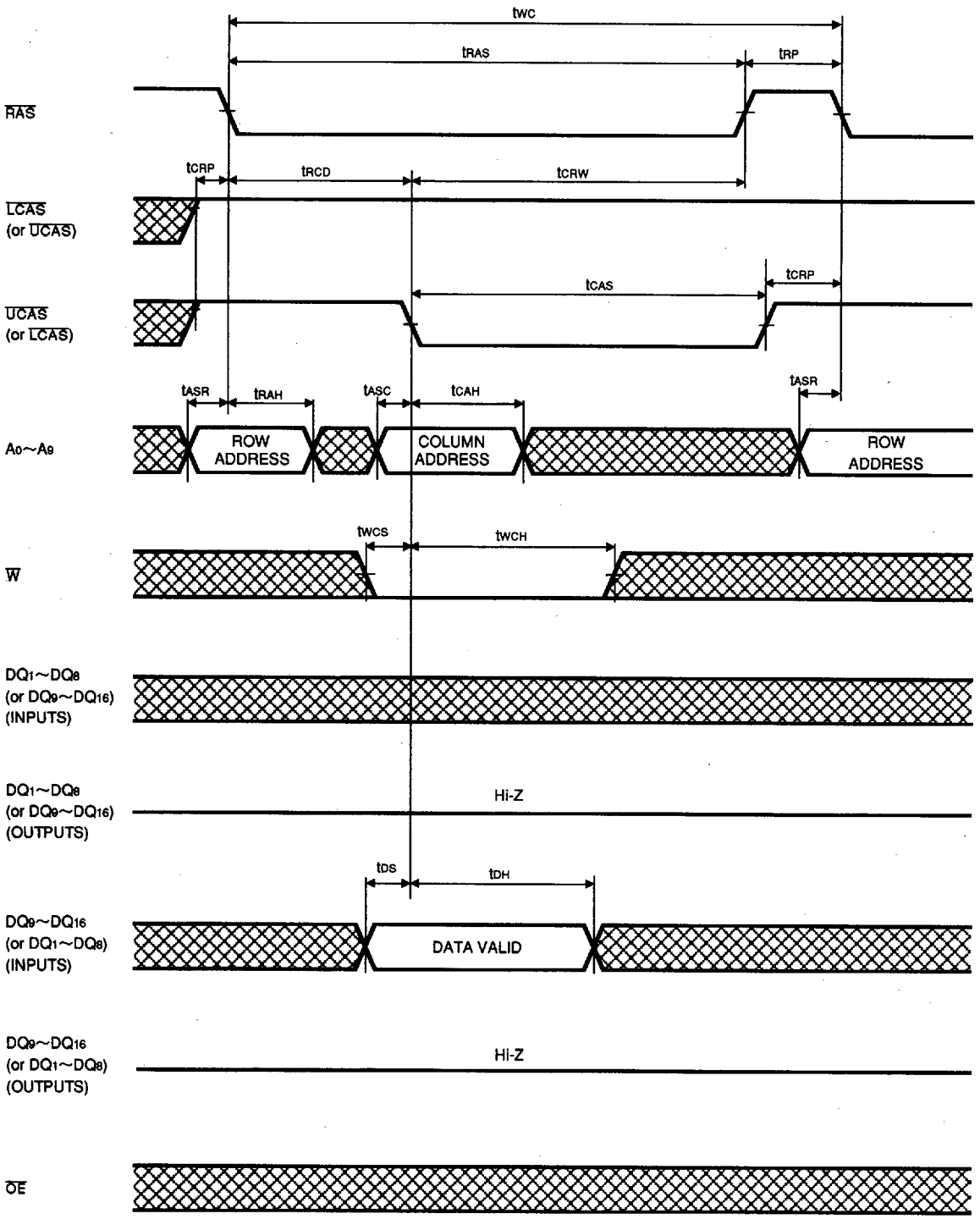
Byte Read Cycle



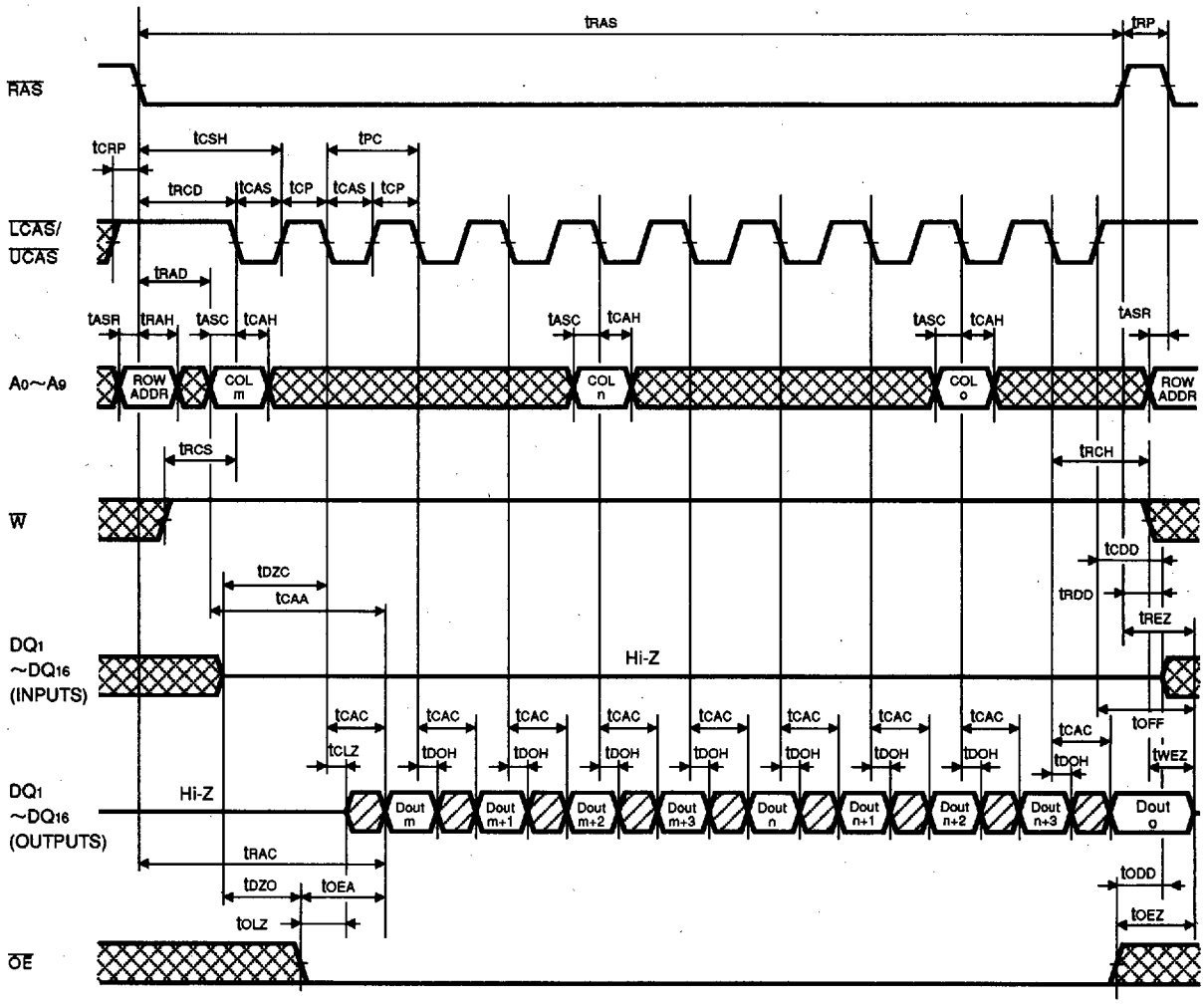
Write Cycle


tWC
tRAS
tRP
RAS
tCRW
tCRP
tRCD
tCAS
tCRP
LCAS / UCAS
tASR
tRAH
tASC
tCAH
tASR
A0~A9
ROW ADDRESS
COLUMN ADDRESS
ROW ADDRESS
tWCS
tWCH
W
tDS
tDH
DQ1~DQ16 (INPUTS)
DATA VALID
DQ1~DQ16 (OUTPUTS)
Hi-Z
OE

Byte Write Cycle

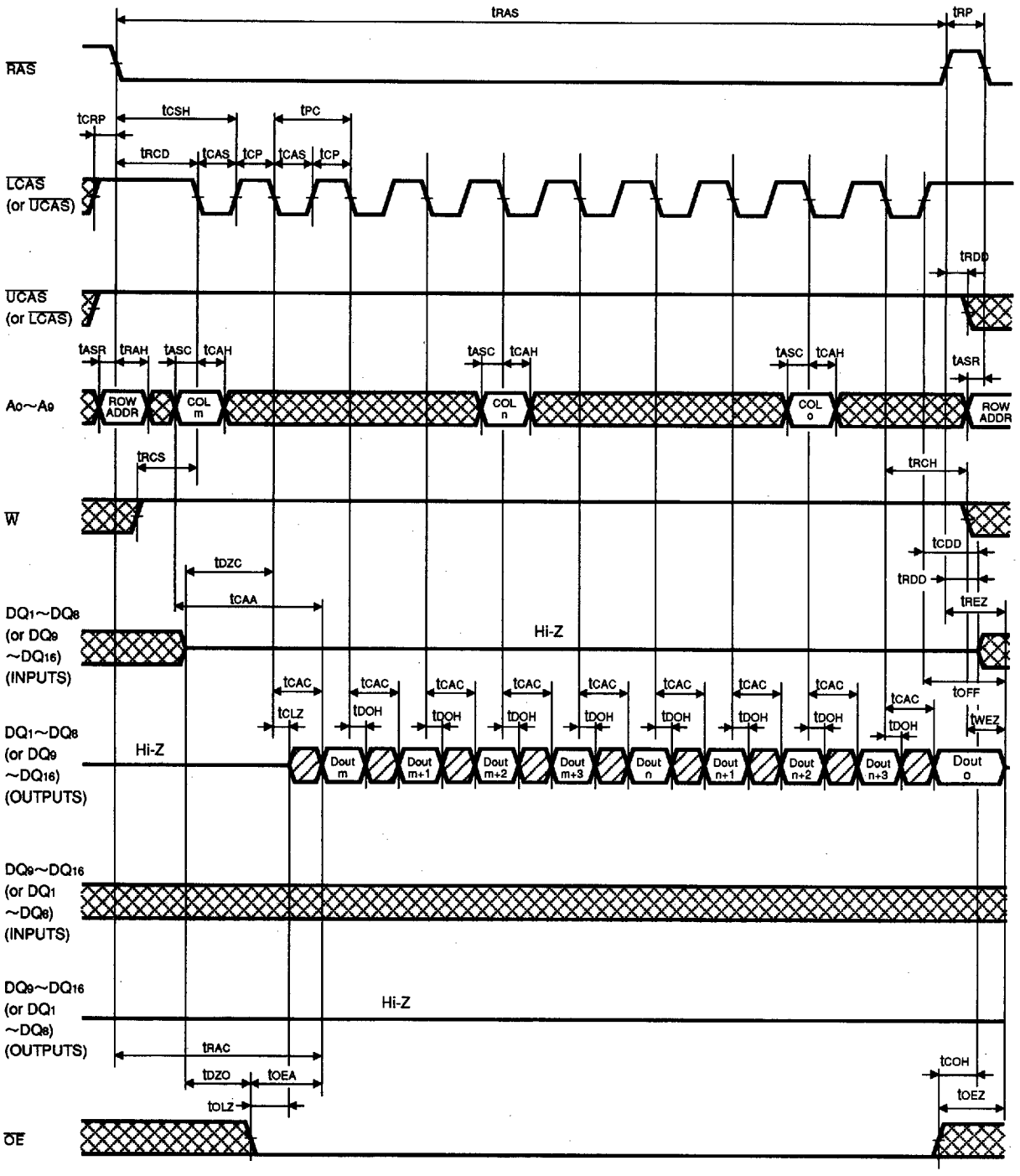


Pipeline Burst Mode Read Cycle (1)

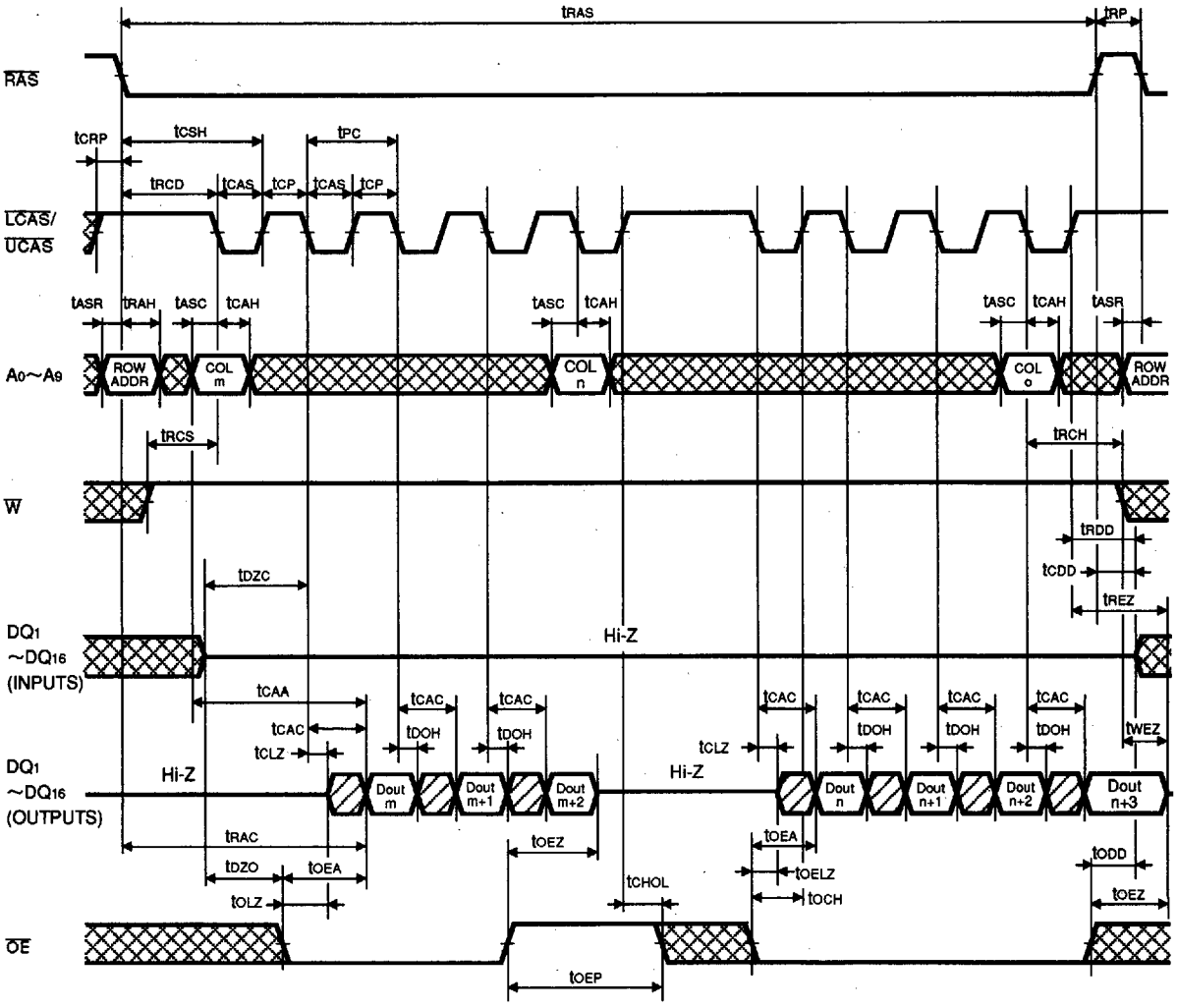


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Pipeline Burst Mode Byte Read Cycle (1)

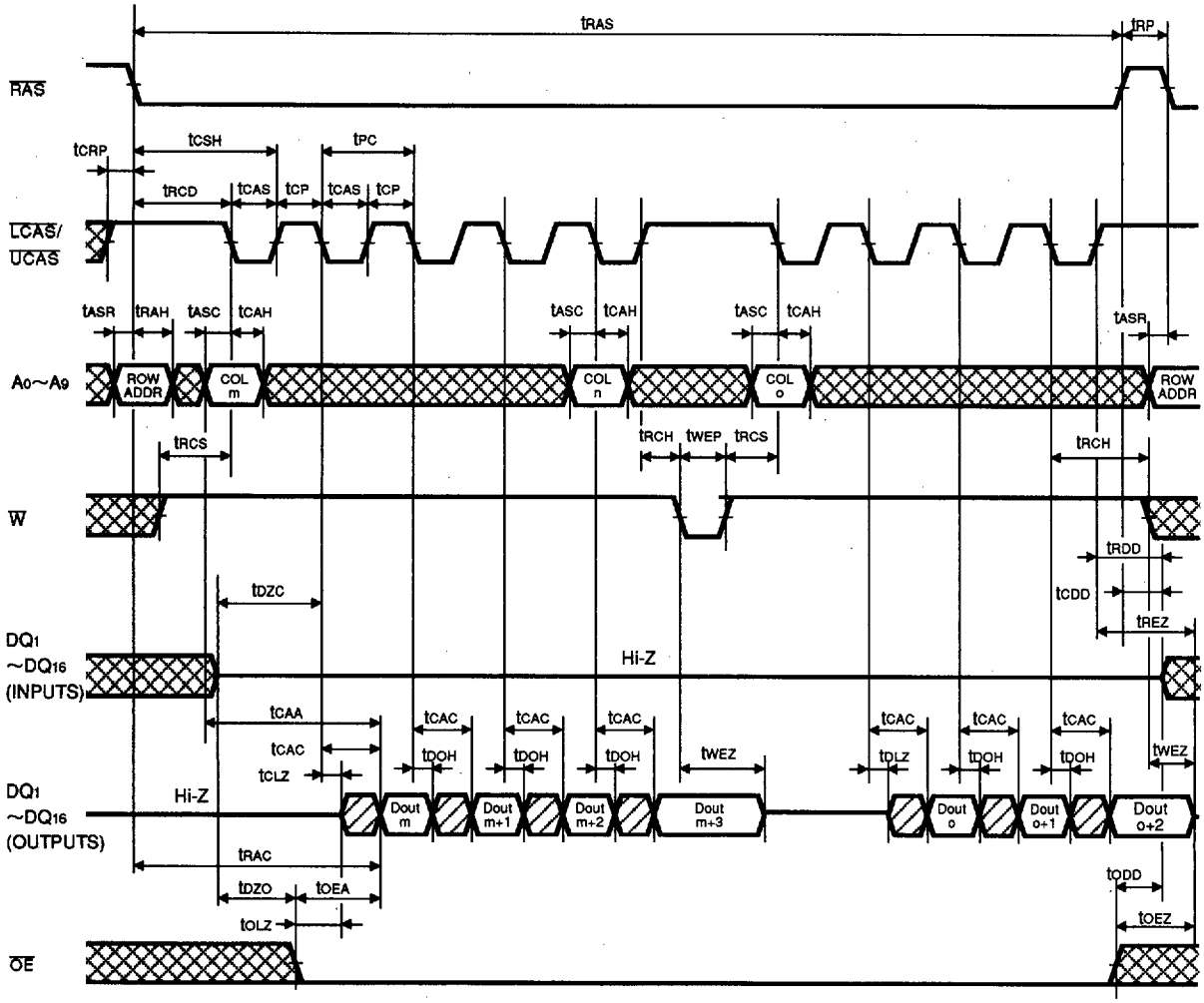


Pipeline Burst Mode Read Cycle (2)

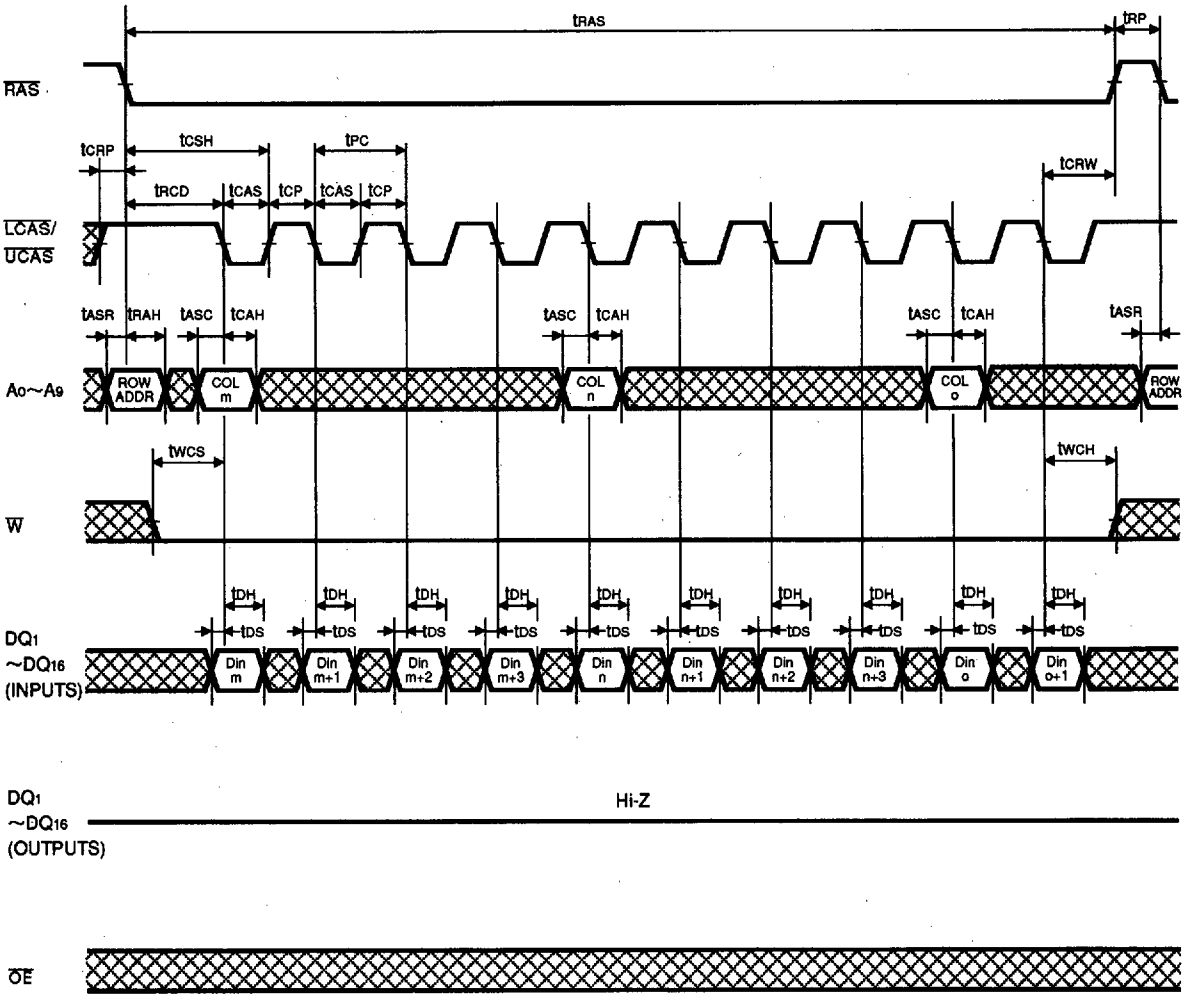


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change

Pipeline Burst Mode Read Cycle (Read Terminated Read)

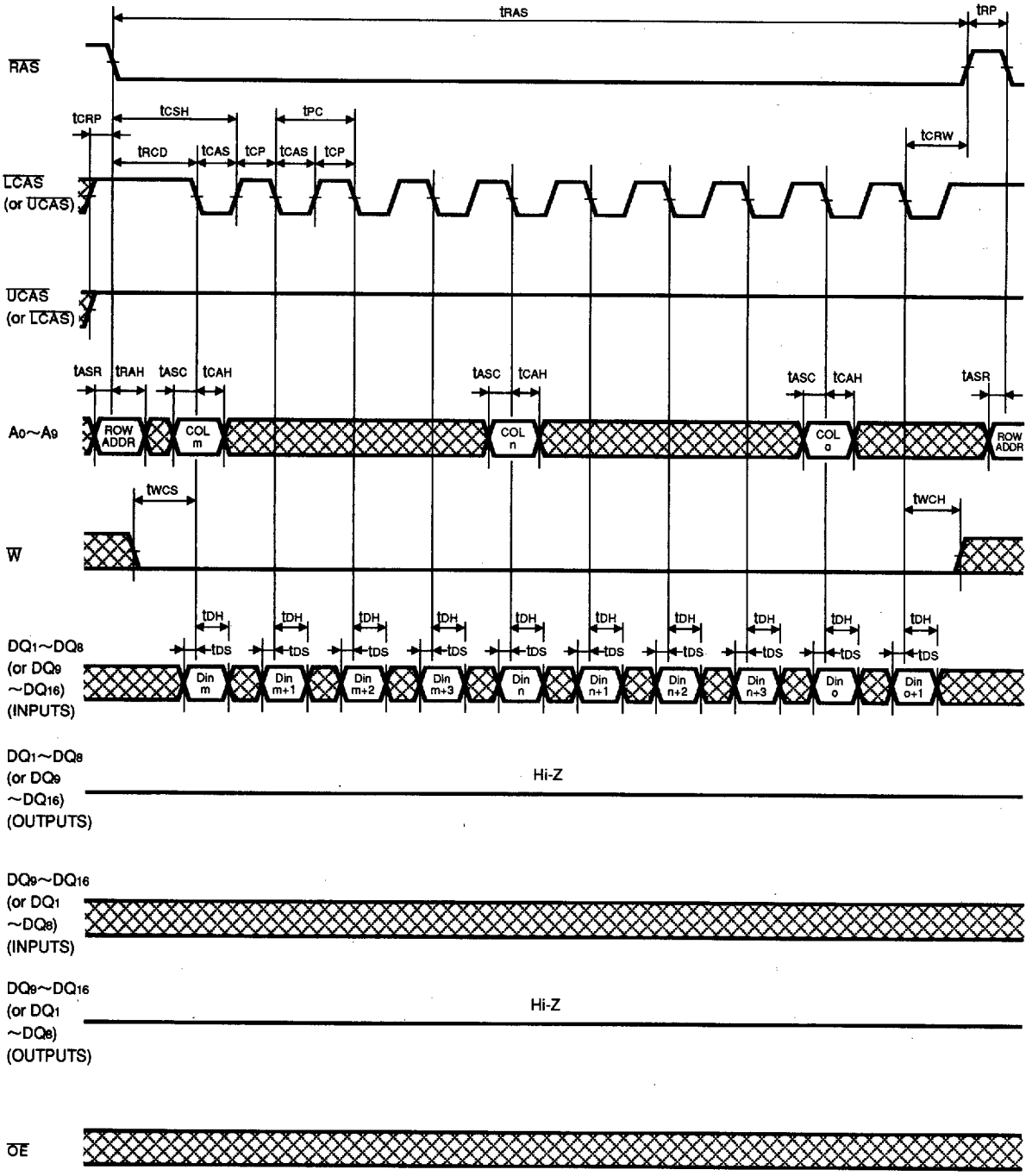


Pipeline Burst Mode Write Cycle

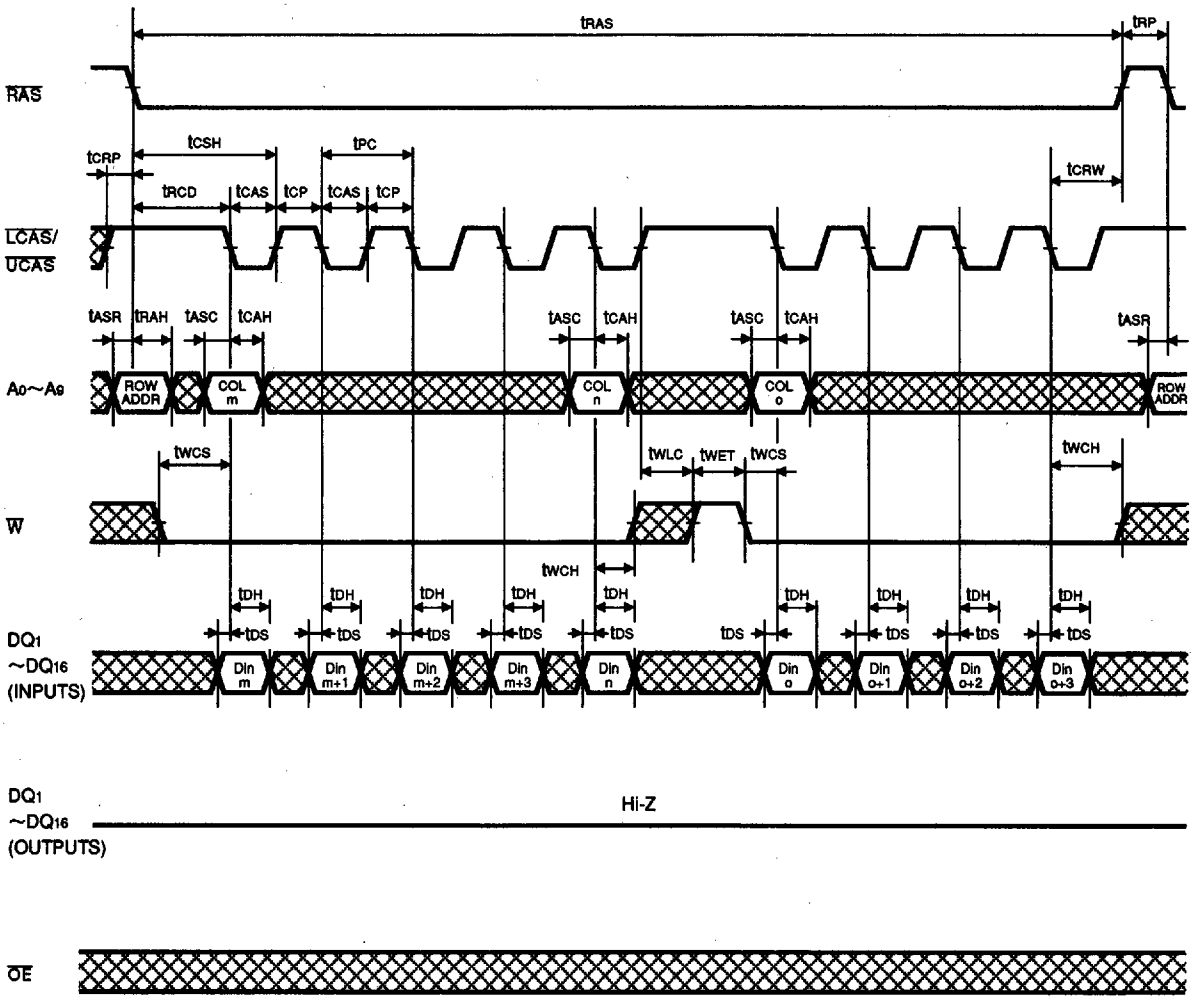


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change

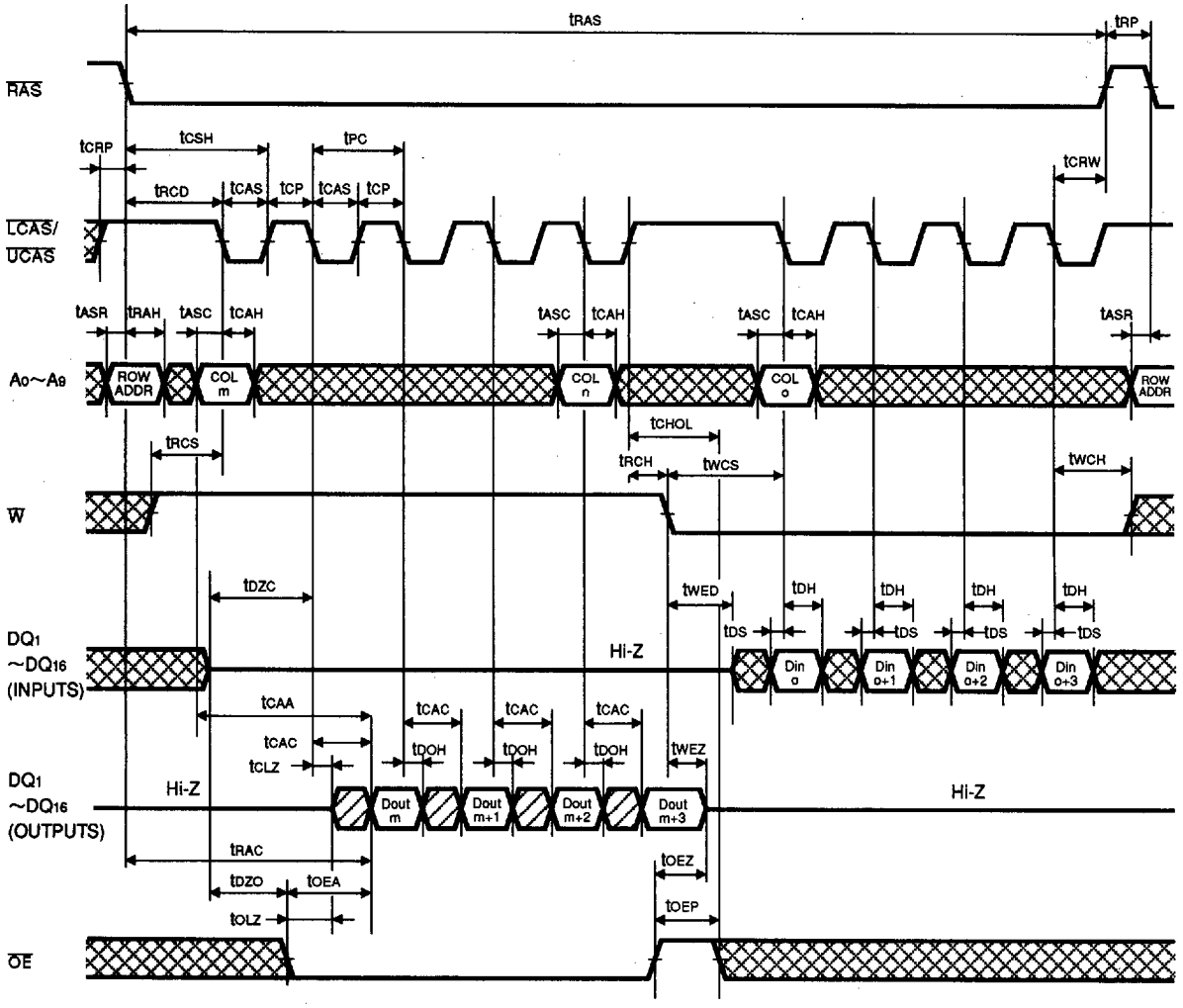
Pipeline Burst Mode Byte Write Cycle



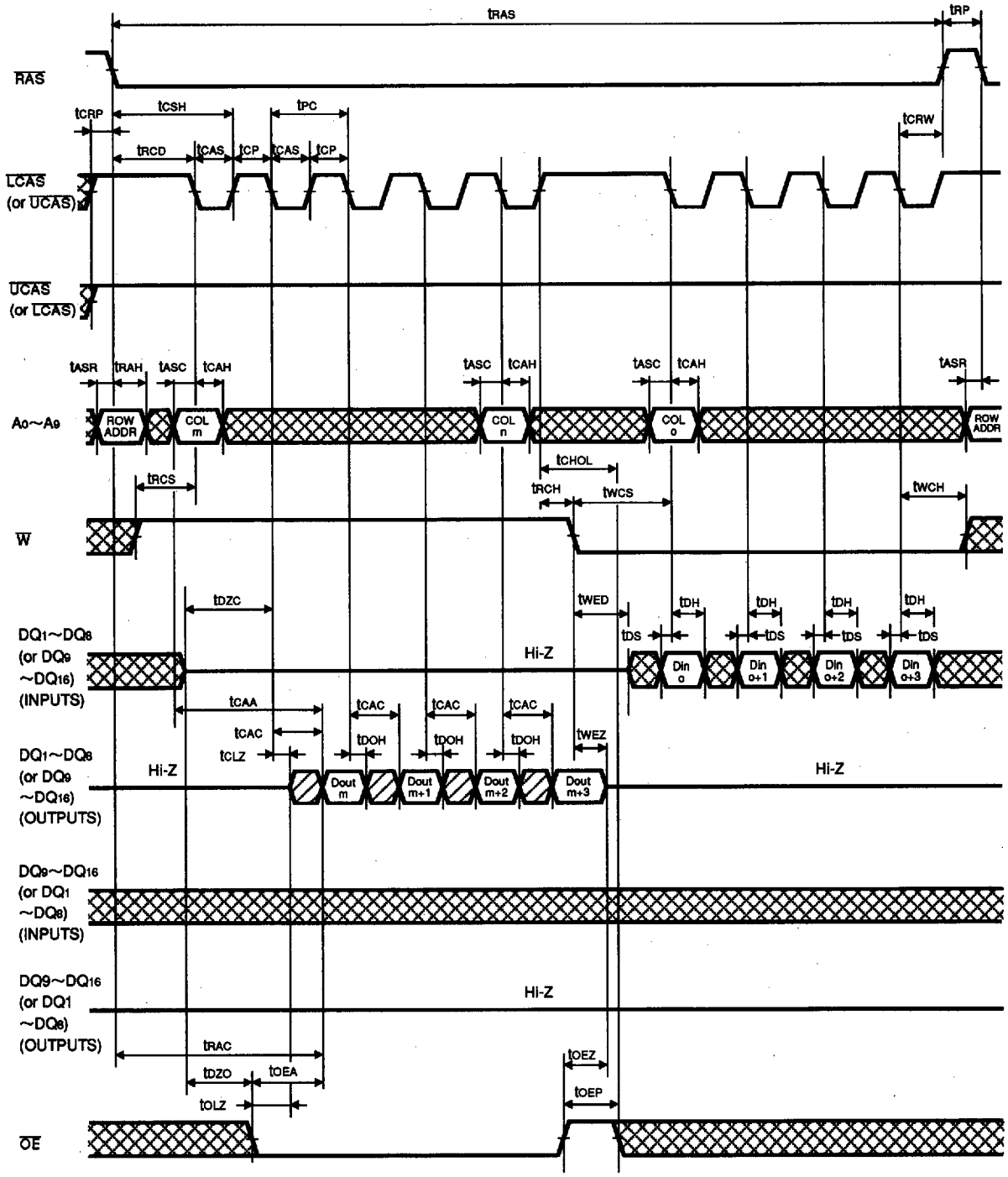
Pipeline Burst Mode Write Cycle (Write terminated Write)



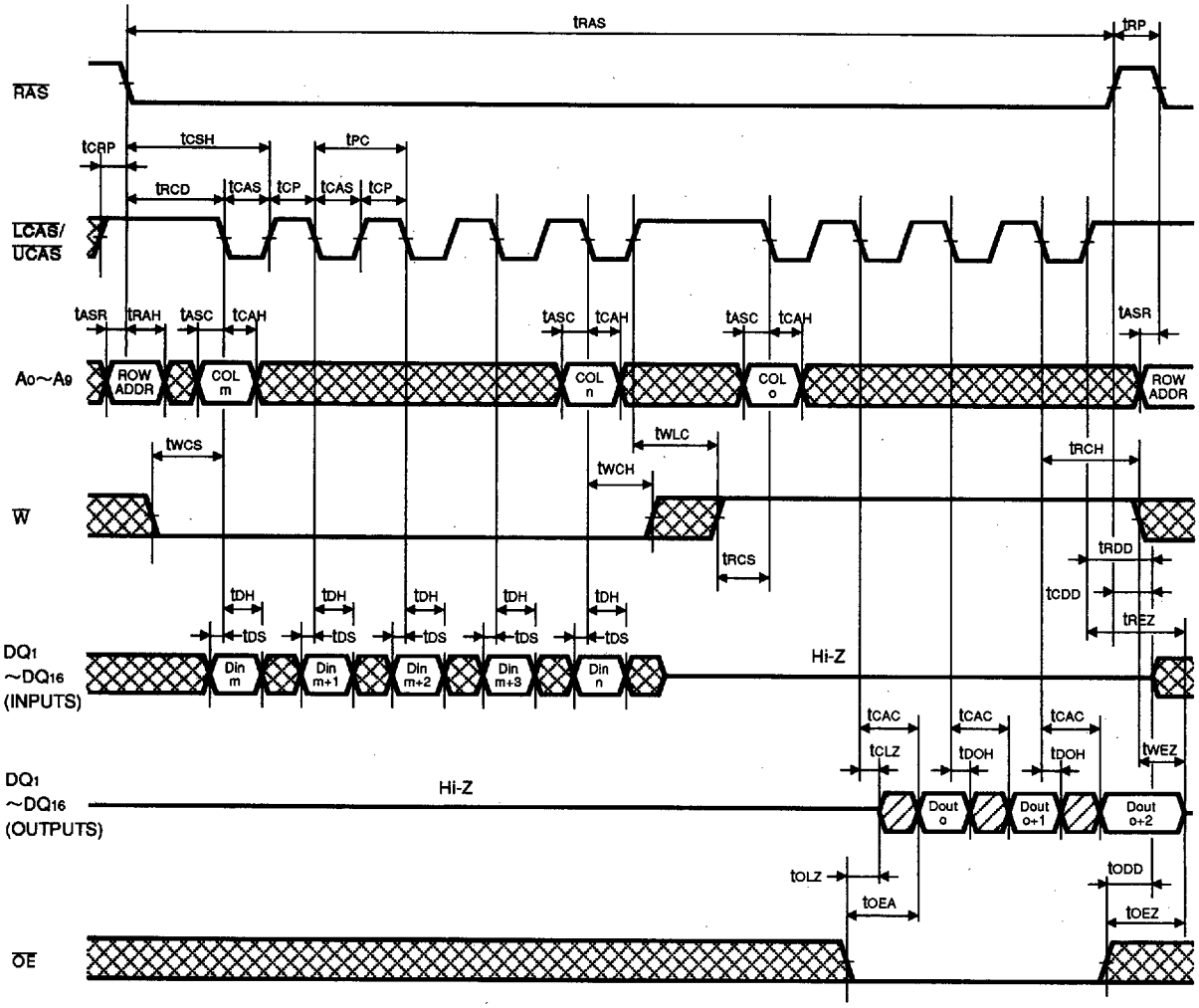
Pipeline Burst Mode Read-Write Cycle



Pipeline Burst Mode Byte Read-Write Cycle

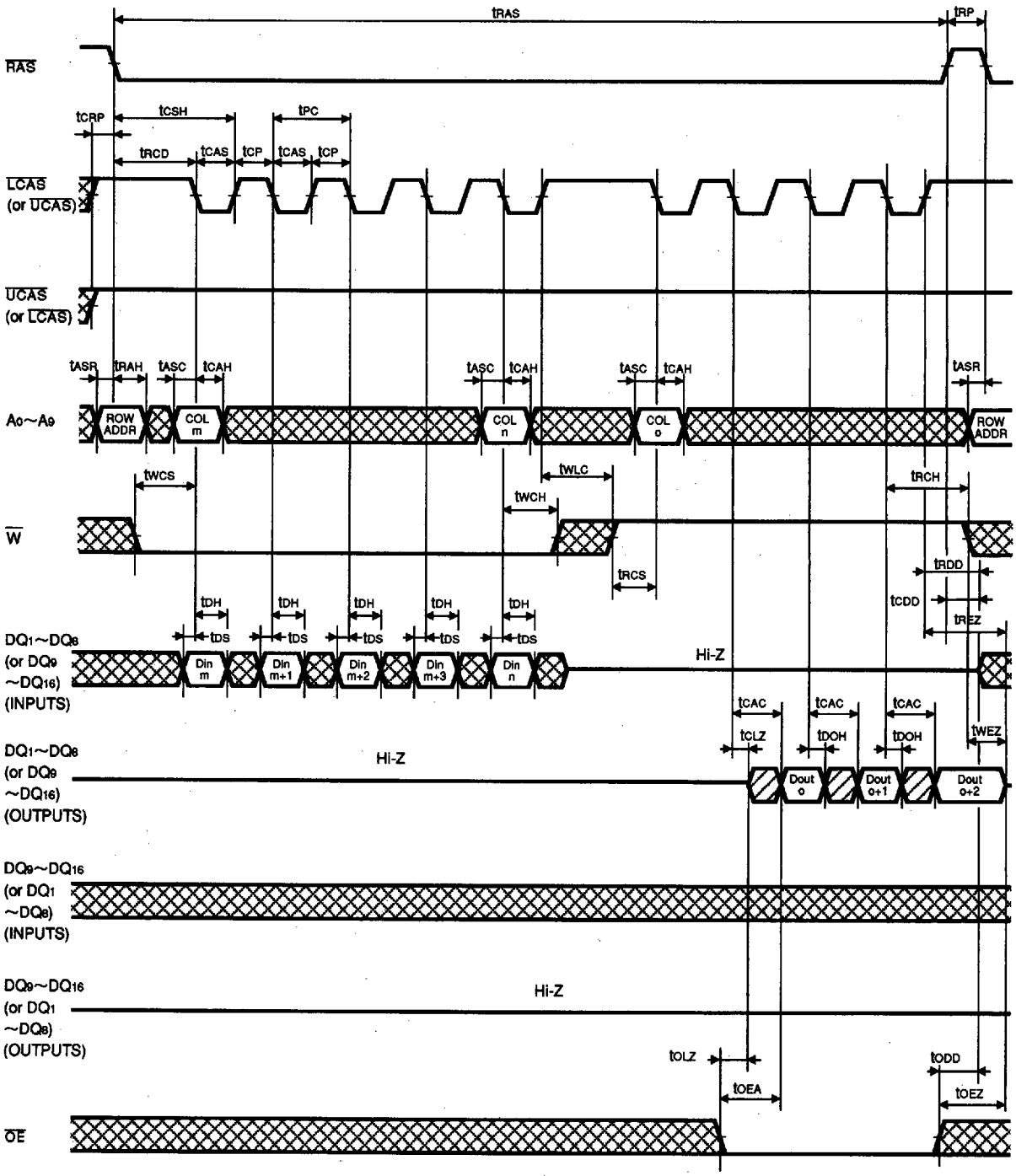


Pipeline Burst Mode Write-Read Cycle



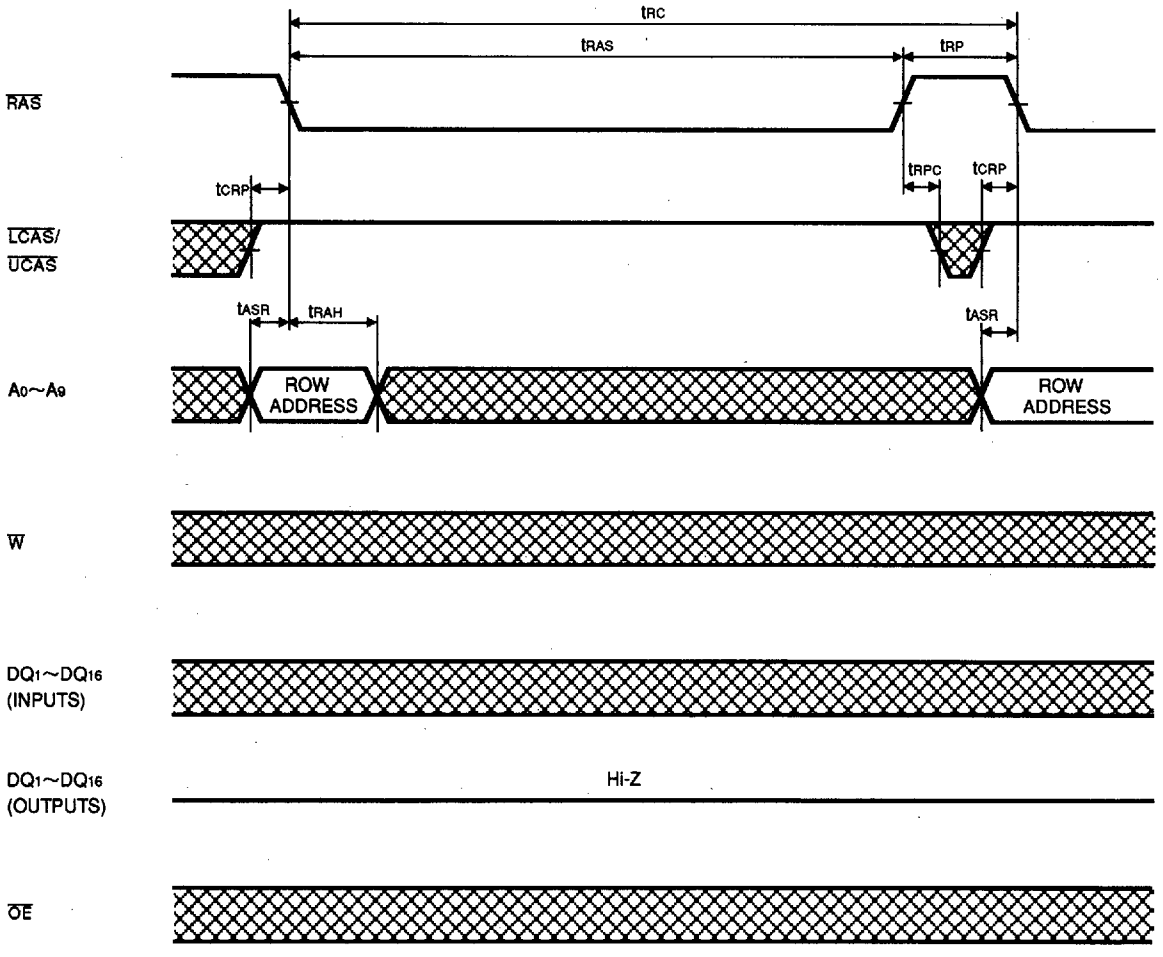
PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Pipeline Burst Mode Byte Write-Read Cycle

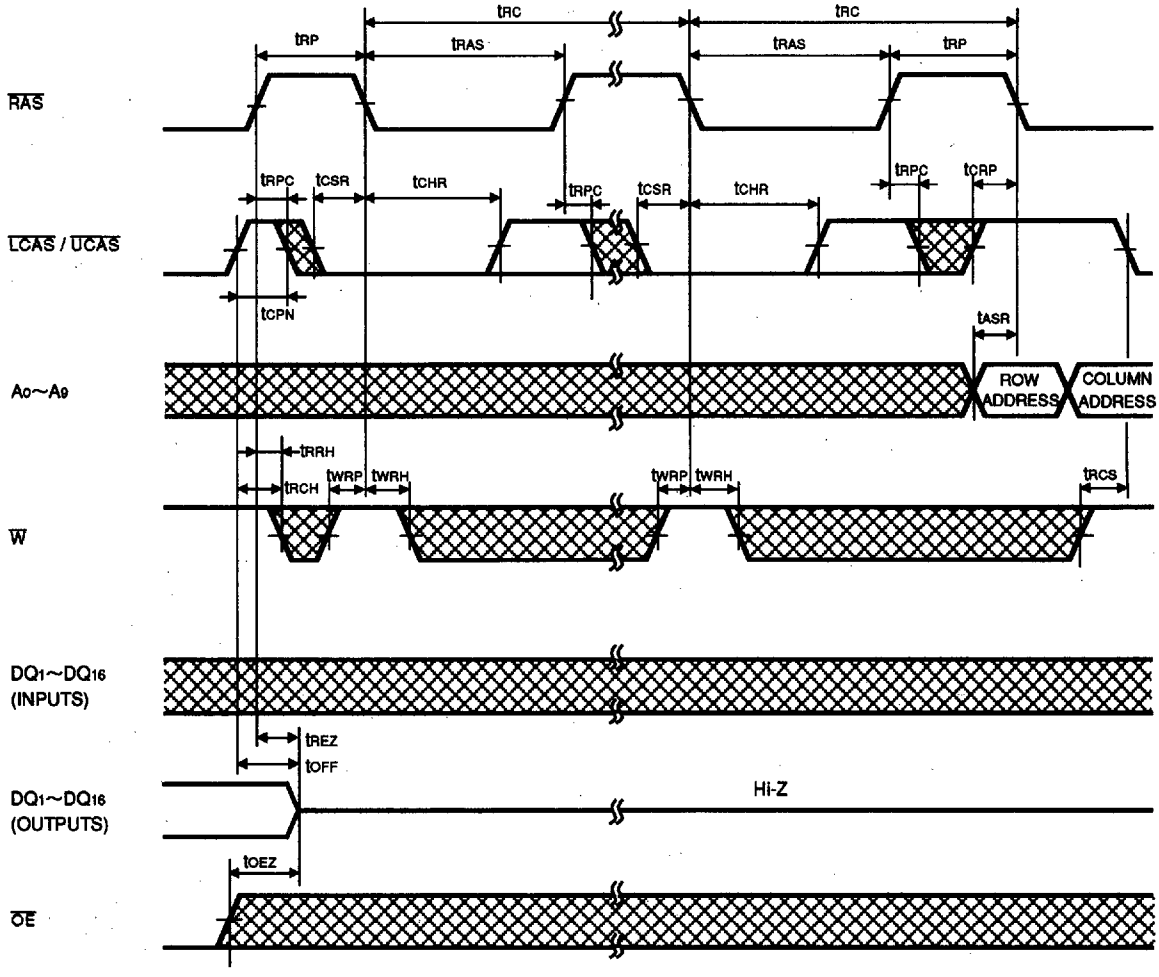


PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

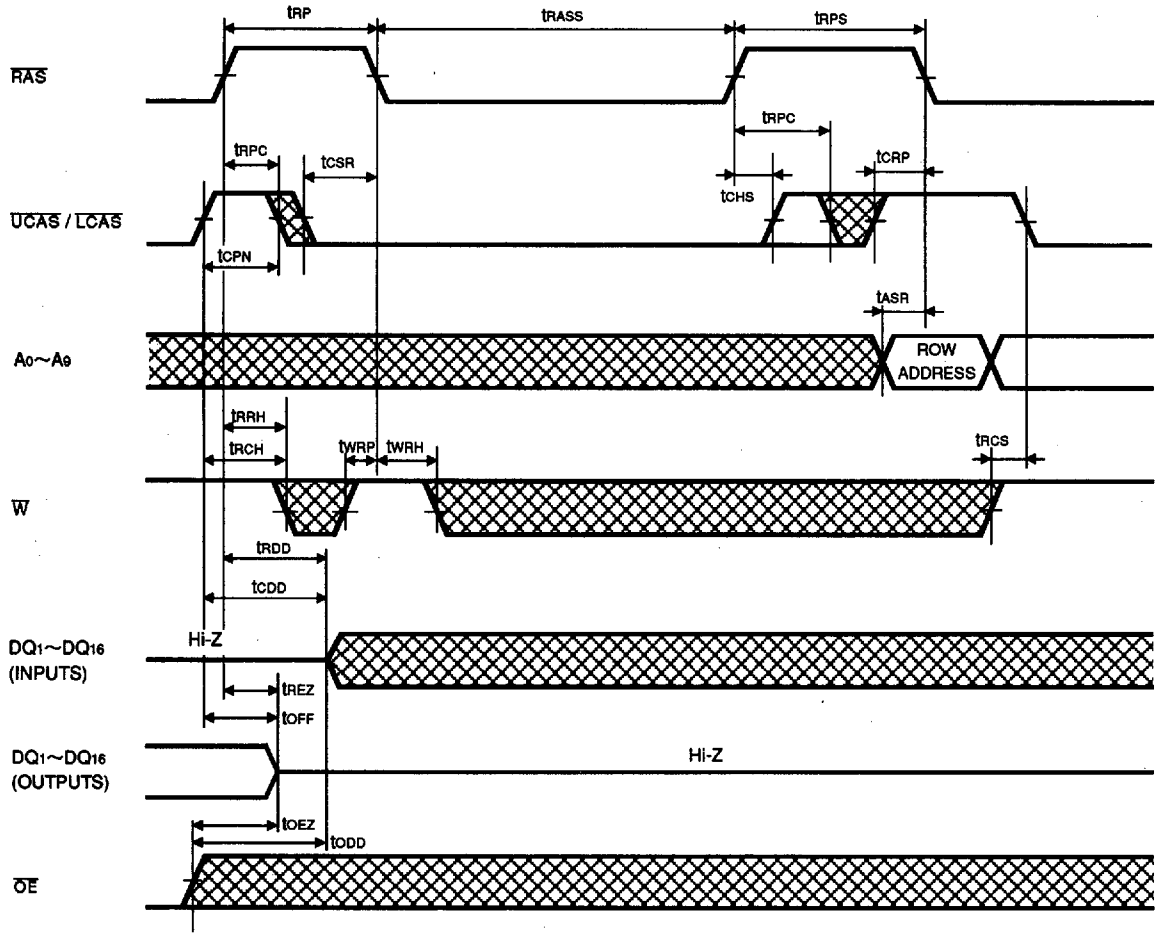
$\overline{RAS}$-only Refresh Cycle



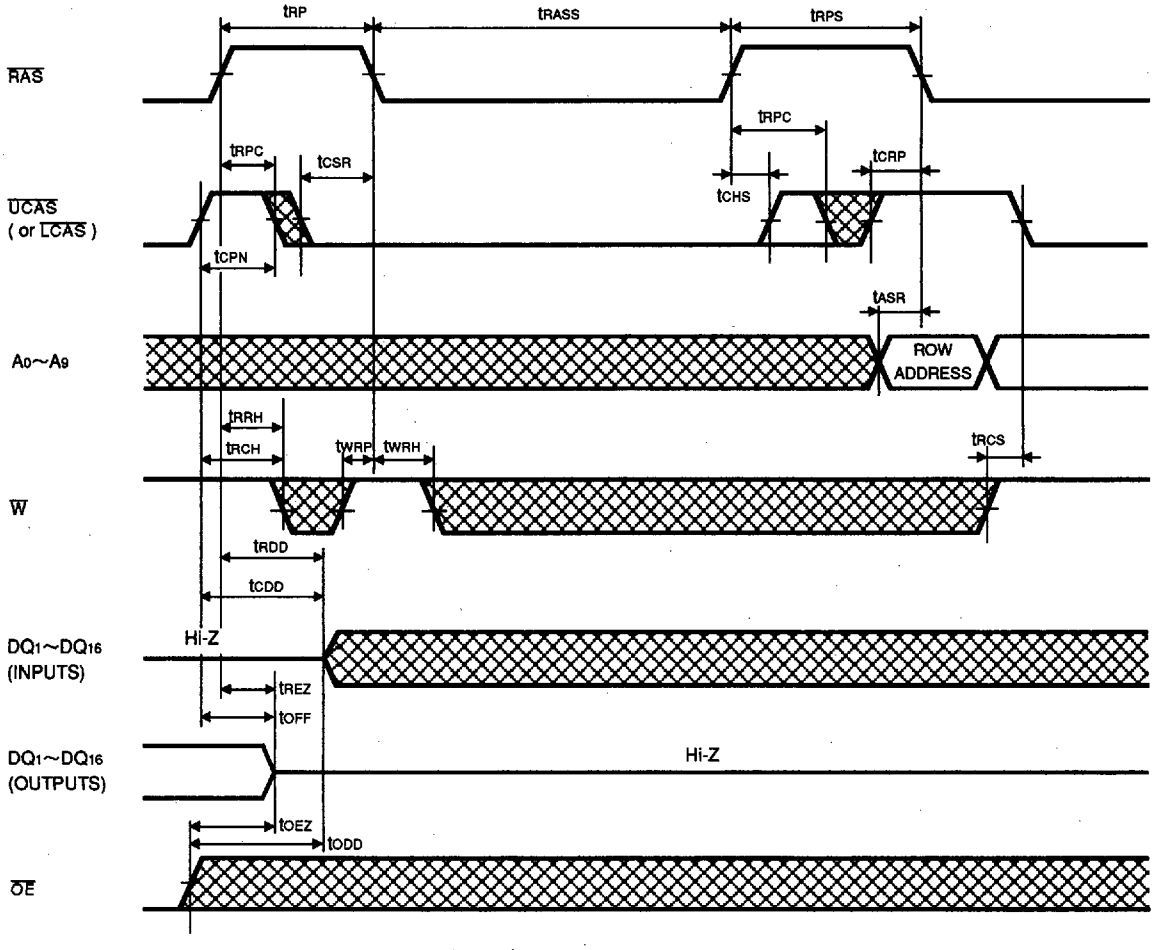
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle, Extended Refresh Cycle *



Self Refresh Cycle*



Upper/(Lower) Self Refresh Cycle*



SELF REFRESH SPECIFICATIONS *

Self refresh devices are denoted by "S" after speed item, like -5S / -6S / -7S. The other characteristics and requirements than the below are same as normal devices.

TIMING REQUIREMENTS (Ta=0~70℃, Vcc=3.15V~3.6V, Vss=0V, unless otherwise noted See notes 13,14)

Symbol	Parameter	Limits						Unit
		M5M4V18167C-5S		M5M4V18167C-6S		M5M4V18167C-7S		
		Min	Max	Min	Max	Min	Max	
t_{RASS}	Self Refresh $\overline{RAS}$ low pulse width	100		100		100		μs
t_{RPS}	Self Refresh $\overline{RAS}$ high precharge time	90		110		130		ns
t_{CHS}	Self Refresh $\overline{RAS}$ hold time	−50		−50		−50		ns

SELF REFRESH ENTRY & EXIT CONDITIONS

(1) In case of distributed refresh

The last / first full refresh cycles (1K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of $t_{NS} \leqq 16.4$ ms and $t_{SN} \leqq 16.4$ ms.

(2) In case of burst refresh

The last / first full refresh cycles (1K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of $t_{NS} + t_{SN} \leqq 16.4$ ms.