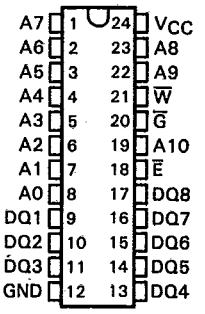
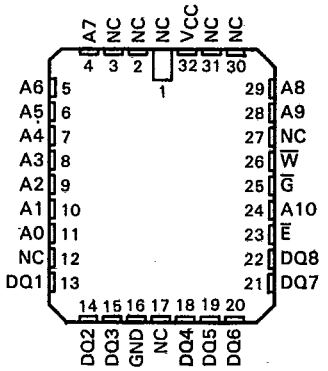
T-46-23-12

- 2048 × 8 Organization
- Common I/O
- Military Temperature Range . . . −55°C to 125°C (M Suffix)
- Fast Static Operation
- Battery Back-Up Operation . . . 2-Volt Data Retention
- Maximum Access Time from Address or Chip Enable
  '68CE16-25 . . . 25 ns
  '68CE16-35 . . . 35 ns
  '68CE16-45 . . . 45 ns
- Single 5-V Supply (10% Tolerance)
- Complementary Silicon Gate MOS Technology with a 6-Transistor Memory Cell
- Automatic Powerdown When Deselected
- TTL Compatible Inputs and Outputs
- 3-State Output
- Low Power Dissipation (V_{CC} = 5.5 V)
  — Active . . . 660 mW MAX
  — Standby . . . 110 mW MAX (TTL Inputs)
  — Standby . . . 5.5 mW MAX (CMOS Inputs)
- Standard and Class B Processing
  — SM Prefix . . . Standard Processing
  — SMJ Prefix . . . Class B Processing
- Output Enable for Bus Control
- Packaging Options:
  — 24-Pin Ceramic 300-mil DIP
  — 32-Pad Leadless Ceramic Chip Carrier

JD PACKAGE
(TOP VIEW)



FG PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A10	Address Inputs
DQ1-DQ8	Data Input/Data Out
$\overline{E}$	Chip Enable/Power Down
$\overline{G}$	Output Enable
GND	Ground
NC	No Connection
V_{CC}	5-V Supply
$\overline{W}$	Write Enable

description

The '68CE16 is a common I/O, 16,384-bit static random-access memory organized as 2048 words by 8 bits. This memory is fabricated using complementary MOS technology utilizing a full CMOS (six transistor cell) memory array.

The '68CE16's static design and control signals ($\overline{E}$, $\overline{G}$, and $\overline{W}$) remove the need for refresh circuitry and simplify timing requirements. The chip-enable pin allows for easy memory expansion and automatic power-down. This feature, in conjunction with the full CMOS array, allows for low standby power operation when the memory is deselected, greatly reducing the overall memory power requirements. The output-enable pin minimizes bus contention problems and adds flexibility.

Access time from either address or chip enable is a maximum of 25, 35, or 45 ns, allowing speed upgrades for new and existing designs.

operation

addresses (A0-A10)

The 11 address inputs select one of the 2048 8-bit words in the RAM. The address inputs must be stable for the duration of a read or write cycle. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors.

chip enable/power down ($\overline{E}$)

The chip enable/power down terminal, which can be driven directly by standard TTL circuits, affects the data-in and data-out terminals and the internal functioning of the chip itself. Whenever the chip enable/power down is low (enabled), the device is operational, input and output terminals are enabled, and data can be read or written. When the chip enable/power down terminal is high (disabled), the device is deselected and put into a reduced-power standby mode. Data is retained during standby.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable terminal. A logic high selects the read mode; a logic low selects the write mode. $\overline{W}$ or $\overline{E}$ must be high when changing addresses to prevent inadvertently writing data into a memory location. The $\overline{W}$ input can be driven directly from standard TTL circuits.

output enable ($\overline{G}$)

The output-enable terminal affects only the data-out terminals. When output enable is at a logic high level, the output terminals are disabled to the high-impedance state. Output enable provides greater output control flexibility, simplifying data bus design.

data in/data out (DQ1-DQ8)

Data can be written into a selected device when the write-enable input is low. The DQ terminals can be driven directly from standard TTL circuits. The three-state output buffer provides direct TTL compatibility with a fanout of twenty Series 54LS or 54ALS TTL gates, sixteen Series 54AS TTL gates, or thirteen Series 54F TTL gates. The DQ terminals are in the high-impedance state when chip enable ($\overline{E}$) is high or whenever a write operation is being performed. Data out is the same polarity as data in.

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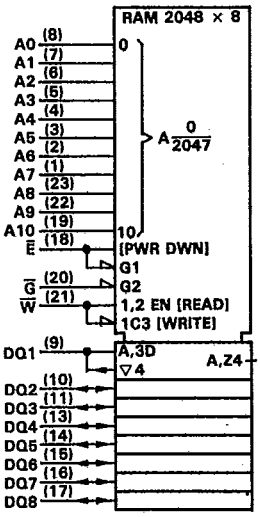
logic symbol†



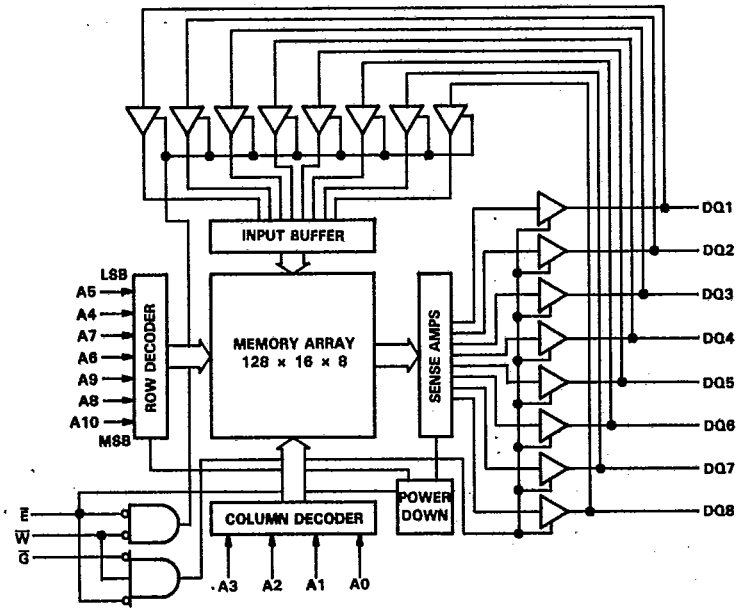
FUNCTION TABLE

INPUTS			OUTPUTS	MODE	POWER
Ē	W̄	Ḡ	DQ1-DQ8		
H	X	X	HI-Z	Standby	Standby
L	H	L	Data Output	Read	Active
L	H	H	HI-Z	Read	Active
L	L	X	Data Input	Write	Active

X = Don't Care.

†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the JD package.

functional block diagram



8

Military Products

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range (see Note 1) . . . . . −0.5 V to 7 V
Input voltage range (see Note 2) . . . . . −1 V to 7 V
Output voltage range in high-impedance state . . . . . −0.5 V to 7 V
Output current . . . . . 20 mA
Minimum operating free-air temperature . . . . . −55°C
Maximum operating case-temperature . . . . . 125°C
Storage temperature range . . . . . −65°C to 150°C
Latch-up current . . . . . 200 mA

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values in this data sheet are with respect to GND.
2. V_{IL} (min) of −3 V for short pulse durations. Prolonged operation at V_{IL} levels below −1 V will result in excessive currents that may damage the device.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.2		$V_{CC}+1$	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_C	Operating case temperature			125	°C
T_A	Operating free-air temperature	−55			°C

NOTE 2: V_{IL} (min) of −3 V for short pulse durations. Prolonged operation at V_{IL} levels below −1 V will result in excessive currents that may damage the device.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	'68CE16-25			'68CE16-35			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	High-level output voltage		V_{CC} = 4.5 V, I_{OH} = −4 mA	2.4			2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V, I_{OL} = 8 mA			0.4			0.4	V
I_I	Input current (load)		0 V ≤ V_I ≤ V_{CC}	−10		10	−10		10	µA
I_O	Output current (leakage)		0 V ≤ V_O ≤ V_{CC}, Output disabled	−10		10	−10		10	µA
I_{CC}	V_{CC} operating supply current		V_{CC} = 5.5 V, I_O = 0 mA			120			120	mA
I_{CCI}	V_{CC} supply current (standby)	TTL-level inputs	$\overline{E}$ ≥ V_{IH}, V_{CC} = 5.5 V			20			20	mA
		CMOS-level inputs	$\overline{E}$ = V_{CC}±0.3, V_{CC} = 5.5 V			0.9			0.9	mA

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electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

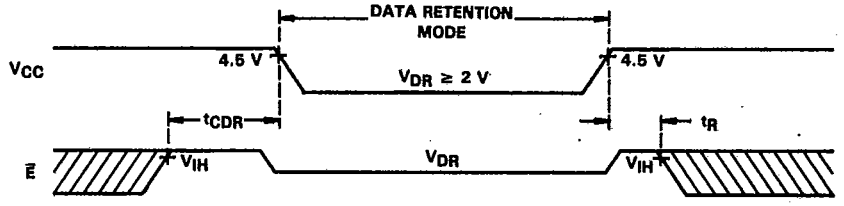
PARAMETER			TEST CONDITIONS	'68CE16-45 MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		V_{CC} = 4.5 V, I_{OH} = −4 mA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V, I_{OL} = 8 mA			0.4	V
I_I	Input current (load)		0 V ≤ V_I ≤ V_{CC}	−10		10	µA
I_O	Output current (leakage)		0 V ≤ V_O ≤ V_{CC}, Output disabled	−10		10	µA
I_{CC}	V_{CC} operating supply current		V_{CC} = 5.5 V, I_O = 0 mA			120	mA
I_{CCI}	V_{CC} supply current (standby)	TTL-level inputs	$\overline{E}$ ≥ V_{IH}, V_{CC} = 5.5 V			20	mA
		CMOS-level inputs	$\overline{E}$ = V_{CC} ± 0.3, V_{CC} = 5.5 V			0.9	mA

data retention characteristics

PARAMETER		TEST CONDITION	MIN	TYP† V_{CC} @ 2.0 V	TYP† V_{CC} @ 3.0 V	MAX V_{CC} @ 2.0 V	MAX V_{CC} @ 3.0 V	UNIT
V_{DR}	V_{CC} for data retention	$\overline{E}$ ≥ V_{CC} − 0.2 V, V_{IN} ≥ V_{CC} − 0.2 V or ≤ GND + 0.2 V	2.0	—	—	—	—	V
I_{CCDR}	Data retention current			3	5	100	200	µA
t_{CDR}§	Chip deselect to data retention time		0	—		—		ns
t_R§	Operation recovery time		$t_{c(RD)}$‡	—		—		ns
I_{LI}§	Input leakage current			—		1		µA

†TYP values listed are typical values at 25°C.
‡$t_{c(RD)}$ = read cycle time.
§This parameter is guaranteed but not tested.

data retention waveform



capacitance, T_A = 25°C, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_i	Input capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5 V			5	pF
C_o	Output capacitance				7	pF

†Capacitance measurements are made on sample basis only.

timing requirements over recommended supply voltage range and operating temperature range

		'68CE16-25			'68CE16-35			'68CE16-45			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$t_{c(rd)}$	Read cycle time	25			35			45			ns
$t_{c(wr)}$	Write cycle time	25			35			45			ns
$t_{w(W)}$	Write-enable pulse duration	20			30			30			ns
$t_{su(E)}$	Chip-enable low to end of write	20			30			40			ns
$t_{su(A)}$	Address setup time to write start	0			0			0			ns
$t_{su(D)}$	Data setup time to write end	10			15			20			ns
$t_{h(A)}$	Address hold time from write end	0			0			0			ns
$t_{h(D)}$	Data hold time from write end	0			0			0			ns
t_{PU}	Delay time, chip-enable low to power up‡	5			5			5			ns
t_{PD}	Delay time, chip-enable high to power down‡			35			35			35	ns
t_{AW}	Address setup to write end	20			30			40			ns

‡This parameter is guaranteed but not tested.

switching characteristics over recommended supply voltage range and operating temperature range

PARAMETER		TEST CONDITIONS	'68CE16-25		'68CE16-35		'68CE16-45		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	R1 = 481 Ω, R2 = 255 Ω, C_L = 30 pf, See Figure 1a		25		35		45	ns
$t_{a(E)}$	Access time from chip enable low			25		35		45	ns
$t_{a(G)}$	Output enable low to data valid			15		20		25	ns
$t_{v(A)}$	Output data valid after address change		0		0		0		ns
$t_{en(W)}$	Output enable time from write enable high§	R1 = 481 Ω, R2 = 255 Ω, C_L = 5 pF, See Figure 1b	0		0		0		ns
$t_{en(E)}$	Output enable time from chip enable low§		5		5		5		ns
$t_{en(G)}$	Output enable time from output enable ($\overline{G}$) low§		0		0		0		ns
$t_{dis(E)}$	Output disable time from chip enable high§			15		20		20	ns
$t_{dis(W)}$	Output disable time from write enable low§			10		15		20	ns
$t_{dis(G)}$	Output disable time from output enable ($\overline{G}$) high§			12		15		15	ns

§Transition is measured ±500 mV from steady state voltage. This parameter is guaranteed but not tested.

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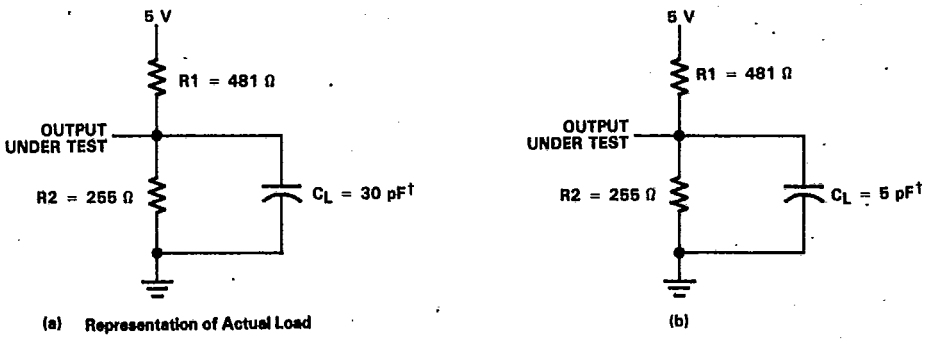
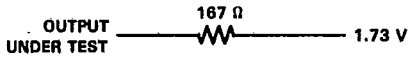
PARAMETER MEASUREMENT INFORMATION

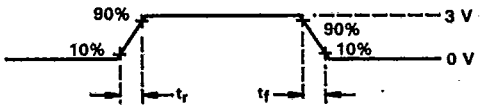


THEVENIN EQUIVALENT OF (a) OR (b)



†C_L includes jig and scope capacitances.

FIGURE 1. OUTPUT LOAD CIRCUIT

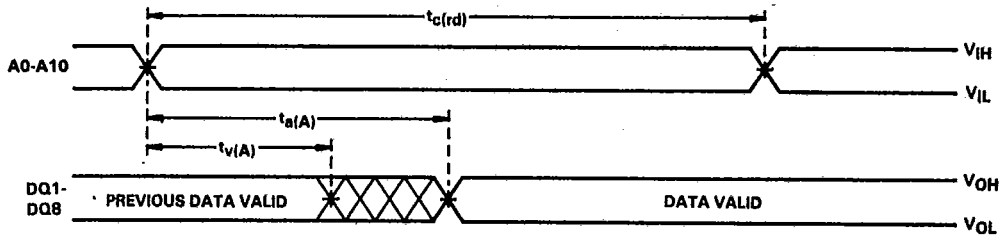


NOTE 4: t_r and $t_f \leq 5$ ns.

FIGURE 2. TRANSITION TIMES

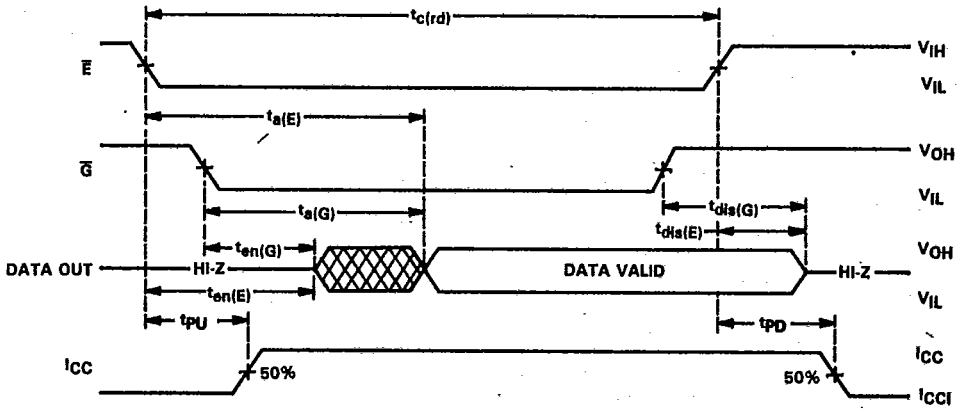
NOTE: All switching characteristics and timing requirements assume test conditions as depicted in Figures 1 and 2 with timing references of 1.5 V (50% reference point) as shown in the subsequent timing diagrams.

read cycle timing from address†



†When $\overline{W}$ is high, $\overline{E}$ is low, and $\overline{G}$ is low, device is continuously selected.

read cycle timing from chip enable‡



‡When $\overline{W}$ is high, address is valid prior to or simultaneously with the high-to-low transition of $\overline{E}$.

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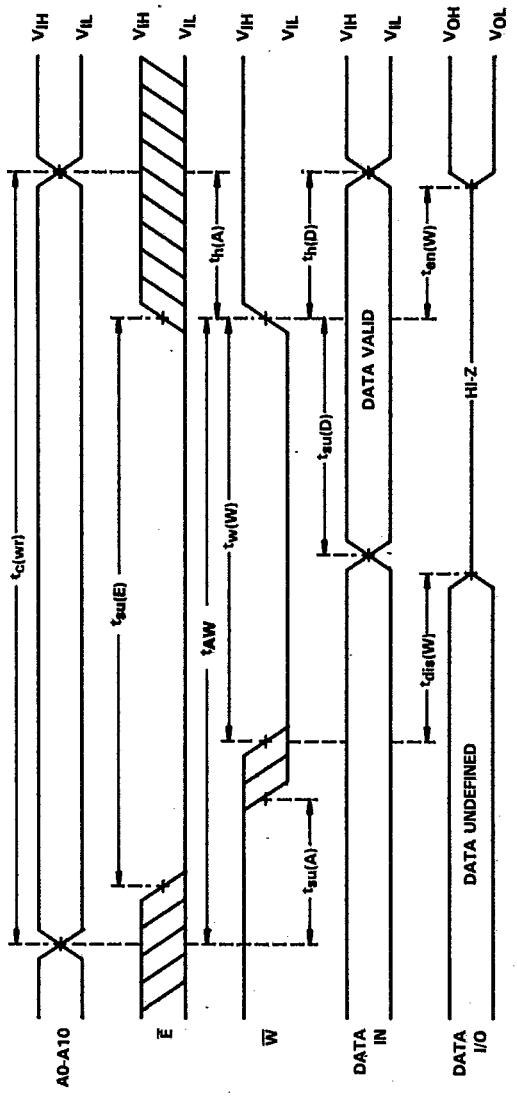
write cycle timing controlled by write enable†



† $\overline{E}$ or $\overline{W}$ must be high during address transitions.

NOTES: 4. The internal write time of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write, and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

5. Data I/O pins enter high-impedance state, as shown when $\overline{G}$ is held low during write.

write cycle timing controlled by chip enable†

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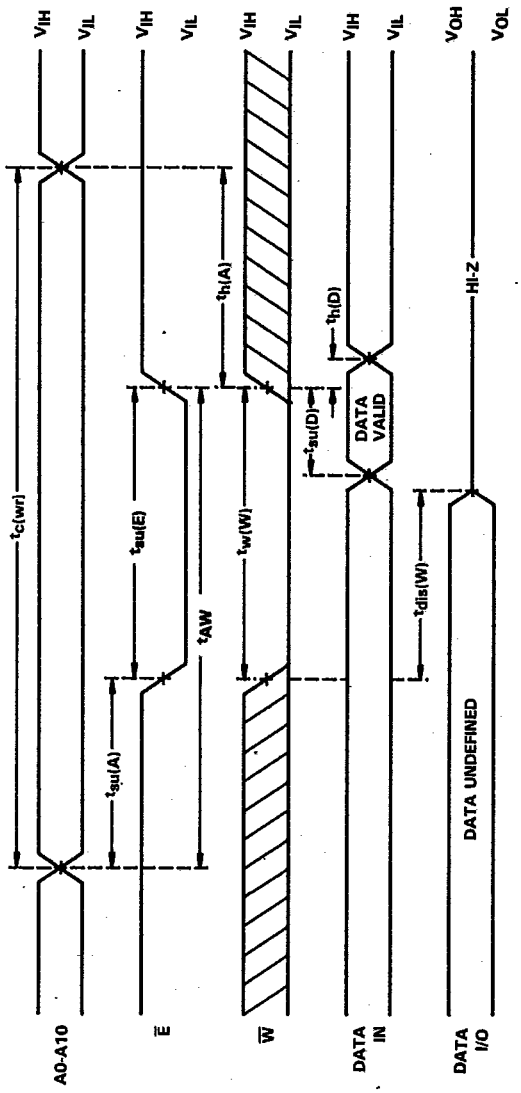

†E or W must be high during address transitions.
NOTE 5: Data I/O pins enter high-impedance state, as shown when G is held low during write.

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