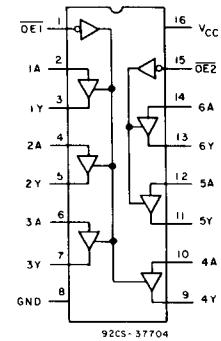
CD54HC367/3A
CD54HCT367/3A

Hex Buffer/Line Driver, 3-State

The RCA-CD54HC367 and CD54HCT367 silicon-gate CMOS three-state buffers are general-purpose high-speed buffers. They have high drive current outputs which enable high-speed operation even when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuitry, yet have speeds comparable to low-power Schottky TTL circuits. Both circuits are capable of driving up to 15 low-power Schottky inputs.

The CD54HC367 and CD54HCT367 are inverting buffers. These devices have two 3-state control inputs ($\overline{OE1}$) and ($\overline{OE2}$) which are NORed together to control all six gates.

The CD54HCT367 logic family is speed, function, and pin compatible with the standard 54LS logic family.



FUNCTIONAL DIAGRAM

Package Specifications

See Section 11, Fig. 11

Static Electrical Characteristics (Limits with black dots (•) are tested 100%)

CHARACTERISTICS		TEST CONDITIONS HC/HCT V_{DD}	V_O	I_O	V_{CC} or GND	V_{IN} HC V_{IL} or V_{IH}	V_{IN} HCT V_{IL} or V_{IH}	LIMITS MIN.	LIMITS MAX.	UNITS
Quiescent Device Current I_{CC}	25°C	6	—	—	6, 0	—	—	—	8•	μA
	-55°C / +125°C	6	—	—	6, 0	—	—	—	160•	μA

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

HCT INPUT LOADING TABLE

INPUT	UNIT LOAD*
$\overline{OE1}$	0.6
All Others	0.55

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

Switching Speed (Limits with black dots (•) are tested 100%.)

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	V_{CC}	25°C HC Min.	25°C HC Max.	25°C HCT Min.	25°C HCT Max.	-55°C to +125°C 54HC Min.	-55°C to +125°C 54HC Max.	-55°C to +125°C 54HCT Min.	-55°C to +125°C 54HCT Max.	UNITS
		V									
Propagation Delay Data to Outputs	t_{PLH} t_{PHL}	2	—	105	—	—	—	160	—	—	ns
		4.5	—	21•	—	25•	—	32•	—	38•	ns
		6	—	18	—	—	—	27	—	—	ns
Propagation Delay Output Enable and Disable to Outputs	t_{PZH}, t_{PZL}, t_{PHZ}, t_{PLZ}	2	—	150	—	—	—	225	—	—	ns
		4.5	—	30•	—	35•	—	45•	—	53•	ns
		6	—	26	—	—	—	38	—	—	ns
Output Transition Time	t_{TLH} t_{THL}	2	—	60	—	—	—	90	—	—	ns
		4.5	—	12	—	12	—	18	—	18	ns
		6	—	10	—	—	—	15	—	—	ns
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C_O	—	—	20	—	20	—	20	—	20	pF

CD54HC367/3A
CD54HCT367/3A

Burn-In Test-Circuit Connections (Use Static II for /3A burn-in and Dynamic for Life Test.)

Static	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
CD54HC/HCT367	3,5,7,9,11, 13	1,2,4,6,8,10,12, 14,15	16	3,5,7,9,11, 13	8	1,2,4,6,10,12, 14-16
Dynamic	**OPEN**	**GROUND**	**1/2 V_{CC} (3V)**	**V_{CC} (6V)**	**OSCILLATOR**	
					50 kHz	**25 kHz**
CD54HC/HCT367	—	1,8,15	3,5,7,9,11,13	16	2,4,6,10,12,14	—

NOTE: Each pin except V_{CC} and Gnd will have a resistor of 2k-47k ohms.

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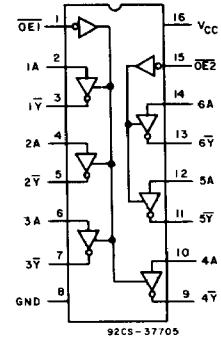
Hex Buffer/Line Driver, 3-State, Inverting

CD54HC368/3A
CD54HCT368/3A

The RCA-CD54HC368 and CD54HCT368 silicon-gate CMOS three-state buffers are general-purpose high-speed buffers. They have high drive current outputs which enable high-speed operation even when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuitry, yet have speeds comparable to low-power Schottky TTL circuits. Both circuits are capable of driving up to 15 low-power Schottky inputs.

The CD54HC368 and CD54HCT368 are inverting buffers. These devices have two output enables: one enable ($\overline{OE1}$) controls 4 gates and the other ($\overline{OE2}$) controls the remaining 2 gates.

The CD54HCT368 logic family is speed, function, and pin compatible with the standard 54LS logic family.



FUNCTIONAL DIAGRAM

Package Specifications

See Section 11, Fig. 11

HCT INPUT LOADING TABLE

INPUT	UNIT LOAD*
$\overline{OE1}$	0.6
All Others	0.55

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.