54F/74F552

Octal Registered Transceiver With Parity and Flags

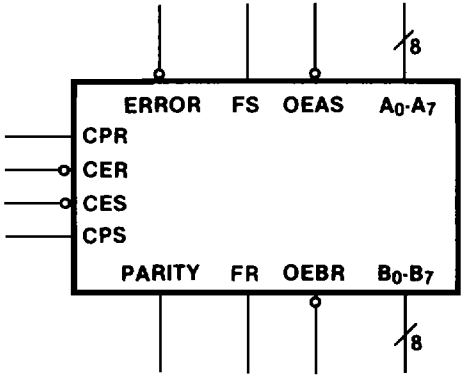
Description

The 'F552 octal transceiver contains two 8-bit registers for temporary storage of data flowing in either direction. Each register has its own clock pulse and clock enable input as well as a flag flip-flop that is set automatically as the register is loaded. The flag output will be reset when the output enable returns to HIGH after reading the output port. Each register has a separate output enable control for its 3-state buffer. The separate Clocks, Flags, and Enables provide considerable flexibility as I/O ports for demand-response data transfer. When data are transferred from the A-port to the B-port, a parity bit is generated. On the other hand, when data are transferred from the B-port to the A-port, the parity of input data on B_0-B_7 is checked.

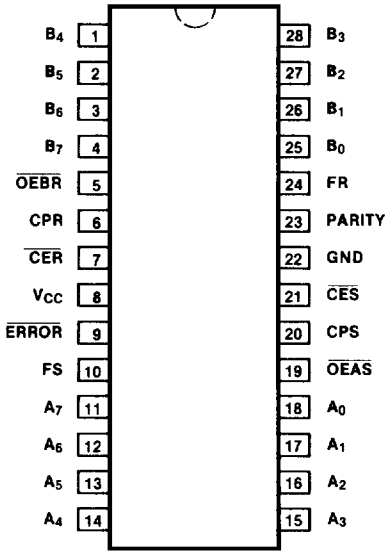
- **8-Bit Bidirectional I/O Port with Handshake**
- **Register Status Flag Flip-Flops**
- **Separate Clock Enable and Output Enable**
- **Parity Generation and Parity Check**
- **B-Outputs Sink 64 mA**

Ordering Code: See Section 5

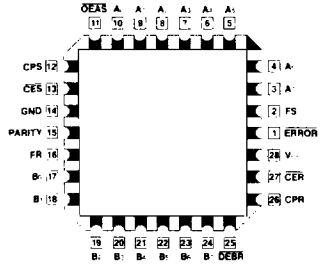
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_0-A_7	A Port Data Transceiver Input	1.75/0.406
	Output	75/15 (12.5)
B_0-B_7	B Port Data Transceiver Input	1.75/0.406
	Output	75/40 (30)
FR	B Port Flag Output	25/12.5
FS	A Port Flag Output	25/12.5
PARITY	Parity Bit Transceiver Input	1.75/0.406
	Output	75/40 (30)
$\overline{ERROR}$	Parity Check Output (Active LOW)	25/12.5
$\overline{CER}$	R Registers Clock Enable Input (Active LOW)	0.5/0.375
$\overline{CES}$	S Registers Clock Enable Input (Active LOW)	0.5/0.375
CPR	R Registers Clock Pulse Input (Active Rising Edge)	0.5/0.375
CPS	S Registers Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{OEBR}$	B Port and PARITY Output Enable (Active LOW) and Clear FR input (Active Rising Edge)	0.5/0.75
$\overline{OEAS}$	A Port Output Enable (Active LOW) and Clear FS input (Active Rising Edge)	0.5/0.75

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Functional Description

Data applied to the A-inputs are entered and stored in the R register on the rising edge of the CPR Clock Pulse, provided that the Clock Enable ($\overline{CER}$) is LOW; simultaneously, the status flip-flop is set and the flag (FR) output goes HIGH. As the Clock Enable ($\overline{CER}$) returns to HIGH, the data will be held in the R register. These data entered from the A-inputs will appear at the B-port I/O pins after the Output Enable ($\overline{OEBR}$) has gone LOW. When $\overline{OEBR}$ is LOW, a parity bit appears at the PARITY pin, which will be set HIGH when there is an even number of 1s or all 0s at the Q outputs of the R register. After the data are assimilated, the receiving system clears the flag FR by changing the signal at the $\overline{OEBR}$ pin from LOW to HIGH.

Data flow from B-to-A flow proceeds in the same manner described for A-to-B flow. A LOW at the $\overline{CES}$ pin and a LOW-to-HIGH transition at CPS pin enter the B-input data and the parity-input data into the S register and the parity register respectively and set the flag output FS to HIGH. A LOW signal at the $\overline{OEAS}$ pin enables the A-port I/O pins and a LOW-to-HIGH transition of the $\overline{OEAS}$ signal clears the FS flag. When $\overline{OEAS}$ is LOW, the parity check output $\overline{ERROR}$ will be HIGH if there is an odd number of 1s at the Q outputs of the S registers and the parity register. The flag FS can be cleared by a LOW-to-HIGH transition of the $\overline{OEAS}$ signal.

Register Function Table

(Applies to R or S Register)

Inputs			Internal Q	Function
D	CP	$\overline{CE}$		
X	X	H	NC	Hold Data
L	↑	L	L	Load Data
H	↑	L	H	
M	↓	L	NC	Keep Old Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↑ = LOW-to-HIGH Transition
↓ = Not LOW-to-HIGH Transition
NC = No Change

Output Control

$\overline{OE}$	Internal Q	A or B Outputs	Function
H	X	Z	Disable Output
L	L	L	Enable Output
L	H	H	

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Flag Flip-Flop Function Table
(Applies to R or S Flag Flip-Flop)

Inputs			Flag Output	Function
$\overline{CE}$	CP	$\overline{OE}$		
H	X	‡	NC	Hold Flag
L	↑	‡	H	Set Flag
X	X	‡	L	Clear Flag

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↑ = LOW-to-HIGH Transition
‡ = Not LOW-to-HIGH Transition
NC = No Change

Parity Generation Function

$\overline{OEBR}$	Number of HIGHs in the Q Outputs of the R Register	Parity Output
H	X	Z
L	0,2,4,6,8	H
L	1,3,5,7	L

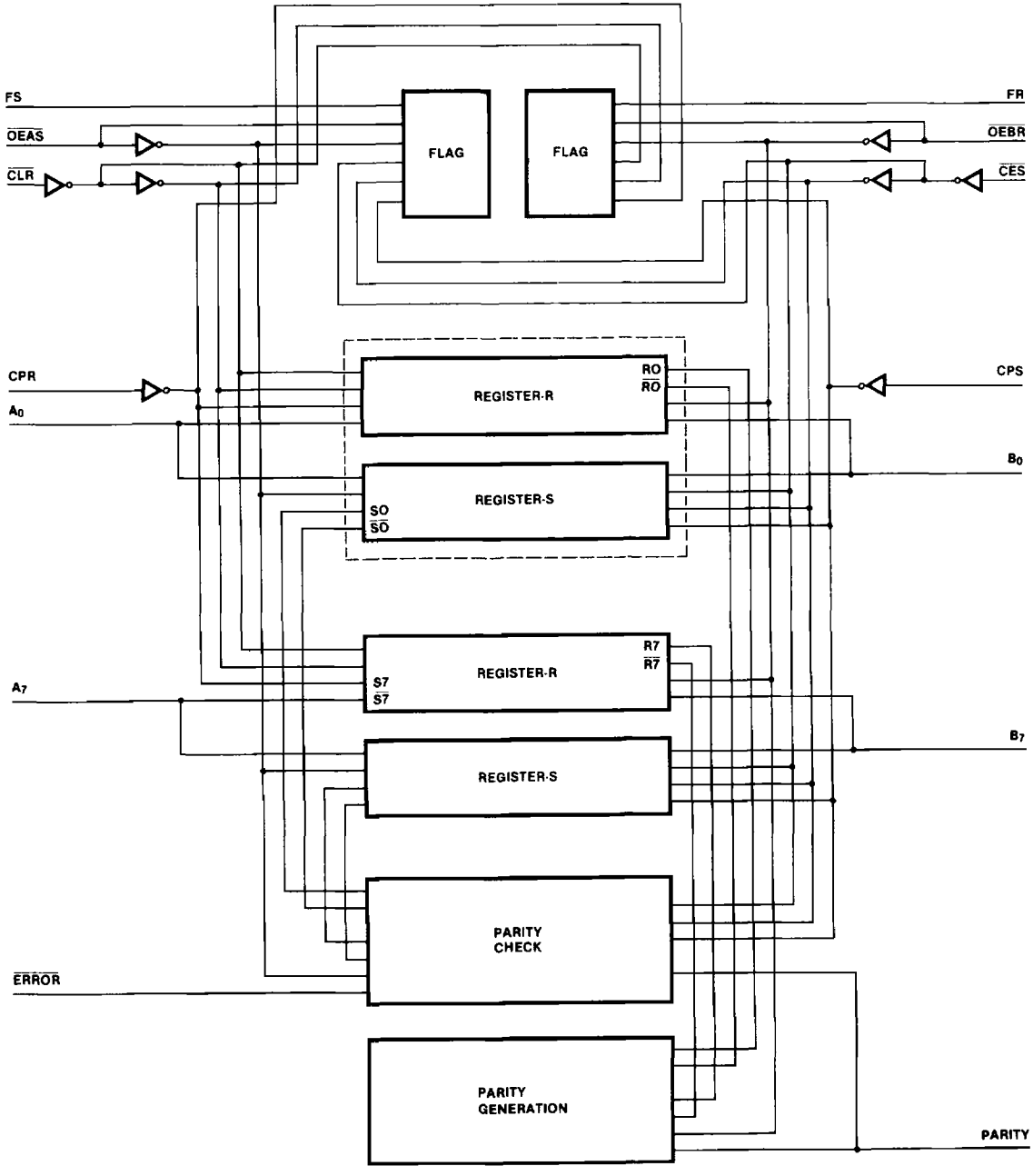
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Parity Check Function

$\overline{OEAS}$	Number of HIGHs in the Q Outputs of the S Register	Parity Input	$\overline{ERROR}$ Output
H	X	X	H
L	0,2,4,6,8	L	L
L	1,3,5,7	L	H
L	0,2,4,6,8	H	H
L	1,3,5,7	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Block Diagram



DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CCZ}	Power Supply Current		110	165	mA	V_{CC} = Max
I_{CCL}			100	150		
I_{CCH}			100	150		

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C, V_{CC} = +5.0 V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.5	6.0	8.0			3.0	9.0	ns	3-1
t_{PHL}	CPS or CPR to A_n or B_n	4.0	7.0	9.5			3.5	10.5		3-7
t_{PLH}	Propagation Delay CPS or CPR to FS or FR	3.0	5.5	7.5			2.5	8.5	ns	3-1, 3-7
t_{PHL}	Propagation Delay $\overline{OEAS}$ to FS	3.5	6.0	8.0			3.0	9.0	ns	3-1, 3-4
t_{PLH}	Propagation Delay	8.0	14.0	18.0			7.0	20.0	ns	3-1
t_{PHL}	CPS to Parity	8.5	14.5	18.5			7.5	20.5		3-11
t_{PLH}	Propagation Delay	8.0	13.5	17.5			7.0	19.5	ns	3-1
t_{PHL}	CPR to $\overline{ERROR}$	7.5	13.0	16.5			6.5	18.5		3-11
t_{PLH}	Propagation Delay	3.5	6.0	8.0			3.0	9.0	ns	3-1
t_{PHL}	$\overline{OEAS}$ to $\overline{ERROR}$	3.0	5.0	7.0			2.5	8.0		3-11
t_{PZH}	Enable Time	3.0	5.5	7.5			2.5	8.5	ns	3-1, 3-12, 3-3
t_{PZL}	$\overline{OEAS}$ or $\overline{OEBR}$ to B_n or A_n	3.5	7.0	9.5			3.0	10.5		
t_{PHZ}	Disable Time	3.0	6.5	8.5			2.5	9.5		
t_{PLZ}	$\overline{OEAS}$ or $\overline{OEBR}$ to B_n or A_n	3.0	5.5	7.5			2.5	8.5		
t_{PZH}	Enable Time	2.5	4.5	6.0			2.0	7.0	ns	3-1, 3-12, 3-13
t_{PZL}	$\overline{OEBR}$ to Parity	3.5	6.0	8.0			3.0	9.0		
t_{PHZ}	Disable Time	3.5	5.5	7.0			2.5	8.0		
t_{PLZ}	$\overline{OEBR}$ to Parity	3.0	6.5	8.5			2.5	9.5		

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A_n or B_n or Parity to CPS or CPR	7.5 4.5		8.5 5.0	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A_n or B_n or Parity to CPS or CPR	0 0		0 0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{CES}$ or $\overline{CER}$ to CPS or CPR	6.0 10.0		7.0 11.5	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{CES}$ or $\overline{CER}$ to CPS or CPR	0 0		0 0		
$t_w(H)$ $t_w(L)$	Pulse Width, HIGH or LOW CPS or CPR	4.0 6.0		4.5 7.0	ns	3-7

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