256K x 4 Bit (with $\overline{OE}$)High-Speed CMOS Static RAM

FEATURES

- Fast Access Time 8,10,12ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 60mA(Max.)
  - (CMOS) : 10mA(Max.)
  - Operating KM64B1003 - 8 : 165mA(Max.)
  - KM64B1003 - 10 : 155mA(Max.)
  - KM64B1003 - 12 : 145mA(Max.)
- Single 5.0V ±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible With 3.3V Devices.
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM64B1003J : 32-SOJ-400

GENERAL DESCRIPTION

The KM64B1003 is a 1,048,576-bit high-speed Static Random Access Memory organized as 262,144 words by 4 bits. The KM64B1003 uses 4 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using SAMSUNG's advanced BiCMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM64B1003 is packaged in a 400 mil 32-pin plastic SOJ.

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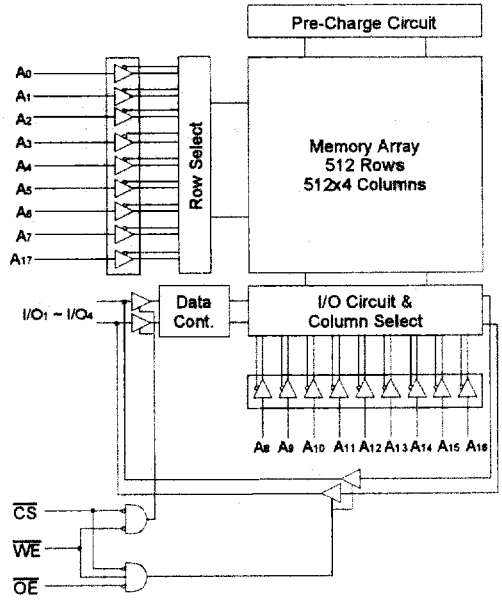
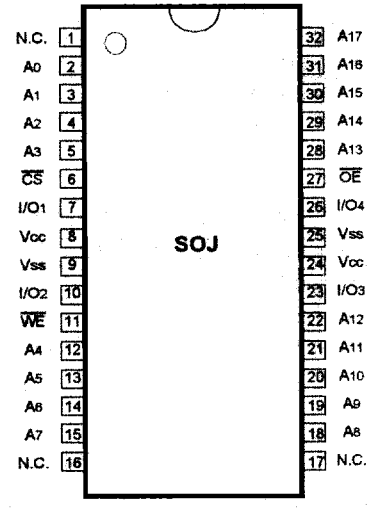
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION(Top View)



PIN FUNCTION

Pin Name	Pin Function
A0 - A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
I/O1 ~ I/O4	Data Inputs/Outputs
Vcc	Power(+5.0V)
Vss	Ground
N.C	No Connection

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ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS(T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	Vcc+0.5**	V
Input Low Voltage	V_{IL}	-0.5*	-	0.8	V

* V_{IL}(Min) =-2.0V a.c(Pulse Width≤6ns) for I≤20mA
** V_{IH}(Max) = Vcc + 2.0V a.c (Pulse Width≤6ns) for I≤20mA

DC AND OPERATING CHARACTERISTICS(T_A=0 to 70°C, Vcc=5.0V±10%, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to Vcc		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT}=Vss to Vcc		-10	10	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA	8ns	-	165	mA
			10ns	-	155	
			12ns	-	145	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	60	mA
	I_{SB1}	f=0MHz, $\overline{CS}$≥Vcc-0.2V, V_{IN}≥Vcc-0.2V or V_{IN}≤0.2V		-	10	mA
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V
	V_{OH1}*	I_{OH1}=-100μA		-	3.95	

* Vcc=5.0V, Temp.=25°C

CAPACITANCE*(T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF

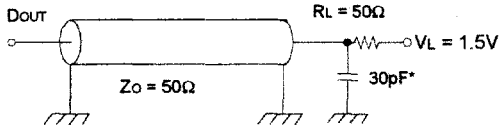
* NOTE : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS(T_A=0 to 70°C, V_{CC}=5.0V±10%, unless otherwise noted.)

TEST CONDITIONS

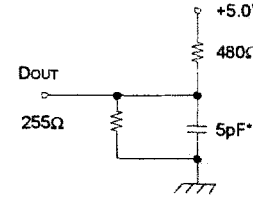
Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



* Capacitive Load consists of all components of the test environment.

Output Loads(B)
for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ}



* Including Scope and Jig Capacitance

READ CYCLE

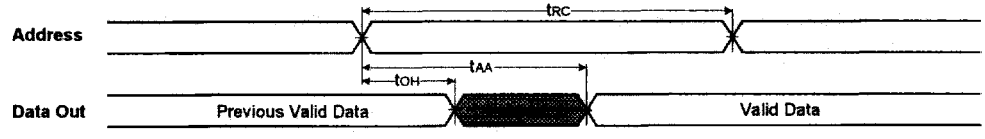
Parameter	Symbol	KM64B1003-8		KM64B1003-10		KM64B1003-12		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	8	-	10	-	12	-	ns
Address Access Time	t_{AA}	-	8	-	10	-	12	ns
Chip Select to Output	t_{CO}	-	8	-	10	-	12	ns
Output Enable to Valid Output	t_{OE}	-	4	-	5	-	6	ns
Chip Enable to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	4	0	5	0	6	ns
Output Disable to High-Z Output	t_{OHZ}	0	4	0	5	0	6	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns

WRITE CYCLE

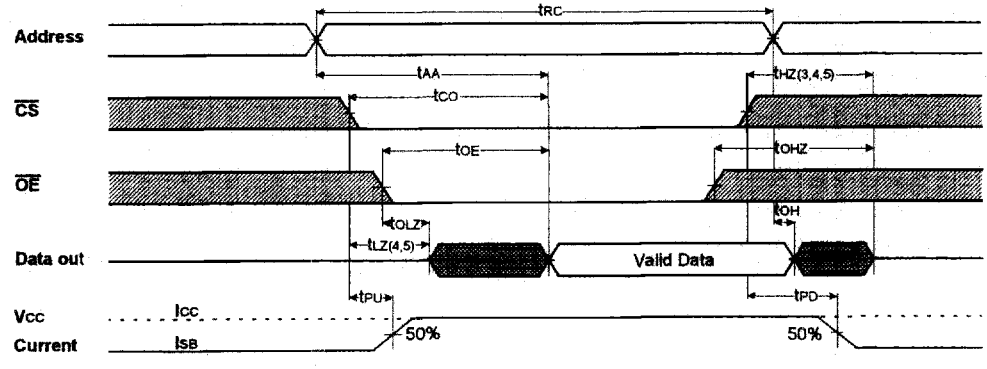
Parameter	Symbol	KM64B1003-8		KM64B1003-10		KM64B1003-12		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	8	-	10	-	12	-	ns
Chip Select to End of Write	t_{CW}	6	-	7	-	8	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	6	-	7	-	8	-	ns
Write Pulse Width($\overline{OE}$ High)	t_{WP}	6	-	7	-	8	-	ns
Write Pulse Width($\overline{OE}$ Low)	t_{WP1}	8	-	9	-	10	-	ns
Write Recovery Time	t_{WR}	1	-	1	-	1	-	ns
Write to Output High-Z	t_{WHZ}	0	4	0	5	0	6	ns
Data to Write Time Overlap	t_{DW}	4	-	5	-	6	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
End Write to Output Low-Z	t_{OW}	3	-	3	-	3	-	ns

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



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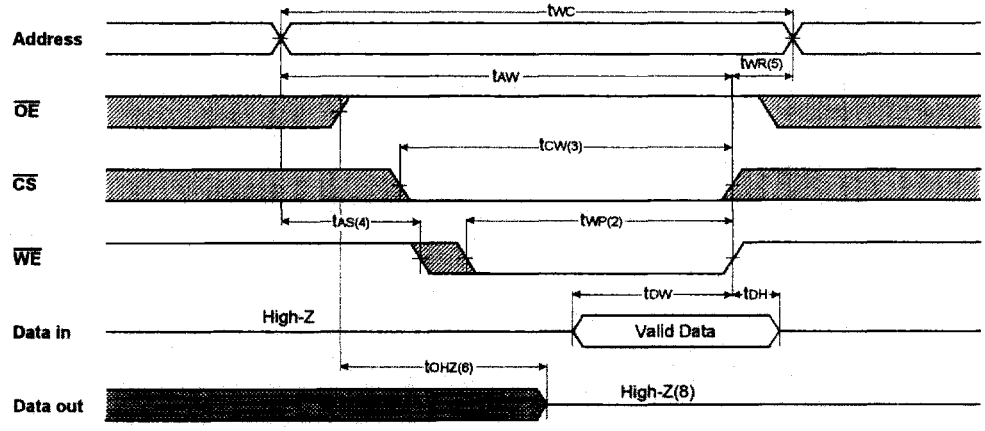
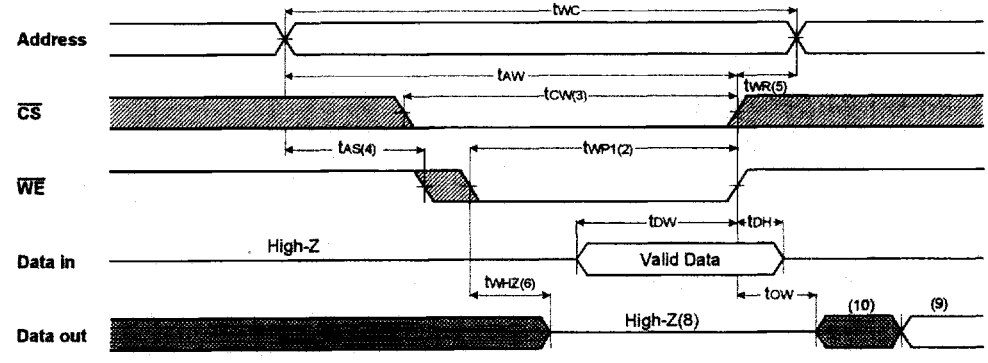
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=V_{IL}.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$= Clock)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



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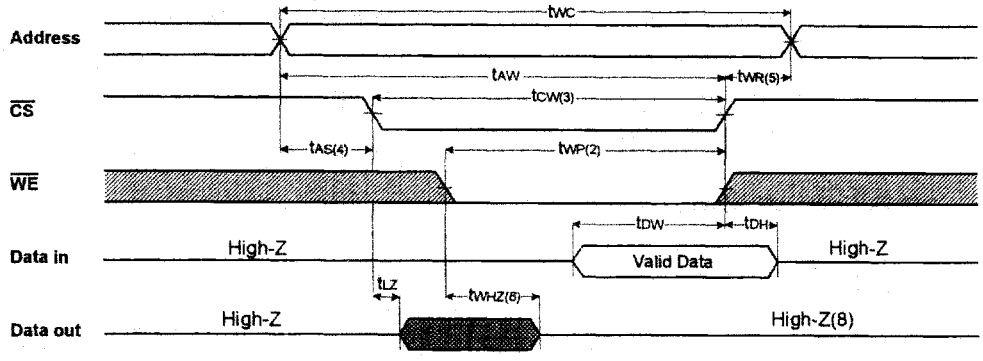
TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* NOTE : X means Don't Care.