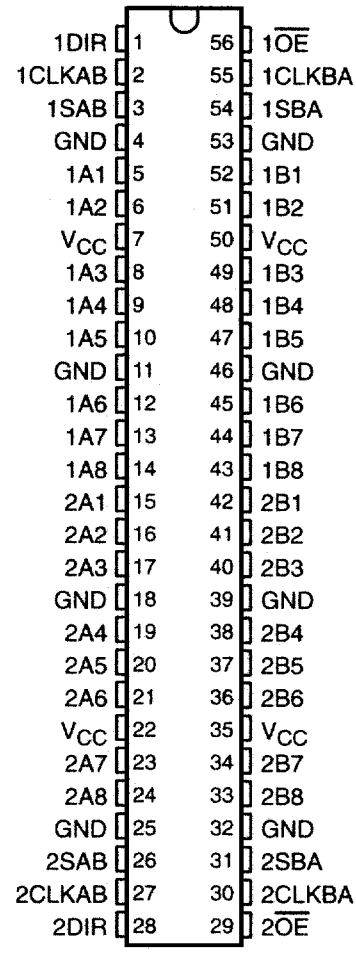
- Members of the Texas Instruments *Widebus*™ Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V $V_{CC}$)
- Support Unregulated Battery Operation Down to 2.7 V
- High-Impedance State During Power Up and Power Down
- Typical $V_{OLP}$ (Output Ground Bounce) < 0.8 V at $V_{CC}$ = 3.3 V, $T_A$ = 25°C
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Power Off Disables Outputs, Permitting Live Insertion
- Distributed $V_{CC}$ and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Spacings

**SN54LVTH16646 . . . WD PACKAGE**
**SN74LVTH16646 . . . DGG OR DL PACKAGE**
**(TOP VIEW)**




## description

The 'LVTH16646 devices are 16-bit bus transceivers designed for low-voltage (3.3-V) $V_{CC}$ operation, but with the capability to provide a TTL interface to a 5-V system environment.

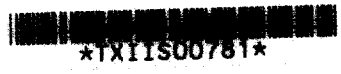
These devices can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVTH16646 devices.



Widebus is a trademark of Texas Instruments Incorporated.







## description (continued)

Output-enable ($\overline{OE}$) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. DIR determines which bus receives data when $\overline{OE}$ is low. In the isolation mode ($\overline{OE}$ high), A data can be stored in one register and/or B data can be stored in the other register.

When an output function is disabled, the input function is still enabled and can be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

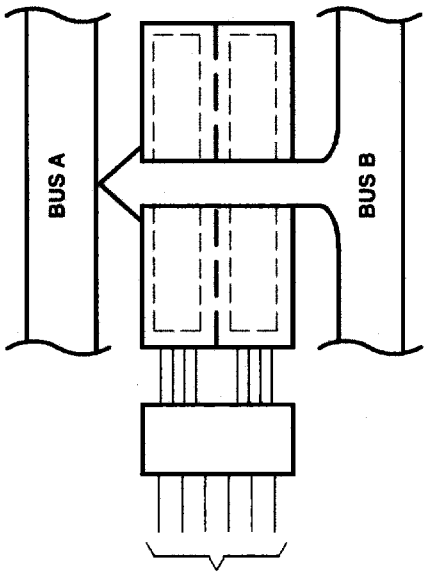
When $V_{CC}$ is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54LVTH16646 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74LVTH16646 is characterized for operation from –40°C to 85°C.

**FUNCTION TABLE**

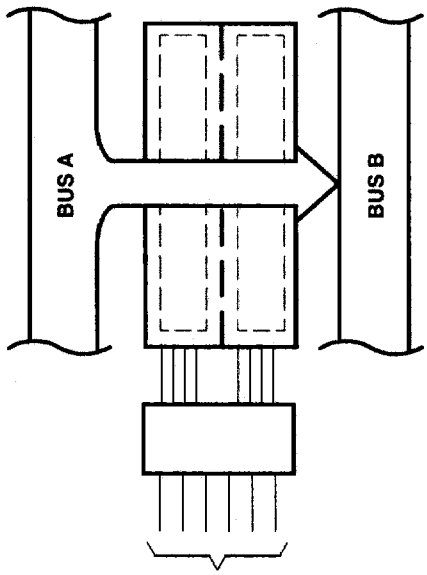
| INPUTS | | | | | | DATA I/O | | OPERATION OR FUNCTION |
|---|---|---|---|---|---|---|---|---|
| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA | A1–A8 | B1–B8 | |
| X | X | ↑ | X | X | X | Input | Unspecified† | Store A, B unspecified† |
| X | X | X | ↑ | X | X | Unspecified† | Input | Store B, A unspecified† |
| H | X | ↑ | ↑ | X | X | Input | Input | Store A and B data |
| H | X | H or L | H or L | X | X | Input disabled | Input disabled | Isolation, hold storage |
| L | L | X | X | X | L | Output | Input | Real-time B data to A bus |
| L | L | X | H or L | X | H | Output | Input | Stored B data to A bus |
| L | H | X | X | L | X | Input | Output | Real-time A data to B Bus |
| L | H | H or L | X | H | X | Input | Output | Stored A data to bus |

† The data-output functions may be enabled or disabled by various signals at $\overline{OE}$ or DIR. Data-input functions are always enabled, i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.



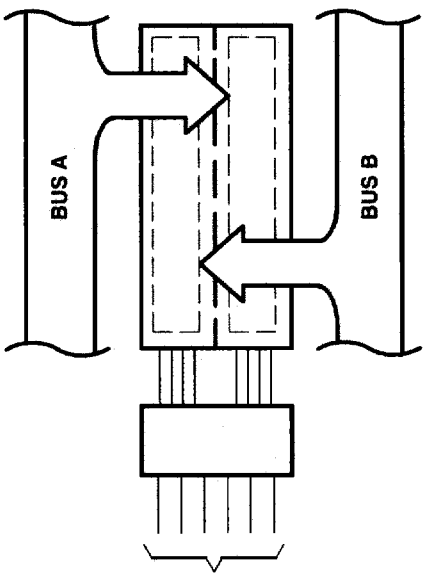

| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| L | L | X | X | X | L |

**REAL-TIME TRANSFER**
**BUS B TO BUS A**



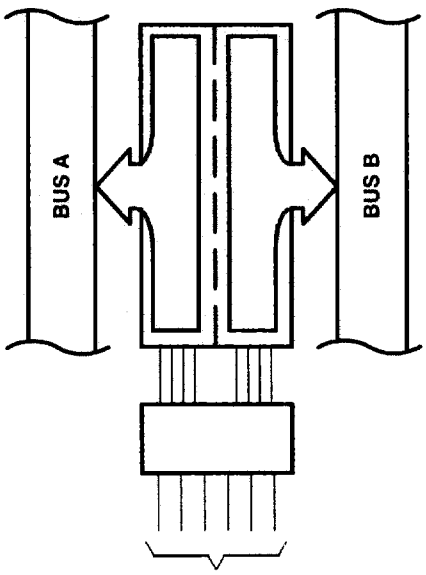

| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| L | H | X | X | L | X |

**REAL-TIME TRANSFER**
**BUS A TO BUS B**




| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| X | X | ↑ | X | X | X |
| X | X | X | ↑ | X | X |
| H | X | ↑ | ↑ | X | X |

**STORAGE FROM**
**A, B, OR A AND B**

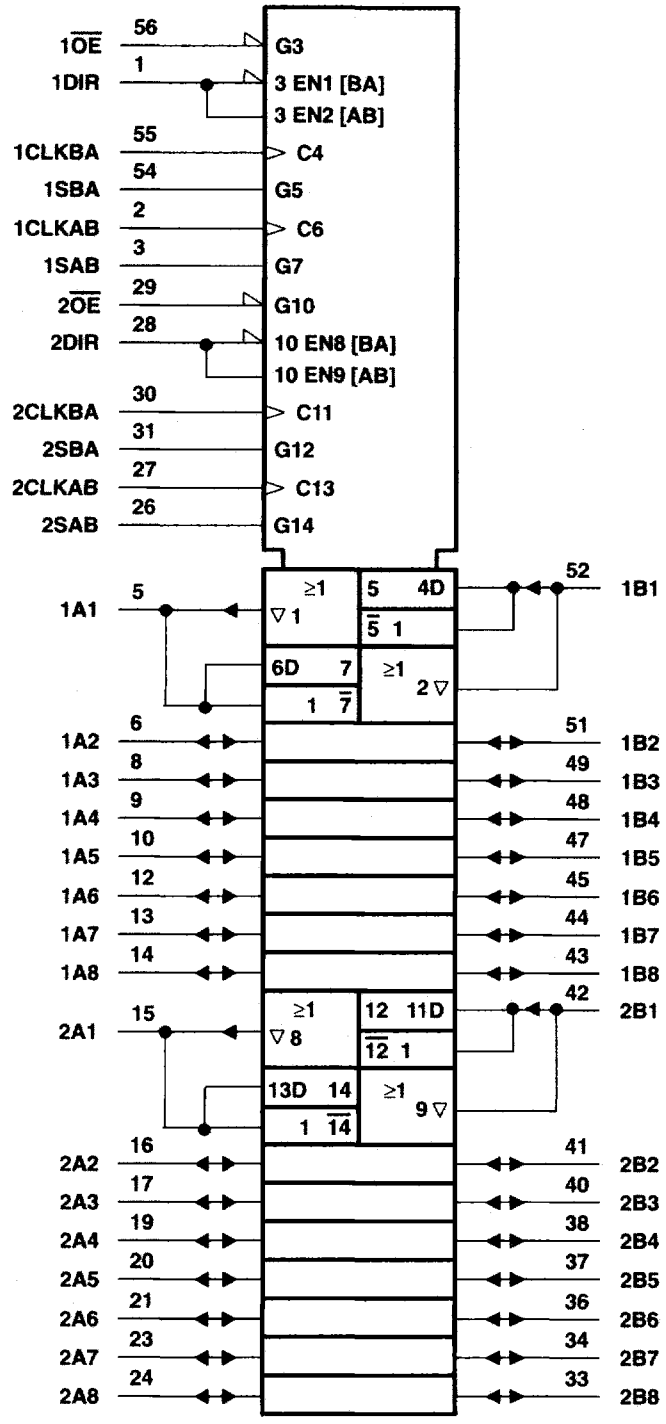



| $\overline{OE}$ | DIR | CLKAB | CLKBA | SAB | SBA |
|---|---|---|---|---|---|
| L | L | X | H or L | X | H |
| L | H | H or L | X | H | X |

**TRANSFER STORED DATA**
**TO A AND/OR B**

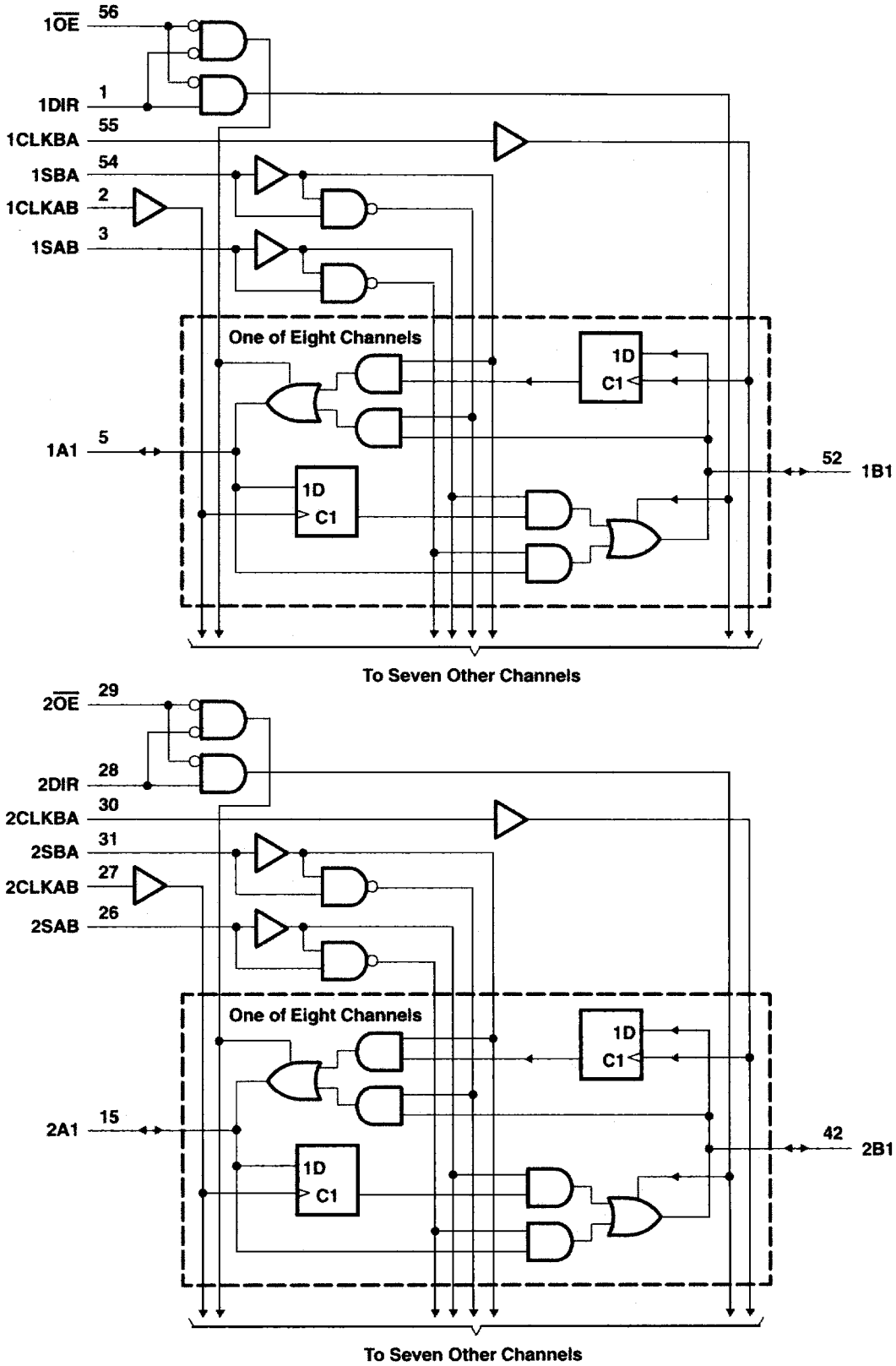
**Figure 1. Bus-Management Functions**

## logic symbol†




† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ ..... –0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) ..... –0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) ..... –0.5 V to 7 V
Voltage range applied to any output in the high state, $V_O$ (see Note 1) ..... –0.5 V to $V_{CC}$ + 0.5 V
Current into any output in the low state, $I_O$: SN54LVTH16646 ..... 96 mA
SN74LVTH16646 ..... 128 mA
Current into any output in the high state, $I_O$ (see Note 2): SN54LVTH16646 ..... 48 mA
SN74LVTH16646 ..... 64 mA
Input clamp current, $I_{IK}$ ($V_I$ < 0) ..... –50 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0) ..... –50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DGG package ..... 81°C/W
DL package ..... 74°C/W
Storage temperature range, $T_{stg}$ ..... –65 C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions (see Note 4)

| | | | SN54LVTH16646 | | SN74LVTH16646 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2.7 | 3.6 | 2.7 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | | 0.8 | V |
| $V_I$ | Input voltage | | | 5.5 | | 5.5 | V |
| $I_{OH}$ | High-level output current | | | –24 | | –32 | mA |
| $I_{OL}$ | Low-level output current | | | 48 | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 10 | | 10 | ns/V |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate | | 200 | | 200 | | µs/V |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 4: All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | SN54LVTH16646 | | | SN74LVTH16646 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP† | MAX | MIN | TYP† | MAX | |
| $V_{IK}$ | | $V_{CC}$ = 2.7 V, | $I_I$ = –18 mA | | | –1.2 | | | –1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 2.7 V to 3.6 V, | $I_{OH}$ = –100 µA | $V_{CC}$–0.2 | | | $V_{CC}$–0.2 | | | V |
| | | $V_{CC}$ = 2.7 V, | $I_{OH}$ = –8 mA | 2.4 | | | 2.4 | | | |
| | | $V_{CC}$ = 3 V | $I_{OH}$ = –24 mA | 2 | | | | | | |
| | | | $I_{OH}$ = –32 mA | | | | 2 | | | |
| $V_{OL}$ | | $V_{CC}$ = 2.7 V | $I_{OL}$ = 100 µA | | | 0.2 | | | 0.2 | V |
| | | | $I_{OL}$ = 24 mA | | | 0.5 | | | 0.5 | |
| | | $V_{CC}$ = 3 V | $I_{OL}$ = 16 mA | | | 0.4 | | | 0.4 | |
| | | | $I_{OL}$ = 32 mA | | | 0.5 | | | 0.5 | |
| | | | $I_{OL}$ = 48 mA | | | 0.55 | | | | |
| | | | $I_{OL}$ = 64 mA | | | | | | 0.55 | |
| $I_I$ | Control inputs | $V_{CC}$ = 3.6 V, | $V_I$ = $V_{CC}$ or GND | | | ±1 | | | ±1 | µA |
| | | $V_{CC}$ = 0 or 3.6 V, | $V_I$ = 5.5 V | | | 10 | | | 10 | |
| | A or B ports‡ | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | | | 20 | | | 20 | |
| | | | $V_I$ = $V_{CC}$ | | | 1 | | | 1 | |
| | | | $V_I$ = 0 | | | –5 | | | –5 | |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O$ = 0 to 4.5 V | | | | | | ±100 | µA |
| $I_{I(hold)}$ | A or B ports | $V_{CC}$ = 3 V | $V_I$ = 0.8 V | 75 | | | 75 | | | µA |
| | | | $V_I$ = 2 V | –75 | | | –75 | | | |
| $I_{OZPU}$ | | $V_{CC}$ = 0 to 1.5 V, $V_O$ = 0.5 V to 3 V, $\overline{OE}$ = don't care | | | | ±100* | | | ±100 | µA |
| $I_{OZPD}$ | | $V_{CC}$ = 1.5 V to 0, $V_O$ = 0.5 V to 3 V, $\overline{OE}$ = don't care | | | | ±100* | | | ±100 | µA |
| $I_{CC}$ | | $V_{CC}$ = 3.6 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | Outputs high | | | 0.19 | | | 0.19 | mA |
| | | | Outputs low | | | 5 | | | 5 | |
| | | | Outputs disabled | | | 0.19 | | | 0.19 | |
| $\Delta I_{CC}$§ | | $V_{CC}$ = 3 V to 3.6 V, One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | | | | 0.2 | | | 0.2 | mA |
| $C_i$ | | $V_I$ = 3 V or 0 | | | 4 | | | 4 | | pF |
| $C_{io}$ | | $V_O$ = 3 V or 0 | | | 10 | | | 10 | | pF |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.
† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ Unused pins at $V_{CC}$ or GND
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than $V_{CC}$ or GND.

## timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

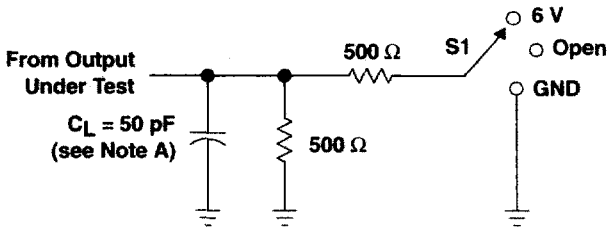
| | | | SN54LVTH16646 | | | | SN74LVTH16646 | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | | 150 | | 150 | | 150 | | 150 | MHz |
| $t_w$ | Pulse duration, CLK high or low | | 3.3 | | 3.3 | | 3.3 | | 3.3 | | ns |
| $t_{su}$ | Setup time, A or B before CLKAB↑ or CLKBA↑ | Data high | 1.2 | | 1.5 | | 1.2 | | 1.5 | | ns |
| | | Data low | 2 | | 2.8 | | 2 | | 2.8 | | |
| $t_h$ | Hold time, A or B after CLKAB↑ or CLKBA↑ | Data high | 0.5 | | 0 | | 0.5 | | 0 | | ns |
| | | Data low | 0.5 | | 0.5 | | 0.5 | | 0.5 | | |

## switching characteristics over recommended operating free-air temperature range, $C_L$ = 50 pF (unless otherwise noted) (see Figure 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH16646 | | | | SN74LVTH16646 | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | | $V_{CC}$ = 2.7 V | | |
| | | | MIN | MAX | MIN | MAX | MIN | TYP† | MAX | MIN | MAX | |
| $f_{max}$ | | | 150 | | 150 | | 150 | | | 150 | | MHz |
| $t_{PLH}$ | CLKBA or CLKAB | A or B | 1.3 | 4.5 | | 5 | 1.3 | 2.8 | 4.2 | | 4.7 | ns |
| $t_{PHL}$ | | | 1.3 | 4.5 | | 5 | 1.3 | 2.8 | 4.2 | | 4.7 | |
| $t_{PLH}$ | A or B | B or A | 1 | 3.6 | | 4.1 | 1 | 2.4 | 3.4 | | 3.9 | ns |
| $t_{PHL}$ | | | 1 | 3.6 | | 4.1 | 1 | 2.1 | 3.4 | | 3.9 | |
| $t_{PLH}$ | SBA or SAB‡ | A or B | 1 | 4.7 | | 5.6 | 1 | 2.8 | 4.5 | | 5.4 | ns |
| $t_{PHL}$ | | | 1 | 4.7 | | 5.6 | 1 | 3 | 4.5 | | 5.4 | |
| $t_{PZH}$ | $\overline{OE}$ | A or B | 1 | 4.5 | | 5.4 | 1 | 2.5 | 4.3 | | 5.2 | ns |
| $t_{PZL}$ | | | 1 | 4.5 | | 5.4 | 1 | 2.6 | 4.3 | | 5.2 | |
| $t_{PHZ}$ | $\overline{OE}$ | A or B | 2 | 5.8 | | 6.3 | 2 | 4 | 5.6 | | 6.1 | ns |
| $t_{PLZ}$ | | | 2 | 5.6 | | 6.3 | 2 | 3.6 | 5.4 | | 6.1 | |
| $t_{PZH}$ | DIR | A or B | 1 | 4.6 | | 5.5 | 1 | 3 | 4.4 | | 5.3 | ns |
| $t_{PZL}$ | | | 1 | 4.6 | | 5.5 | 1 | 3 | 4.4 | | 5.3 | |
| $t_{PHZ}$ | DIR | A or B | 1.5 | 6 | | 7.1 | 1.5 | 3.9 | 5.7 | | 6.8 | ns |
| $t_{PLZ}$ | | | 1.5 | 5.5 | | 6 | 1.5 | 3.6 | 5.2 | | 5.7 | |

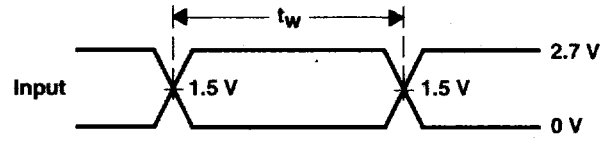
† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ These parameters are measured with the internal output state of the storage register opposite that of the bus input.

## PARAMETER MEASUREMENT INFORMATION

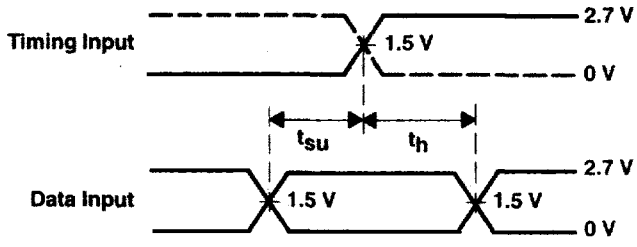



LOAD CIRCUIT

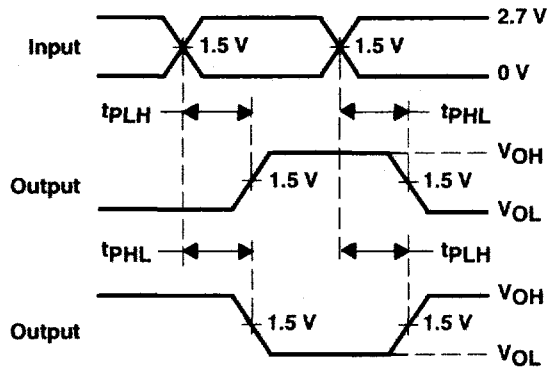
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V |
| $t_{PHZ}/t_{PZH}$ | GND |



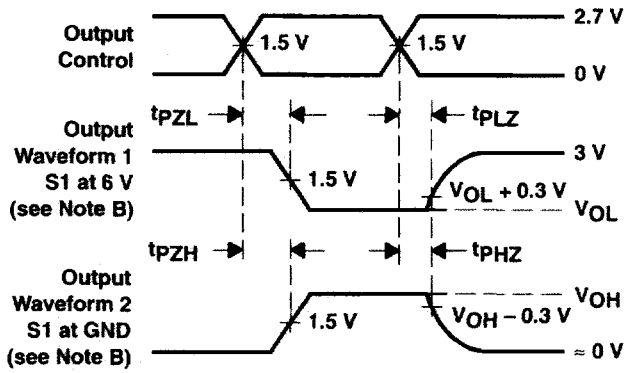

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. *Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.* Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.

**Figure 2. Load Circuit and Voltage Waveforms**

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