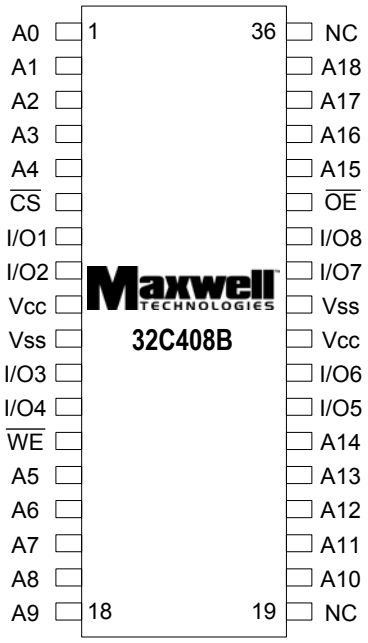
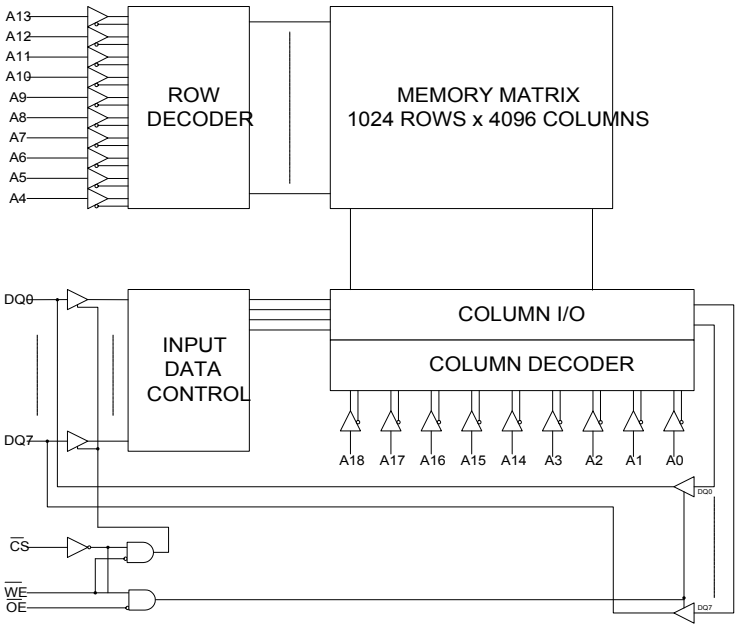
32C408B
4 Megabit (512K x 8-Bit) SRAM





Logic Diagram

FEATURES:

- 512k x 8-bit CMOS architecture
- RAD-PAK® technology hardened against natural space radiation
- Total dose hardness:
  - > 100 krad (Si), depending upon space mission
- Single event effect:
  - SEL_{TH}: ≥ 68 MeV/mg/cm^2
  - SEU_{TH}: < 3MeV/mg/cm^2
  - SEU saturated cross section: 6E-9 cm^2/bit
- Package:
  -36 pin RAD-PAK® flat pack
- Fast propagation time:
  -20, 25, 30 ns maximum access time
- Single 5V ± 10% power supply
- Low power dissipation:
  - Standby: 60mA (TTL); 10mA (CMOS)
  - Operating: 180 mA (20 ns); 170 mA (25 ns); 160 mA (30 ns)
- TTL compatible inputs and outputs
- Fully static operation
  - No clock or refresh required
- Three state outputs

DESCRIPTION:

Maxwell Technologies' 32C408B high-speed 4 Megabit SRAM microcircuit features a greater than 100 krad (Si) total dose tolerance, depending upon space mission. Using RAD-PAK® packaging technology, the 32C408B realizes higher density, higher performance and lower power consumption, and is well suited for high-speed system application. Its fully static design eliminates the need for external clocks, while the CMOS circuitry reduces power consumption and provides higher reliability. The 32C408B is equipped with eight common input/output lines, chip select and output enable, allowing for greater system flexibility and eliminating bus contention.

Maxwell Technologies' patented RAD-PAK packaging technology incorporates radiation shielding in the microcircuit package. In a GEO orbit, RAD-PAK can provides true greater than 100 krad (Si) total radiation dose tolerance; dependent upon space mission. The patented radiation-hardened RAD-PAK technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or a space mission. This product is available with packaging and screening up to Class S.

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TABLE 1. 32C408B ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.5	V_{CC}+0.5	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	-0.5	7.0	V
Power Dissipation	P_D	--	1.0	W
Storage Temperature	T_S	-65	+150	˚C
Operating Temperature	T_A	-55	+125	˚C

TABLE 2. 32C408B RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	V_{CC}	4.5	5.5	V
Ground	V_{SS}	0	0	V
Input High Voltage [1]	V_{IH}	2.2	V_{CC}+0.5	V
Input Low Voltage [2]	V_{IL}	-0.5	0.8	V
Thermal Impedance	Θ_{JC}	--	0.63	°C/W

1. V_{IH}(max) = V_{CC} + 2.0V ac(pulse width ≤ 10ns) for I ≤ 20mA.
2. V_{IL} (min) = -2.0V ac(pulse width ≤ 10ns) for I ≤ 20mA.

TABLE 3. 32C408B DC ELECTRICAL CHARACTERISTICS[1]

PARAMETER	CONDITION	SYMBOL	MIN	TYP	MAX	UNIT
Input Leakage Current	V_{IN} = V_{SS} to V_{CC}	I_{LI}	-2	--	2	µA
Output Leakage Current	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{OUT} =V_{SS} to V_{CC}	I_{LO}	-2	--	2	µA
Output Low Voltage	I_{OL} = 8mA	V_{OL}	--	--	0.4	V
Output High Voltage	I_{OH} = -4mA	V_{OH}	2.4		--	V
Average Operating Current -20 -25 -30	Min cycle, 100% Duty, $\overline{CS}$=V_{IL}, I_{OUT}=0mA, V_{IN} = V_{IH} or V_{IL}	I_{CC}	 -- -- --	--	 180 170 160	mA
Standby Power Supply Current	$\overline{CS}$ = V_{IH}	I_{SB}	--	--	60	mA
	f = 0MHz, $\overline{CS}$ ≥ V_{CC} - 02V, V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V	I_{SB1}	--	--	10	
Input Capacitance [2]	V_{IN} = 0V, f = 1MHz, T_A = 25 °C.	C_{IN}	--	--	6	pF
Output Capacitance [2]	$V_{I/O}$ = 0V	$C_{I/O}$	--	--	6	pF

1. V_{CC} = 4.5V to 5.5V; V_{SS} = 0V; T_A = -55 to +125 ˚C.

2. Guaranteed by design.

TABLE 4. 32C408B AC CHARACTERISTICS FOR READ CYCLE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Read Cycle Time	t_{RC}				ns
-20		20	--	--	
-25		25	--	--	
-30		30	--	--	
Address Access Time	t_{AA}				ns
-20		--	--	20	
-25		--	--	25	
-30		--	--	30	
Chip Select Access Time	t_{CO}				ns
-20		--	--	20	
-25		--	--	25	
-30		--	--	30	
Output Enable to Output Valid	t_{OE}				
-20		--	--	10	ns
-25		--	--	12	
-30		--	--	14	
Chip Select to Output in Low-Z	t_{LZ}				ns
-20		--	3	--	
-25		--	3	--	
-30		--	3	--	
Output Enable to Output in Low-Z	t_{OLZ}				ns
-20		--	0	--	
-25		--	0	--	
-30		--	0	--	
Chip Deselect to Output in High-Z	t_{HZ}				ns
-20		--	5	--	
-25		--	6	--	
-30		--	8	--	
Output Disable to Output in High-Z	t_{OHZ}				ns
-20		--	5	--	
-25		--	6	--	
-30		--	8	--	
Output Hold from Address Change	t_{OH}				ns
-20		3	--	--	
-25		5	--	--	
-30		5	--	--	
Chip Select to Power Up Time	t_{PU}				ns
-20		--	0	--	
-25		--	0	--	
-30		--	0	--	
Chip Select to Power Down Time	t_{PD}				ns
-20		--	10	--	
-25		--	15	--	
-30		--	20	--	

Table 5. 32408B Functional Description [1]

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

1. X = don't care.

Table 6. 32C408B AC Characteristics for Write Cycle

Parameter	Symbol	Min	Typ	Max	Unit
Write Cycle Time	t_{WC}				ns
-20		20	--	--	
-25		25	--	--	
-30		30	--	--	
Chip Select to End of Write	t_{CW}				ns
-20		14	--	--	
-25		15	--	--	
-30		17	--	--	
Address Setup Time	t_{AS}				ns
-20		0	--	--	
-25		0	--	--	
-30		0	--	--	
Address Valid to End of Write	t_{AW}				ns
-20		14	--	--	
-25		15	--	--	
-30		17	--	--	
Write Pulse Width ($\overline{OE}$ High)	t_{WP}				ns
-20		14	--	--	
-25		15	--	--	
-30		17	--	--	
Write Recovery Time	t_{WR}				ns
-20		0	--	--	
-25		0	--	--	
-30		0	--	--	
Write to Output in High-Z [1]	t_{WHZ}				ns
-20		0	5	10	
-25		0	5	10	
-30		0	6	12	
Data to Write Time Overlap	t_{DW}				ns
-20		8	--	--	
-25		9	--	--	
-30		10	--	--	

TABLE 6. 32C408B AC CHARACTERISTICS FOR WRITE CYCLE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
End Write to Output Low-Z [1]	t_{OW}				ns
-20		4	6	--	
-25		5	7	--	
-30		6	8	--	
Data Hold from Write Time	t_{DH}				ns
-20		0	--	--	
-25		0	--	--	
-30		0	--	--	

1. Guaranteed by design.

FIGURE 1. TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$ CLOCK)

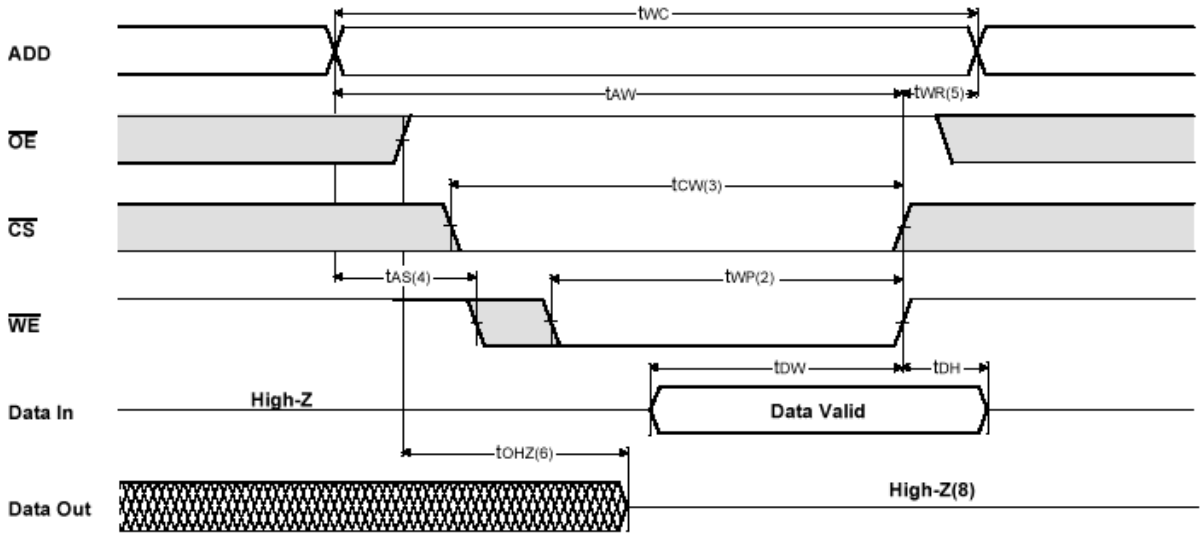
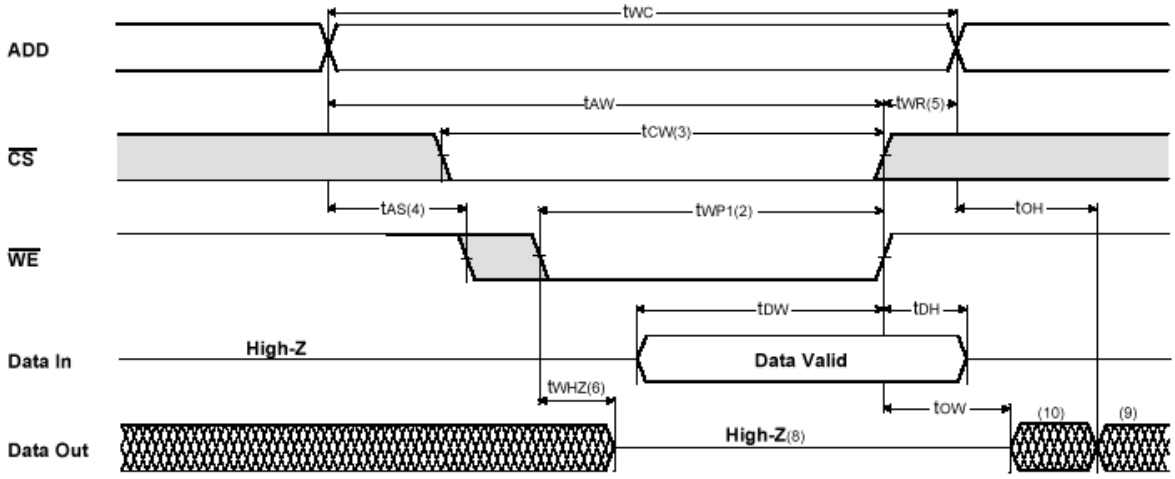


FIGURE 2. TIMING WAVEFORM OF WRITE CYCLE ($\overline{OE}$ LOW FIXED)



1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low: A write ends at the earliest transition among $\overline{CS}$ going high or $\overline{WE}$ going high. t_{WP} is measured from beginning of write to end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. TWR applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. IC $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. D_{OUT} is the read data of the new address.
10. When $\overline{CS}$ is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FIGURE 3. TIMING WAVEFORM OF READ CYCLE(1) (ADDRESS CONTROLLED, $\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})

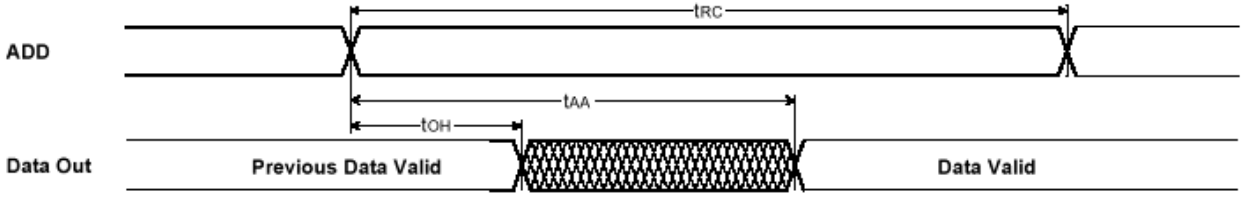
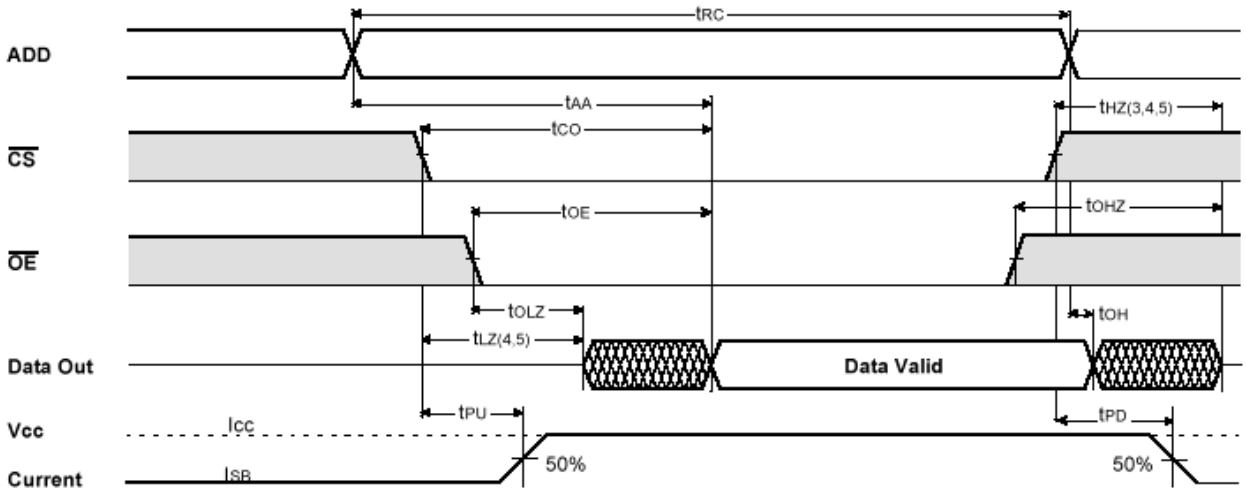


FIGURE 4. TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$ = V_{IH})



1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, $t_{HZ(max)}$ is less than $t_{LZ(min)}$ both for a given device and from device to device.
5. Transition is measured +200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ = V_{IL}.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention is necessary during read and write cycle.

FIGURE 5. SRAM HEAVY ION CROSS SECTION

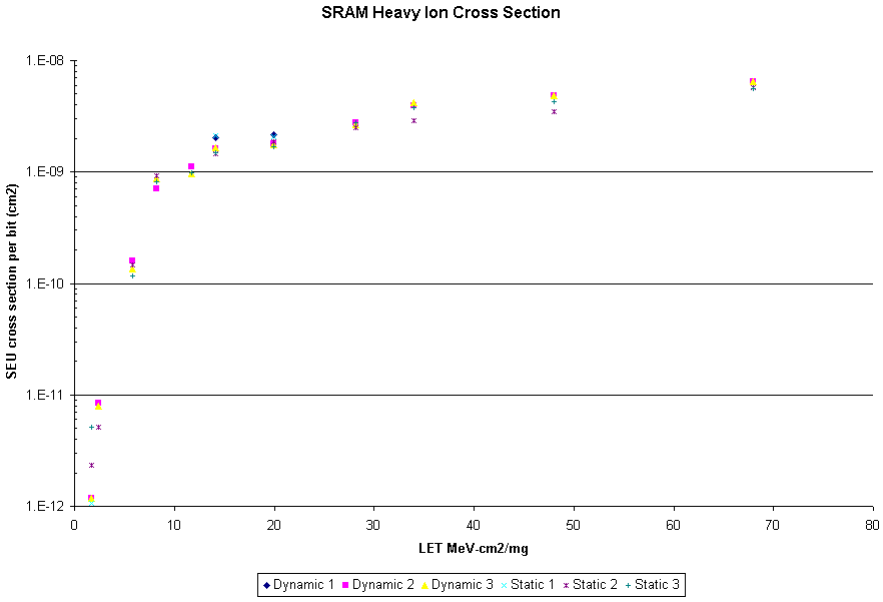
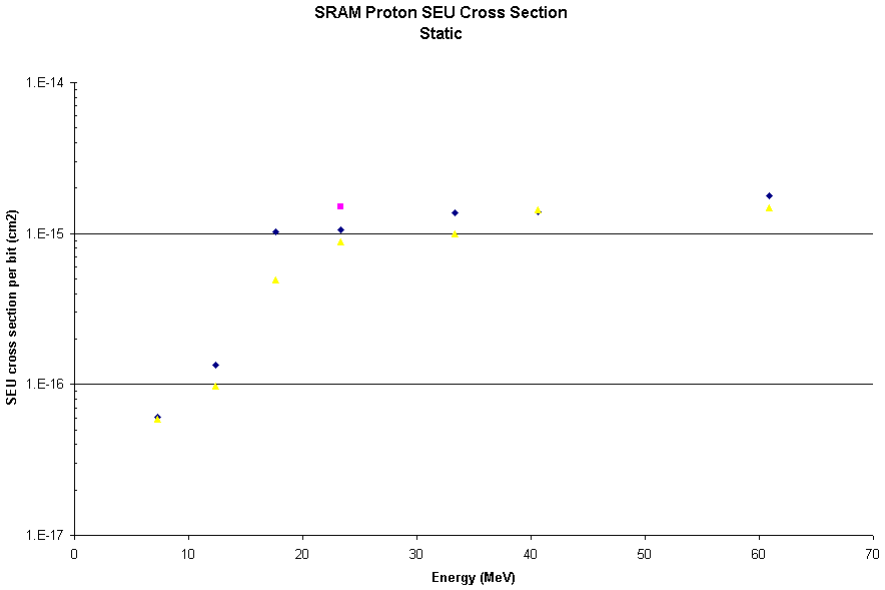
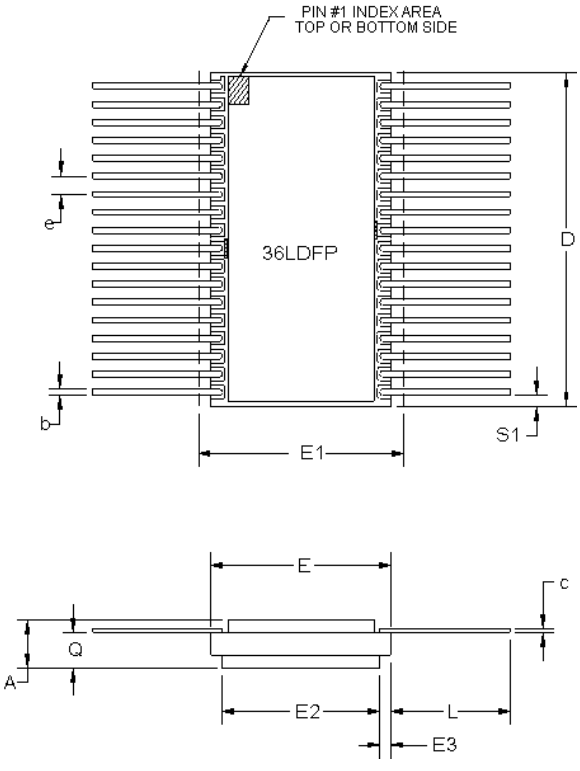


FIGURE 6. SRAM PROTON SEU CROSS SECTION STATIC





36 Pin Flat Rad-Pak® Package

Symbol	Dimension		
	Min	Nom	Max
A	0.122	0.135	0.148
b	0.015	0.017	0.019
c	0.008	0.010	0.012
D	--	0.930	0.940
E	0.638	0.645	0.652
E1	--	--	0.690
E2	0.560	0.565	--
E3	0.005	0.040	--
e	0.050 BSC		
L	0.390	0.400	0.410
Q	0.088	0.098	0.108
S1	0.005	0.032	--
N	36		

F36-01

Note: All dimensions in inches

Important Notice:

These data sheets are created using the chip manufacturers published specifications. Maxwell Technologies verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and Maxwell Technologies assumes no responsibility for the use of this information.

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