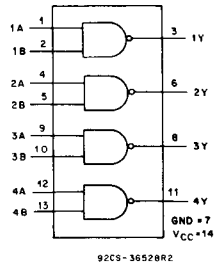
CD54HC03/3A
CD54HCT03/3A

Quad 2-Input NAND Gate

The RCA-CD54HC03 and CD54HCT03 logic gates utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The 54HCT logic family is functionally as well as pin compatible with the standard 54LS logic family. These open-drain NAND gates can drive into resistive loads to output voltages as high as 10 V.



FUNCTIONAL DIAGRAM

Package Specifications

See Section 11, Fig. 10

Static Electrical Characteristics (Limits with black dots (•) are tested 100%) — Complete Specification

CHARACTERISTIC	CD54HC03 TEST CONDITIONS			CD54HC03 LIMITS					CD54HCT03 TEST CONDITIONS		CD54HCT03 LIMITS					UNITS
				+25°C			-55/ +125°C				+25°C			-55/ +125°C		
	V_I V	I_O mA	V_{CC} V	Min.	Typ.	Max.	Min.	Max.	V_I V	V_{CC} V	Min.	Typ.	Max.	Min.	Max.	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	—	4.5 to 5.5	2•	—	—	2•	—	V
			4.5	3.15•	—	—	3.15•	—								
			6	4.2	—	—	4.2	—								
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8•	—	0.8•	V
			4.5	—	—	1.35•	—	1.35•								
			6	—	—	1.8	—	1.8								
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1•	—	0.1•	V
			4.5	—	—	0.1•	—	0.1•								
			6	—	—	0.1	—	0.1								
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26•	—	0.4•	V_{IL} or V_{IH}	4.5	—	—	0.26•	—	0.4•	V
		5.2	6	—	—	0.26	—	0.4								
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1•	—	±1•	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1•	—	±1•	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	2•	—	40•	V_{CC} or Gnd	5.5	—	—	2•	—	40•	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*									V_{CC} -2.1	4.5 to 5.5	—	100	360	—	490	μA
Output Leakage Current I_{OZ}	V_{IL}	V_O = 10 V thru 1 KΩ	6	—	—	0.5•	—	10•	$V_I = V_{IL}$ V_O = 10 V thru 1 KΩ	5.5	—	—	0.5•	—	10•	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

CD54HC03/3A
CD54HCT03/3A

HCT INPUT LOADING TABLE

INPUT	UNIT LOAD*
nA, nB	1

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

Switching Speed (Limits with black dots (•) are tested 100%.)

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS V_{CC} V	LIMITS 25°C HC Min.	HC Max.	HCT Min.	HCT Max.	-55°C to +125°C 54HC Min.	54HC Max.	54HCT Min.	54HCT Max.	UNITS
Propagation Delay Output Low to High Impedance and High Impedance to Output Low	t_{PLZ} t_{PZL}	2	—	100	—	—	—	150	—	—	ns
		4.5	—	20•	—	24•	—	30•	—	36•	
		6	—	17	—	—	—	26	—	—	
Transition Times	t_{THL}	2	—	75	—	—	—	110	—	—	
		4.5	—	15	—	15	—	22	—	22	
		6	—	13	—	—	—	19	—	—	
Input Capacitance	C_I	—	—	10	—	10	—	10	—	10	pF

Burn-In Test-Circuit Connections (Use Static II for /3A burn-in and Dynamic for Life Test.)

Static	STATIC BURN-IN I OPEN	GROUND	V_{CC} (6V)	STATIC BURN-IN II OPEN	GROUND	V_{CC} (6V)
CD54HC/HCT03	3,6,8,11	1,2,4,5,7,9,10,12,13	14	3,6,8,11	7	1,2,4,5,9,10,12-14
Dynamic	**OPEN**	**GROUND**	**1/2 V_{CC} (3V)**	**V_{CC} (6V)**	**OSCILLATOR 50 kHz**	**25 kHz**
CD54HC/HCT03	—	7	3,6,8,11	14	1,2,4,5,9,10, 12,13	—

NOTE: Each pin except V_{CC} and Gnd will have a resistor of 2k-47k ohms.