National Semiconductor

54F/74F550 • 54F/74F551
Octal Registered Transceiver with Status Flags

General Description

The 'F550 and 'F551 octal transceivers each contain two 8-bit registers for temporary storage of data flowing in either direction. Each register has its own clock pulse and clock enable inputs, as well as a flag flip-flop that is set automatically as the register is loaded. Each flag flip-flop is provided with a clear input, and each register has a separate output enable control for its TRI-STATE® buffers. The separate clocks, flags and enables provide considerable flexibility as I/O ports for demand-response data transfer. The 'F550 is non-inverting; the 'F551 inverts data in both directions.

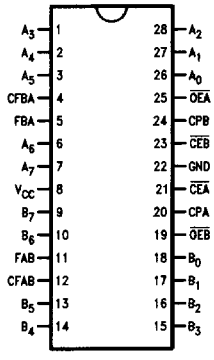
Features

- 8-bit bidirectional I/O port with handshake
- Back-to-back registers for storage
- Register status flag flip-flops
- Separate edge-detecting clears for flags
- Inverting and non-inverting versions
- B outputs sink 64 mA (48 mA Mil)

Ordering Code: See Section 5

Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak 'F550



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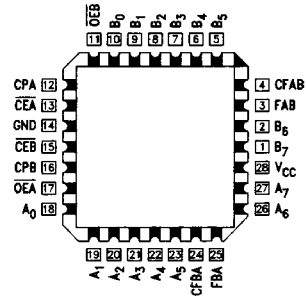
Pin Assignment for LCC 'F550



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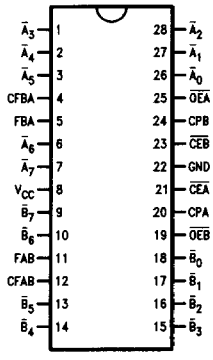
'F551



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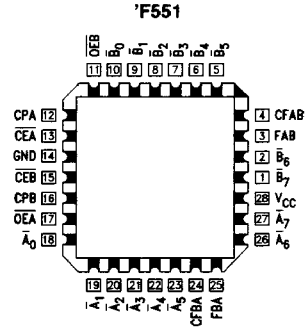
IEEE/IEC

'F551



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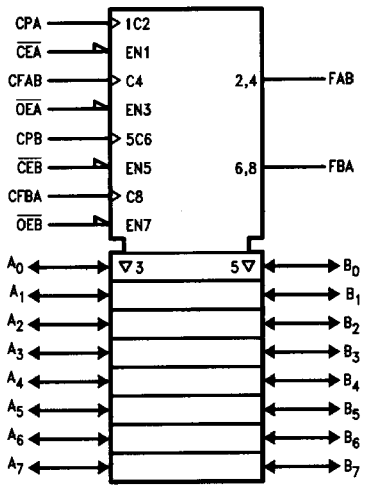
Connection Diagrams (Continued)

'F550



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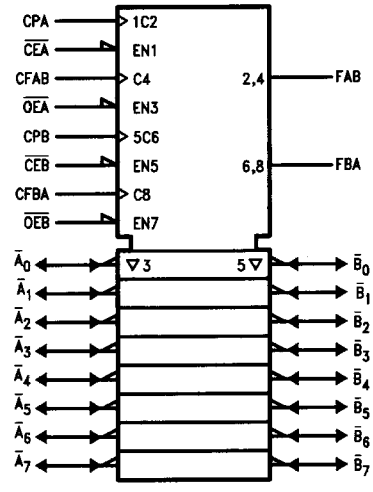
'F551



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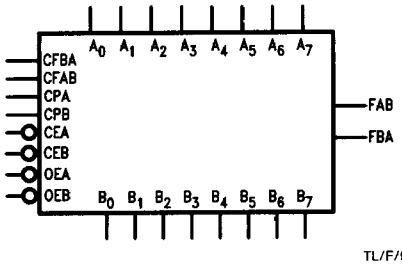
Logic Symbols

'F550



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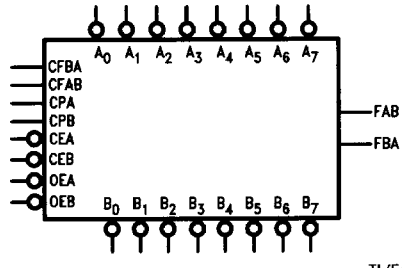
'F551



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Unit Loading/Fan Out: See Section 2 for U.L. definitions

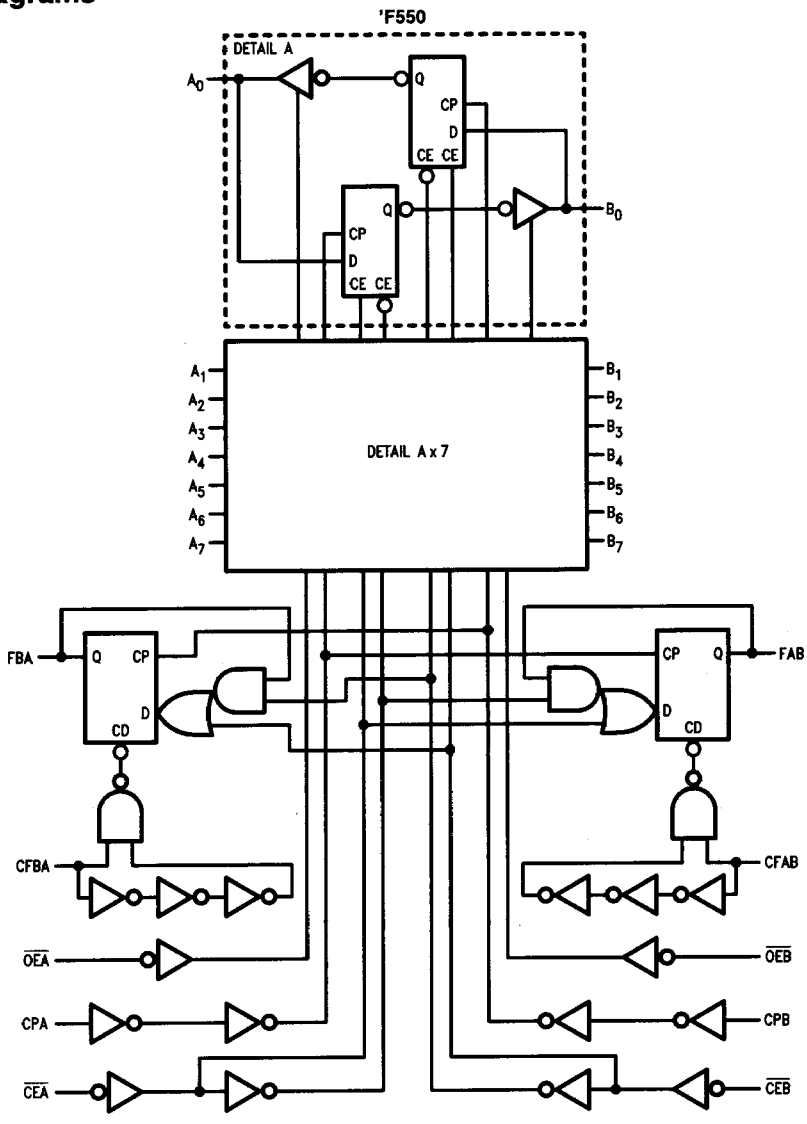
Pin Names	Description	54F/74F U.L. HIGH/LOW	54F/74F Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
CPA	A-to-B Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/−0.6 mA
CPB	B-to-A Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/−0.6 mA
$\overline{CEA}$	A-to-B Clock Enable Input (Active LOW)	1.0/1.0	20 μA/−0.6 mA
$\overline{CEB}$	B-to-A Clock Enable Input (Active LOW)	1.0/1.0	20 μA/−0.6 mA
$\overline{OEA}$	A Output Enable Input (Active LOW)	1.0/1.0	20 μA/−0.6 mA
$\overline{OEB}$	B Output Enable Input (Active LOW)	1.0/1.0	20 μA/−0.6 mA
CFAB	A-to-B Flag Clear Input (Active Rising Edge)	1.0/1.0	20 μA/−0.6 mA
CFBA	B-to-A Flag Clear Input (Active Rising Edge)	1.0/1.0	20 μA/−0.6 mA
A_0–A_7	A-to-B Data Inputs or	3.5/1.083	70 μA/−0.65 mA
	TRI-STATE B-to-A Outputs	150/40 (33.3)	−3 mA/24 mA (20 mA)
B_0–B_7	B-to-A Data Inputs or	3.5/1.083	70 μA/−0.65 mA
	TRI-STATE A-to-B Outputs	600/106.6 (80)	−12 mA/64 mA (48 mA)
FAB	A-to-B Status Flag Output (Active HIGH)	50/33.3	−1 mA/20 mA
FBA	B-to-A Status Flag Output (Active HIGH)	50/33.3	−1 mA/20 mA

Functional Description

Data applied to the A inputs is entered and stored on the rising edge of the A Clock Pulse (CPA), provided that the A Clock Enable ($\overline{CEA}$) is LOW; simultaneously, the status flip-flop is set and the A-to-B flag (FAB) output goes HIGH. Data thus entered from the A inputs is present at the inputs to the B output buffers, but only appears on the B I/O pins when the B Output Enable ($\overline{OEB}$) signal is made LOW. After the B output data is assimilated, the receiving system clears the A-to-B flag flip-flop by applying a LOW-to-HIGH transition to the CFAB input. Optionally, the $\overline{OEB}$ and CFAB pins can be tied together and operated by one function from the receiving system.

Data flow from B-to-A proceeds in the same manner described for A-to-B flow. Inputs $\overline{CEB}$ and CPB enter the B input data and set the B-to-A flag (FBA) output HIGH. A LOW signal on $\overline{OEA}$ enables the A output buffers and a LOW-to-HIGH transition on CFBA clears the FBA flag.

Logic Diagrams



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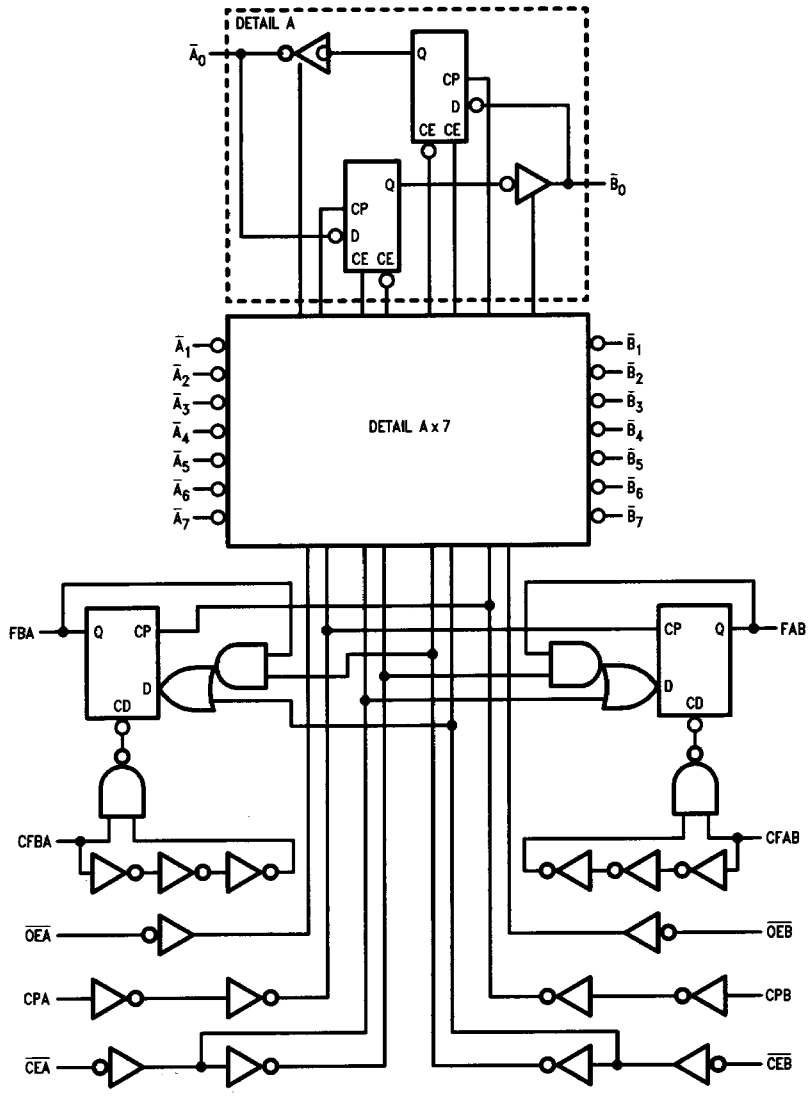
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Logic Diagrams (Continued)

'F551



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA (A_0–A_7)
		54F 10% V_{CC}	2.4					I_{OH} = −3 mA (A_0–A_7)
		54F 10% V_{CC}	2.0					I_{OH} = −12 mA (B_0–B_7)
		74F 10% V_{CC}	2.5					I_{OH} = −1 mA (A_0–A_7)
		74F 10% V_{CC}	2.4					I_{OH} = −3 mA (A_0–A_7)
		74F 10% V_{CC}	2.0					I_{OH} = −15 mA (B_0–B_7)
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA (A_0–A_7)
		74F 5% V_{CC}	2.7					I_{OH} = −3 mA (A_0–A_7)
V_{OL}	Output Low Voltage	54F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA (A_0–A_7)
		54F 10% V_{CC}			0.55			I_{OL} = 48 mA (B_0–B_7)
		74F 10% V_{CC}			0.5			I_{OL} = 24 mA (A_0–A_7)
		74F 10% V_{CC}			0.55			I_{OL} = 64 mA (B_0–B_7)
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	V_{IN} = 2.7V (Non I/O Inputs)
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	V_{IN} = 7.0V (Non I/O Inputs)
		74F			7.0			
I_{BVIT}	Input HIGH Current Breakdown (I/O)	54F			1.0	mA	Max	V_{IN} = 5.5V (A_n, B_n)
		74F			0.5			
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	V_{OUT} = V_{CC}
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V (Non I/O Inputs)
I_{IH} + I_{OZH}	Output Leakage Current				70	μA	Max	V_{OUT} = 2.7V (A_0–A_7, B_0–B_7)
I_{IL} + I_{OZL}	Output Leakage Current				−650	μA	Max	V_{OUT} = 0.5V (A_0–A_7, B_0–B_7)

DC Electrical Characteristics (Continued)

Symbol	Parameter	54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
I_{OS}	Output Short-Circuit Current	−60 −100		−150 −225	mA mA	Max Max	V_{OUT} = 0V (A_0–A_7) V_{OUT} = 0V (B_0–B_7)
I_{ZZ}	Bus Drainage Test			500	μA	0.0V	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current		84	140	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current		105	140	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current		102	140	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF Min	Typ	Max	54F T_A, V_{CC} = Mil, C_L = 50 pF Min	Max	74F T_A, V_{CC} = Com, C_L = 50 pF Min	Max	Units	Fig. No.
t_{PLH} t_{PHL}	Propagation Delay CPA or CPB to B_n or A_n	3.0 4.0	5.5 7.0	7.5 9.0			2.5 3.5	8.5 10.0	ns	2–3
t_{PLH}	Propagation Delay CPA or CPB to FBA or FAB	3.5	6.0	8.0			3.0	9.0	ns	2–3
t_{PHL}	Propagation Delay CFAB or CFBA to FAB or FBA	5.0	9.0	11.5			4.5	13.0	ns	2–3
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	2.5 3.5	5.5 7.0	7.5 9.5			2.0 3.0	8.5 10.5	ns	2–5
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEA}$ or $\overline{OEB}$ to A_n or B_n	3.0 2.5	6.5 5.5	9.0 7.5			2.5 2.0	10.0 8.5		

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F T_A = +25°C, V_{CC} = +5.0V Min	Max	54F T_A, V_{CC} = Mil Min	Max	74F T_A, V_{CC} = Com Min	Max	Units	Fig. No.
t_s(H) t_s(L)	Setup Time, HIGH or LOW A_n, B_n to CPA, CPB	4.0 4.0				4.5 4.5		ns	2–6
t_h(H) t_h(L)	Hold Time, HIGH or LOW A_n, B_n to CPA, CPB	2.0 2.0				2.5 2.5			
t_s(H) t_s(L)	Setup Time, HIGH or LOW $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB	1.0 4.0				1.5 4.5		ns	2–6
t_h(H) t_h(L)	Hold Time, HIGH or LOW $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB	2.0 2.0				2.5 2.5			
t_w(H) t_w(L)	Pulse Width, HIGH or LOW CPA or CPB	3.0 3.0				3.5 3.5		ns	2–4
t_w(H)	Pulse Width, HIGH CFAB or CFBA	3.0				3.5		ns	2–4
t_{rec}	Recovery Time CFAB, CFBA to CPA, CPB	9.0				10.0		ns	2–6