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SEMICONDUCTOR™

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74LVT373 • 74LVTH373
Low Voltage Octal Transparent Latch with 3-STATE Outputs (Preliminary)

General Description

The LVT373 and LVTH373 consist of eight latches with 3-STATE outputs for bus organized system applications. The latches appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data satisfying the input timing requirements is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in a high impedance state.

The LVTH373 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These octal latches are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT373 and LVTH373 are fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining low power dissipation.

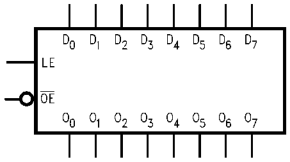
Features

- Input and output interface capability to systems at 5V V_{CC}
- Bus-Hold data inputs eliminate the need for external pull-up resistors to hold unused inputs (74LVTH373), also available without bushold feature (74LVT373).
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink –32 mA/+64 mA
- Functionally compatible with the 74 series 373

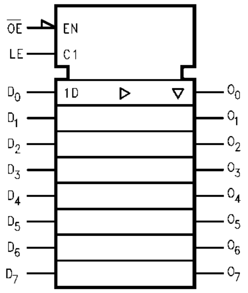
Ordering Code:

Order Number	Package Number	Package Description
74LVT373WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300” Wide
74LVT373SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVT373MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74LVT373MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74LVTH373WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300” Wide
74LVTH373SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVTH373MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74LVTH373MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Logic Symbols



IEEE/IEC



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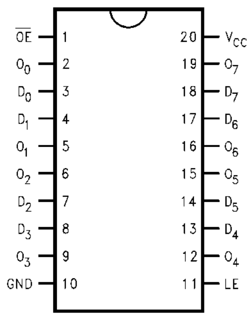
Connection Diagram



$\overline{OE}$ 1
O_0 2
D_0 3
D_1 4
O_1 5
O_2 6
D_2 7
D_3 8
O_3 9
GND 10
20 V_{CC}
19 O_7
18 D_7
17 D_6
16 O_6
15 O_5
14 D_5
13 D_4
12 O_4
11 LE

Pin Descriptions

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
O_0–O_7	3-STATE Latch Outputs

Truth Table

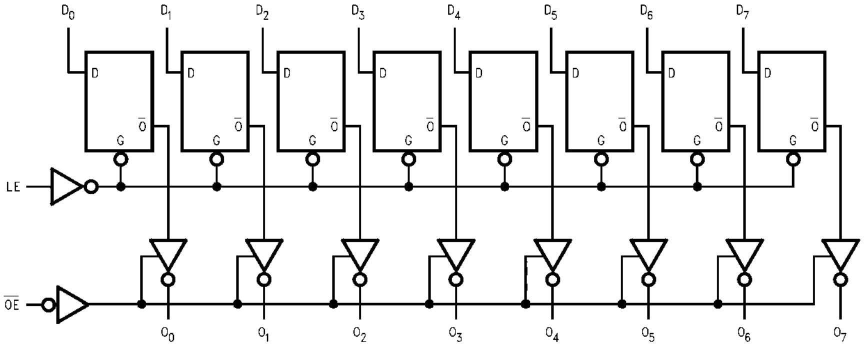
Inputs			Outputs
LE	$\overline{OE}$	D_n	O_n
X	H	X	Z
H	L	L	L
H	L	H	H
L	L	X	O_0

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH-to-LOW transition of Latch Enable

Functional Description

The LVT373 and LVTH373 contain eight D-type latches with 3-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-STATE standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagram



D_0
D_1
D_2
D_3
D_4
D_5
D_6
D_7
D
G
$\overline{O}$
LE
$\overline{OE}$
O_0
O_1
O_2
O_3
O_4
O_5
O_6
O_7

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	–0.5 to +4.6		V
V_I	DC Input Voltage	–0.5 to +7.0		V
V_O	DC Output Voltage	–0.5 to +7.0	Output in 3-STATE	V
		–0.5 to +7.0	Output in HIGH or LOW State (Note 2)	V
I_{IK}	DC Input Diode Current	–50	V_I < GND	mA
I_{OK}	DC Output Diode Current	–50	V_O < GND	mA
I_O	DC Output Current	64	$V_O > V_{CC}$ Output at HIGH State	mA
		128	$V_O > V_{CC}$ Output at LOW State	
I_{CC}	DC Supply Current per Supply Pin	±64		mA
I_{GND}	DC Ground Current per Ground Pin	±128		mA
T_{STG}	Storage Temperature	–65 to +150		°C

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	2.7	3.6	V
V_I	Input Voltage	0	5.5	V
I_{OH}	HIGH Level Output Current		–32	mA
I_{OL}	LOW Level Output Current		64	mA
T_A	Free-Air Operating Temperature	–40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V	0	10	ns/V

Note 1: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

Note 2: I_O Absolute Maximum Rating must be observed.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = -40°C$ to $+85°C$			Units	Conditions
			Min	Typ (Note 3)	Max		
V_{IK}	Input Clamp Diode Voltage	2.7			−1.2	V	$I_I = -18$ mA
V_{IH}	Input HIGH Voltage	2.7–3.6	2.0			V	$V_O \leq 0.1V$ or
V_{IL}	Input LOW Voltage	2.7–3.6			0.8		$V_O \geq V_{CC} - 0.1V$
V_{OH}	Output HIGH Voltage	2.7–3.6	$V_{CC} - 0.2$			V	$I_{OH} = -100$ µA
		2.7	2.4			V	$I_{OH} = -8$ mA
		3.0	2.0			V	$I_{OH} = -32$ mA
V_{OL}	Output LOW Voltage	2.7			0.2	V	$I_{OL} = 100$ µA
		2.7			0.5	V	$I_{OL} = 24$ mA
		3.0			0.4	V	$I_{OL} = 16$ mA
		3.0			0.5	V	$I_{OL} = 32$ mA
		3.0			0.55	V	$I_{OL} = 64$ mA
$I_{I(HOLD)}$ (Note 4)	Bus-Hold Input Minimum Drive	3.0	75			µA	$V_I = 0.8V$
			−75			µA	$V_I = 2.0V$
$I_{I(OD)}$ (Note 4)	Bus-Hold Input Over-Drive Current to Change State	3.0	500			µA	(Note 5)
			−500			µA	(Note 6)
I_I	Input Current	3.6			10	µA	$V_I = 5.5V$
	Control Pins	3.6			±1	µA	$V_I = 0V$ or V_{CC}
	Data Pins	3.6			−5	µA	$V_I = 0V$
					1	µA	$V_I = V_{CC}$
I_{OFF}	Power Off Leakage Current	0			±100	µA	$0V \leq V_I$ or $V_O \leq 5.5V$
$I_{PU/PD}$	Power up/down 3-STATE Output Current	0–1.5V			±100	µA	$V_O = 0.5V$ to $3.0V$ $V_I = $ GND or V_{CC}
I_{OZL}	3-STATE Output Leakage Current	3.6			−5	µA	$V_O = 0.5V$
I_{OZH}	3-STATE Output Leakage Current	3.6			5	µA	$V_O = 3.0V$
$I_{OZH}+$	3-STATE Output Leakage Current	3.6			10	µA	$V_{CC} < V_O \leq 5.5V$
I_{CCH}	Power Supply Current	3.6			0.19	mA	Outputs HIGH
I_{CCL}	Power Supply Current	3.6			5	mA	Outputs LOW
I_{CCZ}	Power Supply Current	3.6			0.19	mA	Outputs Disabled
$I_{CCZ}+$	Power Supply Current	3.6			0.19	mA	$V_{CC} \leq V_O \leq 5.5V$, Outputs Disabled
ΔI_{CC}	Increase in Power Supply Current (Note 7)	3.6			0.2	mA	One Input at $V_{CC} - 0.6V$ Other Inputs at V_{CC} or GND

Note 3: All typical values are at $V_{CC} = 3.3V$, $T_A = 25°C$.

Note 4: Applies to Bushold versions only (74LVTH373).

Note 5: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 6: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

Note 7: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics (Note 8)

Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$			Units	Conditions $C_L = 50$ pF $R_L = 500\Omega$
			Min	Typ	Max		
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	3.3		0.8		V	(Note 9)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	3.3		−0.8		V	(Note 9)

Note 8: Characterized in SOIC package. Guaranteed parameter, but not tested.

Note 9: Max number of outputs defined as (n). n−1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$ $C_L = 50$ pF, $R_L = 500\Omega$					Units
		$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$		
		Min	Typ (Note 10)	Max	Min	Max	
t_{PHL}	Propagation Delay	1.5		3.9	1.5	4.5	ns
t_{PLH}	D_n to O_n	1.5		3.9	1.5	4.5	
t_{PHL}	Propagation Delay	1.7		4.2	1.7	4.9	ns
t_{PLH}	LE to O_n	1.7		4.2	1.7	4.9	
t_{PZL}	Output Enable Time	1.3		4.8	1.3	5.9	ns
t_{PZH}		1.3		4.8	1.3	5.5	
t_{PLZ}	Output Disable Time	1.9		4.6	1.9	4.9	ns
t_{PHZ}		1.9		4.5	1.9	4.6	
t_W	LE Pulse Width	3.0			3.0		ns
t_S	Setup Time, D_n to LE	1.1			0.4		ns
t_H	Hold Time, D_n to LE	1.4			1.4		ns

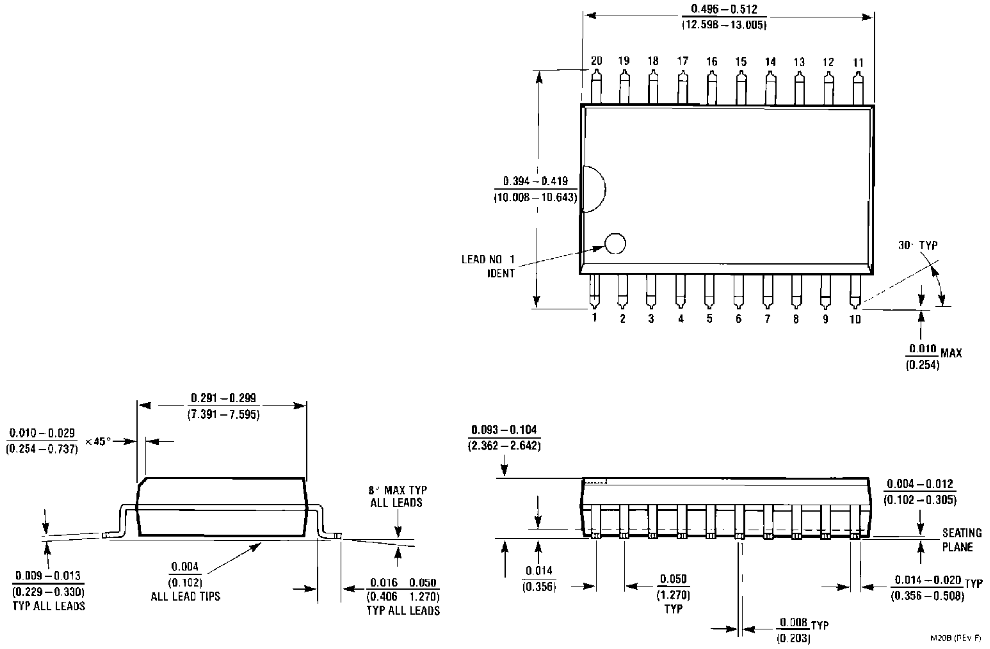
Note 10: All typical values are at $V_{CC} = 3.3V$, $T_A = 25°C$.

Capacitance (Note 11)

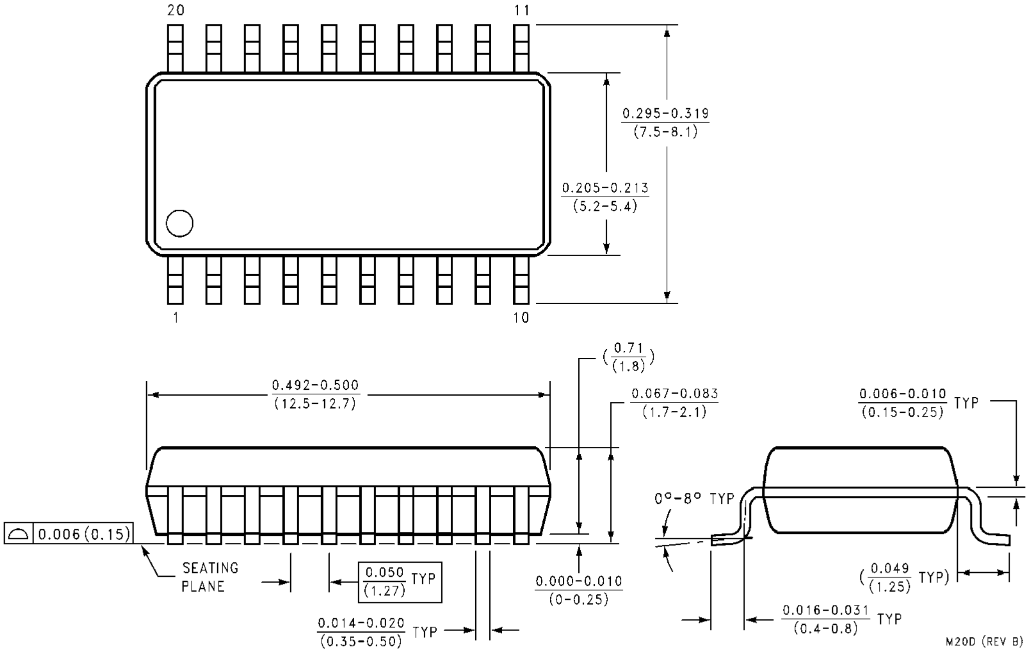
Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	V_{CC} = Open, $V_I = 0V$ or V_{CC}	4	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.0V$, $V_O = 0V$ or V_{CC}	8	pF

Note 11: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

Physical Dimensions inches (millimeters) unless otherwise noted

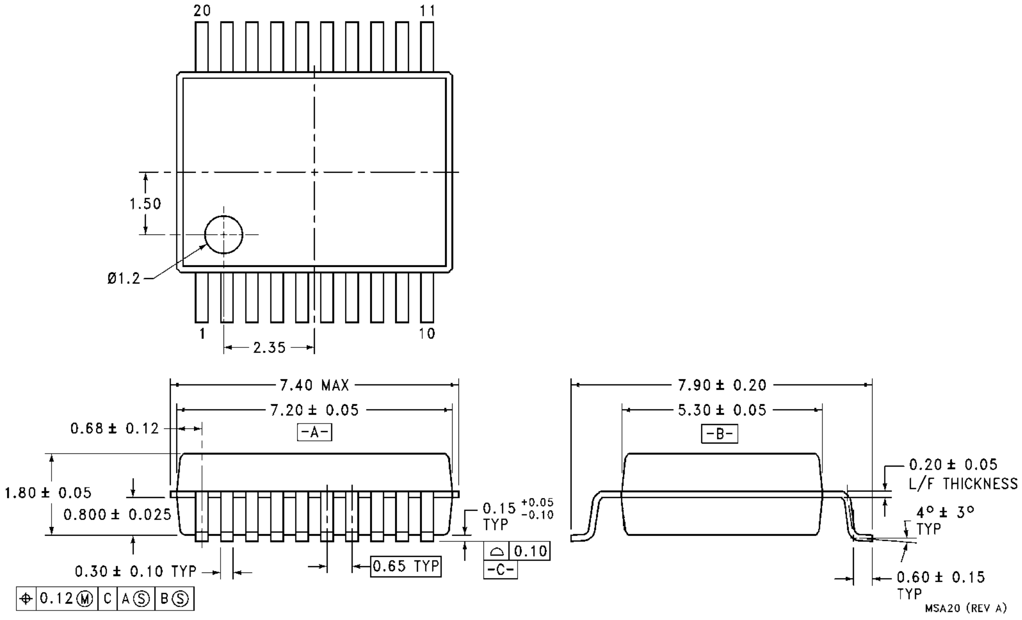

0.496 – 0.512
(12.598 – 13.005)
20 19 18 17 16 15 14 13 12 11
0.394 – 0.419
(10.008 – 10.643)
LEAD NO. 1
IDENT
1 2 3 4 5 6 7 8 9 10
30° TYP
0.010 MAX
(0.254)
0.291 – 0.299
(7.391 – 7.595)
0.010 – 0.029
(0.254 – 0.737)
× 45°
8° MAX TYP
ALL LEADS
0.009 – 0.013
(0.229 – 0.330)
TYP ALL LEADS
0.004
(0.102)
ALL LEAD TIPS
0.016 – 0.050
(0.406 – 1.270)
TYP ALL LEADS
0.093 – 0.104
(2.362 – 2.642)
0.004 – 0.012
(0.102 – 0.305)
SEATING
PLANE
0.014
(0.356)
0.050
(1.270)
TYP
0.014 – 0.020 TYP
(0.356 – 0.508)
0.008 TYP
(0.203)
M20B (REV F)

20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B


20
11
1
10
0.295-0.319
(7.5-8.1)
0.205-0.213
(5.2-5.4)
0.492-0.500
(12.5-12.7)
(0.71/1.8)
0.067-0.083
(1.7-2.1)
0.006-0.010 TYP
(0.15-0.25)
0°-8° TYP
0.006 (0.15)
SEATING
PLANE
0.050 TYP
(1.27)
0.000-0.010
(0-0.25)
0.014-0.020 TYP
(0.35-0.50)
(0.049/1.25 TYP)
0.016-0.031 TYP
(0.4-0.8)
M20D (REV B)

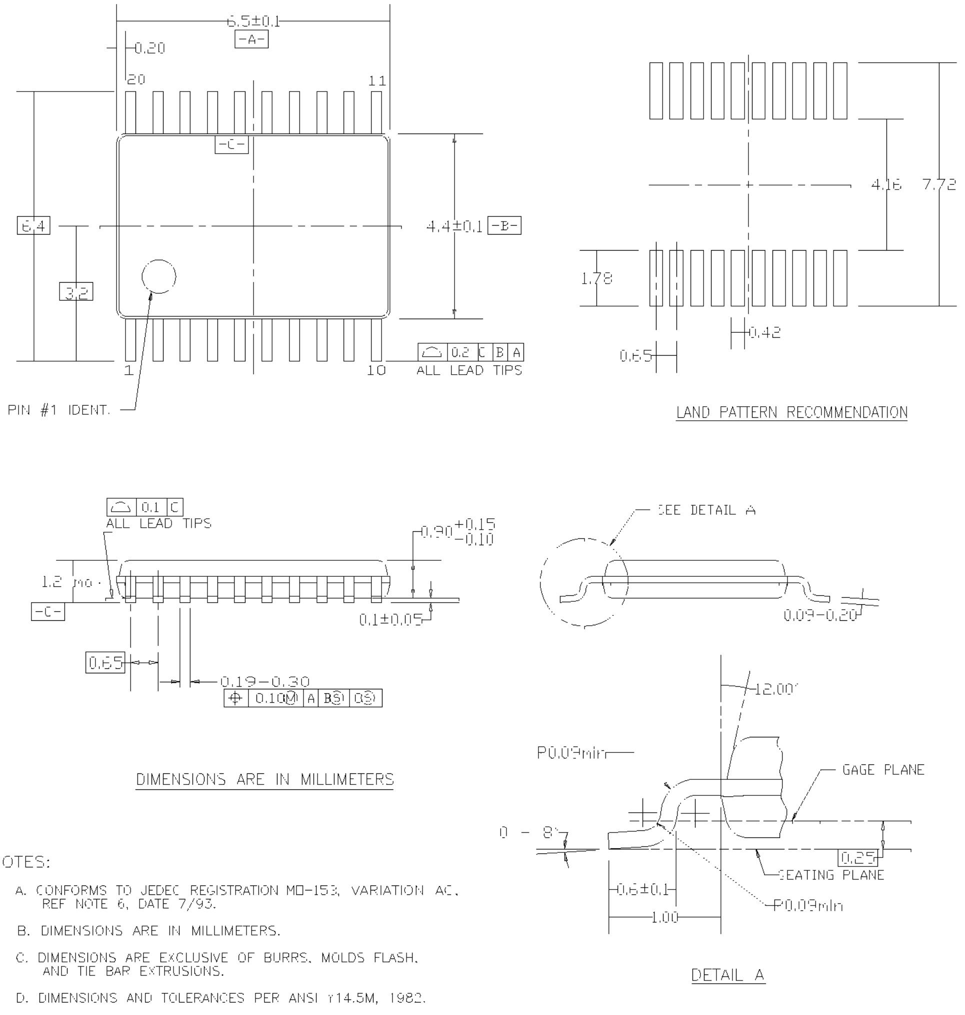
20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)


20
11
1.50
Ø1.2
1
10
2.35
7.40 MAX
7.20 ± 0.05
-A-
0.68 ± 0.12
1.80 ± 0.05
0.800 ± 0.025
0.15 +0.05 -0.10 TYP
0.10
-C-
0.30 ± 0.10 TYP
0.65 TYP
0.12 M C A S B S
7.90 ± 0.20
5.30 ± 0.05
-B-
0.20 ± 0.05 L/F THICKNESS
4° ± 3° TYP
0.60 ± 0.15 TYP
MSA20 (REV A)

20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
Package Number MSA20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)


6.5±0.1
-A-
0.20
20
11
-C-
6.4
3.2
4.4±0.1
-B-
0.2 C B A
ALL LEAD TIPS
1
10
PIN #1 IDENT.
4.16
7.72
1.78
0.42
0.65
LAND PATTERN RECOMMENDATION
0.1 C
ALL LEAD TIPS
0.90 +0.15 −0.10
1.2 MAX
-C-
0.1±0.05
0.65
0.19−0.30
0.10 M A B S C S
DIMENSIONS ARE IN MILLIMETERS
SEE DETAIL A
0.09−0.20
12.00°
R0.09min
GAGE PLANE
0 − 8°
0.25
SEATING PLANE
0.6±0.1
R0.09min
1.00
DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20

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