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Aptos SEMICONDUCTOR

*PRELIMINARY*

# AP9B111/AP9B111L

## 3.3V, 128K x 8 Very High-Speed, Low-Power, CMOS Static RAM with Optional 2V Data Retention

### Features

- Fast access times: 8 and 10ns
- Fast output enable ($t_{DOE}$) for cache applications
- Drives a 50 pF load vs. 30 pF industry-standard load
- Multiple center power and ground pins for improved noise immunity
- 2V/100 µA data retention ("L" version)
- Low active power: 270 mW (Max.) at 10ns
- Low standby current: 7.2 mW (Max.)
- Fully static operation, no clock or refresh required
- TTL and CMOS-compatible inputs and outputs
- Single 3.0 V to 3.6 V power supply
- Packaged in industry-standard 32-Pin, 300-Mil and 400-Mil SOJ

### Functional Description

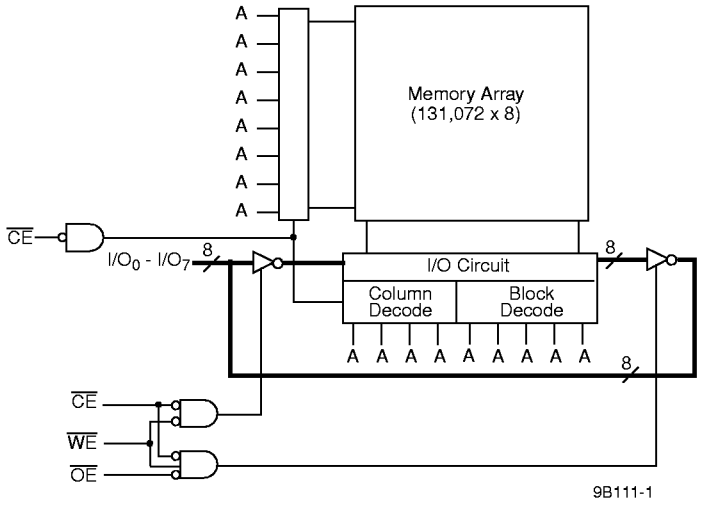
The Aptos AP9B111/AP9B111L is a high-speed, low-power, 128K x 8 CMOS static RAM. It is fabricated using Aptos' high-performance, 0.35µ, CMOS process technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 8 ns (Max.)

When Chip Enable ($\overline{CE}$) is HIGH the device assumes a standby mode at which the power dissipation can be reduced down to 7.2 mW (Max.) at CMOS input levels. At 2V $V_{CC}$, power is reduced to 0.2 mW (Max.) ("L" version).

Easy memory expansion is provided by using asserted LOW $\overline{CE}$ and asserted LOW output enable inputs ($\overline{OE}$). The asserted LOW write enable ($\overline{WE}$) controls both writing and reading of the memory.

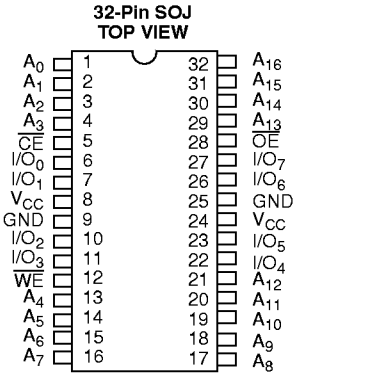
The AP9B111/AP9B111L is pin-compatible with other 3.3V, 128K x 8 center power and ground SRAMs in the SOJ package.

**Block Diagram**




9B111-1

**Pin Configuration**




9B111-2

### Selection Guide

| | AP9B111/L-8 | AP9B111/L-10 |
|---|---|---|
| Maximum Access Time (ns) | 8 | 10 |
| Maximum Operating Current (mA) | 85 | 75 |
| Maximum Standby Current (mA) | 2 | 2 |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65 °C to +150 °C

Ambient Temperature with Power Applied ..... -55 °C to +125 °C

$V_{CC}$ Supply Relative to GND ..... -0.5V to +7.0V

Voltage on Any Pin Relative to GND ..... -0.5V to $V_{CC}$ +0.5V

Short Circuit Output Current [1] ..... ±20 mA

Power Dissipation ..... 1.0 W

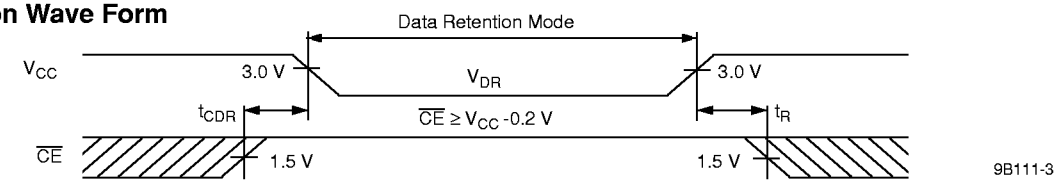
## Electrical Characteristics Over the Operating Range ($0°C \le T_A \le 70°C$, $V_{CC}$ = 3.0 V Min. to 3.6 V Max.)

| Symbol | Parameter | Test Conditions | 9B111/L-8 | | 9B111/L-10 | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| $I_{CC1}$ | Dynamic Operating Current [2] | $V_{CC}$ = Max., $I_{OUT}$ = 0 mA, $\overline{CE} = V_{IL}$, f = fmax. | | 85 | | 75 | mA |
| $I_{CC2}$ | Operating Current [2] | $V_{CC}$ = Max., $I_{OUT}$ = 0 mA, $\overline{CE} = V_{IL}$, f = 0 | | 50 | | 50 | mA |
| $I_{SB1}$ | TTL Standby Current -TTL Inputs | $V_{CC}$ = Max., $V_{IN} = V_{IH}$ or $V_{IL}$, $\overline{CE} \ge V_{IH}$, f=fmax. | | 25 | | 20 | mA |
| $I_{SB2}$ | CMOS Standby Current -CMOS Inputs | $V_{CC}$ = Max., $\overline{CE} \ge V_{CC}$ -0.2 V, $V_{IN} \ge V_{CC}$ -0.2 V or $V_{IN} \le 0.2$ V, f = 0 | | 2 | | 2 | mA |
| $I_{LI}$ | Input Leakage Current | $GND \le V_{IN} \le V_{CC}$ | -1 | 1 | -1 | 1 | µA |
| $I_{LO}$ | Output Leakage Current | $GND \le V_{OUT} \le V_{CC}$, Output Disabled | -1 | 1 | -1 | 1 | µA |
| $V_{OH}$ | Output High Voltage | $V_{CC}$ = Min., $I_{OH}$ = - 4.0 mA | 2.4 | | 2.4 | | V |
| $V_{OL}$ | Output Low Voltage | $V_{CC}$ = Min., $I_{OL}$ = 8.0 mA | | 0.4 | | 0.4 | V |
| $V_{IH}$ | Input High Voltage [3] | | 2.0 | $V_{CC}$ +0.3 | 2.0 | $V_{CC}$ +0.3 | V |
| $V_{IL}$ | Input Low Voltage [3] | | -0.3 | 0.8 | -0.3 | 0.8 | V |

## Data Retention Characteristics ("L" Version)

| Symbol | Description | Test Conditions [4] | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for Data Retention | $V_{CC} = V_{DR}$ = 2.0 V, $\overline{CE} \ge V_{CC}$-0.2 V, $V_{IN} \ge V_{CC}$-0.2 V or $V_{IN} \le 0.2$ V | 2.0 | | V |
| $I_{CCDR}$ | Data Retention Current | | | 100 | µA |
| $t_{CDR}$ | Chip Deselect to Data Retention Time | | 0 | | ns |
| $t_R$ | Operation Recovery Time | | $t_{RC}$ | | ns |

### Data Retention Wave Form




**Notes:**

1. No more than one output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
2. $I_{CC}$ is dependent upon output loading and cycle rates. Specified values are with outputs open.
3. $V_{IL}$ undershoot = -1.0V where $t=t_{RC}/4$ per cycle. $V_{IH}$ overshoot = $V_{CC}$ +1.0V where $t=t_{RC}/4$ per cycle.
4. No input may exceed $V_{CC}$ +0.3 V (DC).
5. Tested initially and after any design or process changes that may effect these parameters.

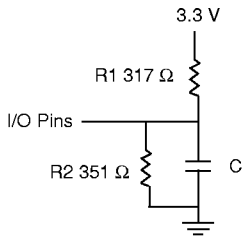
## Capacitance [5]

| Symbol | Description | Max. | Unit |
|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 5 | pF |
| $C_{IO}$ | I/O Capacitance | 5 | pF |

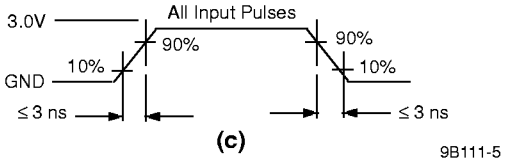
### AC Test Loads and Waveforms

**(a)** $C_1$= 50 pF INCLUDING JIG AND SCOPE

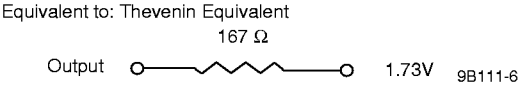
**(b)** $C_2$=5 pF INCLUDING JIG AND SCOPE




9B111-4




9B111-5




9B111-6

## Switching Characteristics Over the Operating Range [6, 7]

| Parameter | Description | 9B111/L-8 | | 9B111/L-10 | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| *Read Cycle* [8] | | | | | | |
| $t_{RC}$ | Read Cycle Time | 8 | | 10 | | ns |
| $t_{AA}$ | Address Access Time | | 8 | | 10 | ns |
| $t_{OHA}$ | Output Hold Time | 3 | | 3 | | ns |
| $t_{ACE}$ | $\overline{CE}$ Access Time | | 8 | | 10 | ns |
| $t_{DOE}$ | $\overline{OE}$ Access Time | | 3 | | 4 | ns |
| $t_{LZOE}$ [9] | $\overline{OE}$ to Low-Z Output | 0 | | 0 | | ns |
| $t_{HZOE}$ [9] | $\overline{OE}$ to High-Z Output | | 3 | | 4 | ns |
| $t_{LZCE}$ [9] | $\overline{CE}$ to Low-Z Output | 3 | | 3 | | ns |
| $t_{HZCE}$ [9] | $\overline{CE}$ to High-Z Output | | 3 | | 4 | ns |
| $t_{PU}$ | $\overline{CE}$ to Power Up | 0 | | 0 | | ns |
| $t_{PD}$ | $\overline{CE}$ to Power Down | | 8 | | 10 | ns |
| *Write Cycle* [10] | | | | | | |
| $t_{WC}$ | Write Cycle Time | 8 | | 10 | | ns |
| $t_{SCE}$ | $\overline{CE}$ to Write End | 7 | | 8 | | ns |
| $t_{AW}$ | Address Set-up Time to Write End | 7 | | 8 | | ns |
| $t_{HA}$ | Address Hold to Write End | 0 | | 0 | | ns |
| $t_{SA}$ | Address Set-up Time to Write Start | 0 | | 0 | | ns |
| $t_{PWE1}$ [11] | $\overline{WE}$ Pulse Width ($\overline{OE}$ = HIGH) | 7 | | 8 | | ns |
| $t_{PWE2}$ | $\overline{WE}$ Pulse Width ($\overline{OE}$ = LOW) | 8 | | 10 | | ns |
| $t_{SD}$ | Data Set-up to Write End | 5 | | 6 | | ns |
| $t_{HD}$ | Data Hold from Write End | 0 | | 0 | | ns |
| $t_{HZWE}$ [9] | $\overline{WE}$ LOW to High-Z Output | | 3 | | 5 | ns |
| $t_{LZWE}$ [9] | $\overline{WE}$ HIGH to Low-Z Output | 2 | | 2 | | ns |

**Notes:**

6. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V and output loading specified in AC Test Loads and Waveforms *Figure (a)* unless otherwise noted.
7. I/O will assume the High-Z state if $\overline{OE} \geq V_{IH}$.
8. $\overline{WE}$ is HIGH for a Read Cycle.
9. Tested with the load in AC Test Loads and Waveforms *Figure (b)*. Transition is measured ±500mV from steady state voltage.
10. The internal write time is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The Data Input Set-up and Hold timing is referenced to the rising or falling edge of the signal that terminates the write.
11. Tested with $\overline{OE}$ HIGH for a minimum of 4 ns before $\overline{WE}$ = LOW to place I/O in High-Z state.
12. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = $V_{IL}$.
13. Address is valid prior to, or coincident with, $\overline{CE}$ LOW transitions.
14. At any given temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$ and $t_{HZOE}$ is less than $t_{LZOE}$.

## Pin Descriptions

### $A_0$ - $A_{16}$: Address Inputs

These 17 address inputs select one of the 131,072 8-bit words in the RAM.

### $\overline{CE}$: Chip Enable Input

$\overline{CE}$ is asserted LOW. The Chip Enable is asserted LOW to read from or write to the device. If Chip Enable is deasserted, the device is deselected and is in a standby power mode. The I/O pins will be in the High-Z state when the device is deselected.

### $\overline{OE}$: Output Enable Input

The Output Enable input is asserted LOW. If the Output Enable is asserted LOW while $\overline{CE}$ is asserted (LOW) and $\overline{WE}$ is deasserted (HIGH), data from the SRAM will be present on the I/O pins. The I/O pins will be in the High-Z state when $\overline{OE}$ is deasserted.

### $\overline{WE}$: Write Enable Input

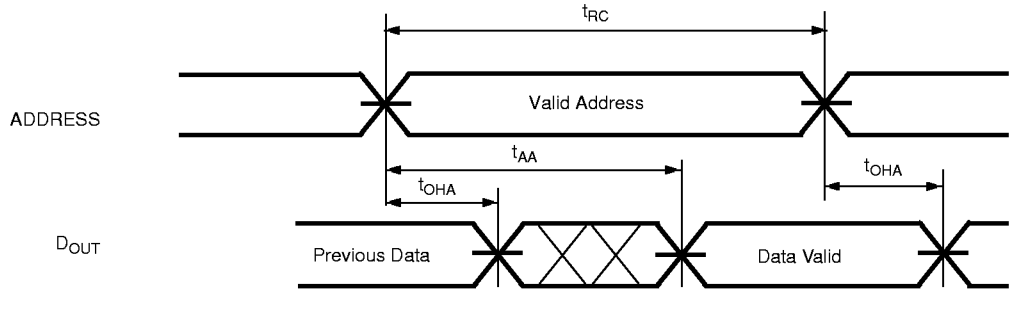
The Write Enable input is asserted LOW and controls read and write operations. When $\overline{CE}$ and $\overline{WE}$ are both asserted (LOW) input data present on the I/O pins will be written into the selected memory location.

### $I/O_0$ - $I/O_7$: Common Input/Output Pins

### GND: Ground

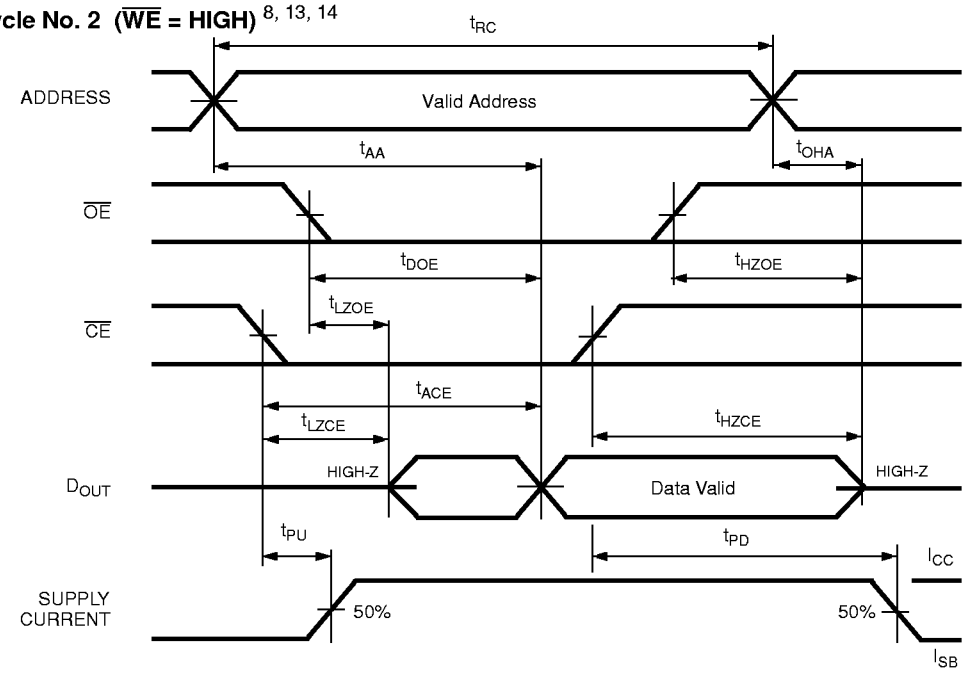
## Switching Waveforms

**Read Cycle No. 1 ($\overline{CE}$ = LOW, $\overline{OE}$ = LOW, $\overline{WE}$ = HIGH)** [8, 12]




9B111-7

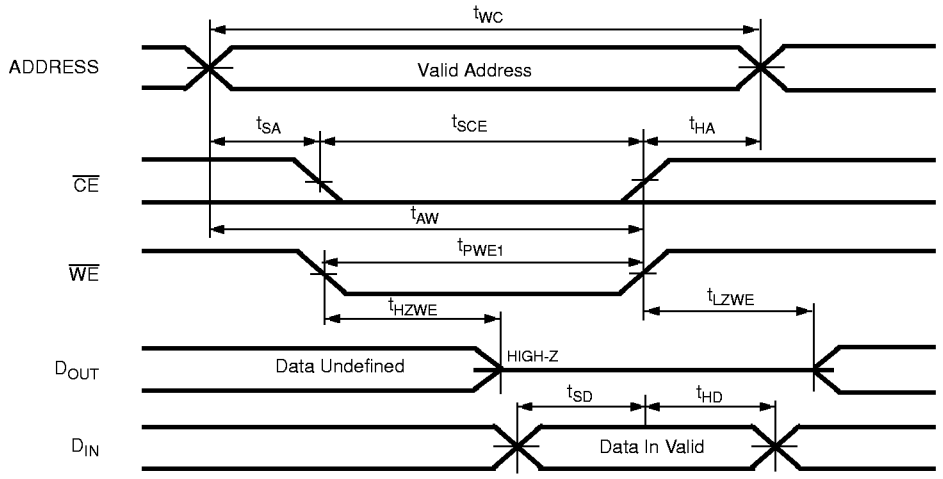
**Read Cycle No. 2 ($\overline{WE}$ = HIGH)** [8, 13, 14]




9B111-8

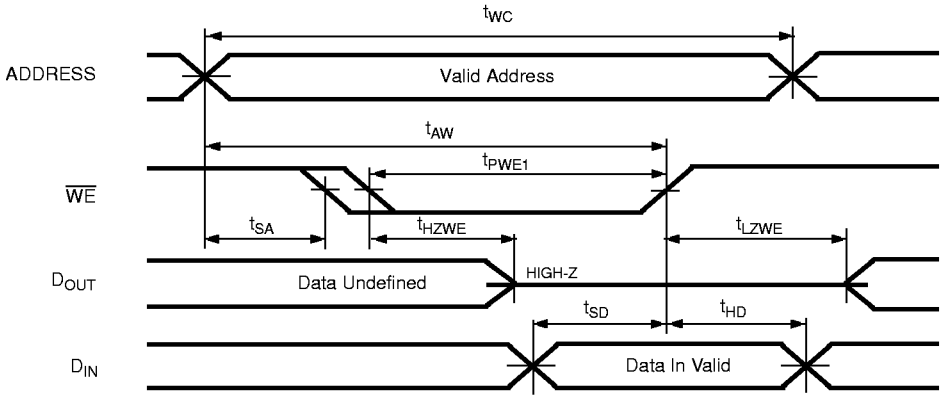
## Switching Waveforms (continued)

### Write Cycle No.1 ($\overline{CE}$ controlled, $\overline{OE}$ is HIGH or LOW: $\overline{CE}$ Terminates Write) [10]



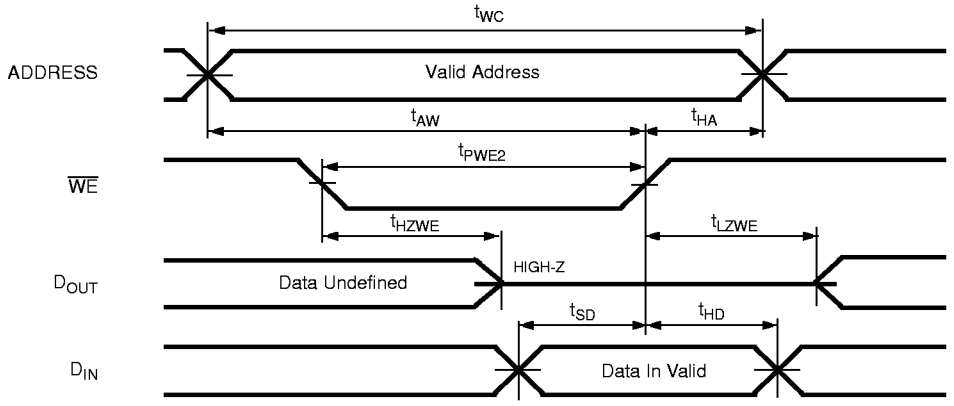

9B111-9

### Write Cycle No.2 ($\overline{WE}$ controlled, $\overline{OE}$ is HIGH, $\overline{CE}$ is LOW: $\overline{WE}$ Terminates Write) [10]




9B111-10

### Write Cycle No.3 ($\overline{WE}$ controlled, $\overline{OE}$ is LOW, $\overline{CE}$ is LOW: $\overline{WE}$ Terminates Write) [10]




9B111-11

## Truth Table

| Mode | $\overline{WE}$ | $\overline{CE}$ | $\overline{OE}$ | I/O | $I_{CC}$ |
|---|---|---|---|---|---|
| Standby | X | H | X | High-Z | $I_{SB1}$, $I_{SB2}$ |
| Selected/Output Disabled | H | L | H | High-Z | $I_{CC1}$, $I_{CC2}$ |
| Read | H | L | L | $D_{OUT}$ | $I_{CC1}$, $I_{CC2}$ |
| Write | L | L | X | $D_{IN}$ | $I_{CC1}$, $I_{CC2}$ |

## Ordering Information

*Standard - AP9B111*

| Speed | Part Number | Package Name | Package Type | Temperature Range |
|---|---|---|---|---|
| 8 | AP9B111-8VC | V32.1 | 32-Pin (400-Mil) Small Outline J-Bend | Commercial |
| | AP9B111-8V3C | V32.2 | 32-Pin (300-Mil) Small Outline J-Bend | |
| 10 | AP9B111-10VC | V32.1 | 32-Pin (400-Mil) Small Outline J-Bend | |
| | AP9B111-10V3C | V32.2 | 32-Pin (300-Mil) Small Outline J-Bend | |

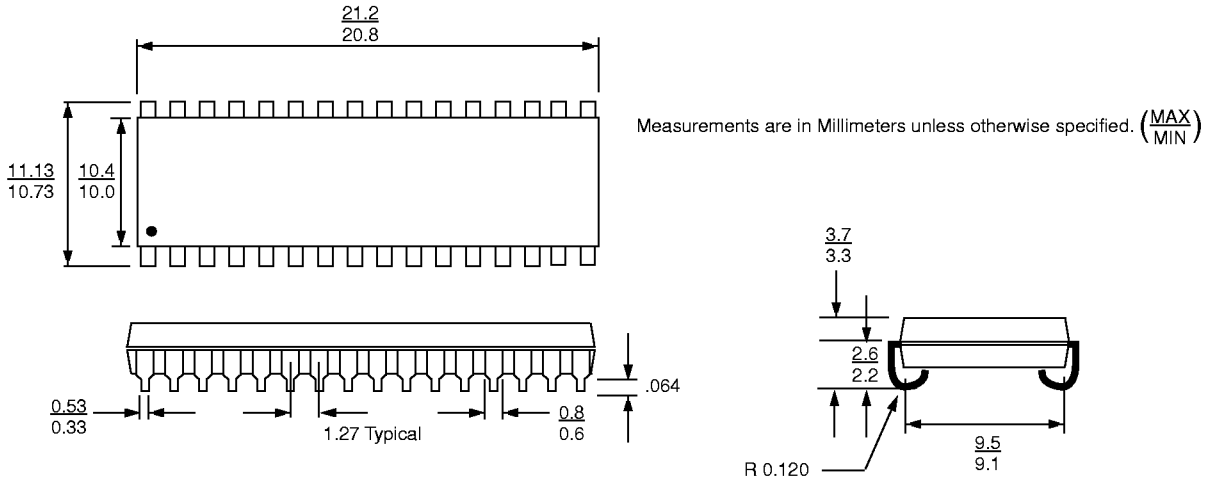
*With Optional 2V Data Retention - AP9B111L*

| Speed | Part Number | Package Name | Package Type | Temperature Range |
|---|---|---|---|---|
| 8 | AP9B111L-8VC | V32.1 | 32-Pin (400-Mil) Small Outline J-Bend | Commercial |
| | AP9B111L-8V3C | V32.2 | 32-Pin (300-Mil) Small Outline J-Bend | |
| 10 | AP9B111L-10VC | V32.1 | 32-Pin (400-Mil) Small Outline J-Bend | |
| | AP9B111L-10V3C | V32.2 | 32-Pin (300-Mil) Small Outline J-Bend | |

Document # DS-00074-Rev *

## Package Diagrams

### V32.1 - 32-Pin (400-Mil) Small Outline J-Bend (SOJ)




### V32.2 - 32-Pin (300-Mil) Small Outline J-Bend (SOJ)