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DS36276
FAILSAFE Multipoint Transceiver

General Description

The DS36276 FAILSAFE Multipoint Transceiver is designed for use on bi-directional differential busses. It is compatible with existing TIA/EIA-485 transceivers, however, it offers an additional feature not supported by standard transceivers.

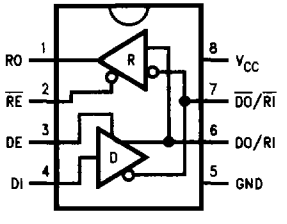
The FAILSAFE feature guarantees the receiver output to a known state when the Interface is in the following conditions: Floating Line, Idle Line (no active drivers), and Line Fault conditions (open or short). The receiver output is in a HIGH state for the following conditions: OPEN Inputs, Terminated Inputs (50Ω), and SHORTED Inputs.

FAILSAFE is a highly desirable feature when the transceivers are used with Asynchronous Controllers such as UARTs.

Features

- FAILSAFE receiver, RO = HIGH for:
  - — OPEN inputs
  - — Terminated inputs
  - — SHORTED inputs
- Compatible with popular interface standards:
  - — TIA/EIA-485 (RS-485)
  - — TIA/EIA-422-A (RS-422-A)
  - — CCITT Recommendation V.11
- Bi-Directional Transceiver
  - — Designed for multipoint transmission
- Separate driver input, driver enable, receiver enable, and receiver output for maximum flexibility
- Wide bus common mode range
  - — (−7V to +12V)
- Pin compatible with: DS75176B, DS96176, DS3695 and SN75176A and B
- Available in plastic DIP and SOIC packages

Connection and Logic Diagram



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Order Number DS36276N or DS36276M
See NS Package Number N08E or M08A

Truth Tables

Driver

Inputs			Outputs	
$\overline{RE}$	DE	DI	DO/RI	$\overline{DO}/\overline{RI}$
X	H	H	H	L
X	H	L	L	H
X	L	X	Z	Z

Receiver

Inputs			Output
$\overline{RE}$	DE	RI−$\overline{RI}$	RO
L	L	≥0V	H
L	L	≤−500 mV	L
H	X	X	Z

Receiver FAILSAFE

Inputs			Output
$\overline{RE}$	DE	RI−$\overline{RI}$	RO
L	L	SHORTED	H
L	L	OPEN	H
H	X	X	Z

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Input Voltage (DE, $\overline{RE}$, DI)	5.5V
Driver Output Voltage/ Receiver Input Voltage	−10V to +15V
Receiver Output Voltage (RO)	5.5V
Maximum Package Power Dissipation @ +25°C	
N Package (derate 9.3 mW/°C above +25°C)	1168 mW
M Package (derate 5.8 mW/°C above +25°C)	726 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 4 sec.)	260°C
Max Junction Temperature	150°C
ESD Rating (HBM, 1.5 kΩ, 100 pF)	≥ 6.0 kV

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Bus Voltage	−7	+12	V
Operating Temperature (T_A) DS36276	0	+70	°C

Electrical Characteristics

Over recommended Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Notes 2, 4)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DRIVER CHARACTERISTICS							
V_{OD}	Differential Output Voltage	I_O = 0 mA (No Load)		1.5	4.8	6.0	V
V_{oDO}	Output Voltage	I_O = 0 mA (Output to GND)		0		6.0	V
$V_{o\overline{DO}}$	Output Voltage			0		6.0	V
V_{T1}	Differential Output Voltage (Termination Load)	R_L = 54Ω (485)	*(Figure 1)*	1.5	2.0	5.0	V
		R_L = 100Ω (422)		2.0	2.3	5.0	V
ΔV_{T1}	Balance of V_{T1} $\lvert V_{T1}\rvert - \lvert\overline{V_{T1}}\rvert$	R_L = 54Ω	(Note 3)	−0.2	0.07	+0.2	V
		R_L = 100Ω		−0.2	0.07	+0.2	V
V_{OS}	Driver Common Mode Output Voltage	R_L = 54Ω	*(Figure 1)*	0	2.5	3.0	V
		R_L = 100Ω		0	2.3	3.0	V
ΔV_{OS}	Balance of V_{OS} $\lvert V_{OS}\rvert - \lvert\overline{V_{OS}}\rvert$	R_L = 54Ω	(Note 3)	−0.2	0.08	+0.2	V
		R_L = 100Ω		−0.2	0.08	+0.2	V
I_{OSD}	Driver Short-Circuit Output Current	V_O = +12V	*(Figure 3)*		134	290	mA
		V_O = V_{CC}			140		mA
		V_O = 0V			−140		mA
		V_O = −7V			−180	−290	mA

Electrical Characteristics (Continued)

Over recommended Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Notes 2, 4)

Symbol	Parameter	Conditions			Min	Typ	Max	Units
RECEIVER CHARACTERISTICS								
V_{TH}	Differential Input High Threshold Voltage (Note 5)	$V_O = V_{OH}$, $I_O = -0.4$ mA $-7V \le V_{CM} \le +12V$				-0.18	0	V
V_{TL}	Differential Input Low Threshold Voltage (Note 5)	$V_O = V_{OL}$, $I_O = 8.0$ mA $-7V \le V_{CM} \le +12V$			-0.5	-0.23		V
V_{HST}	Hysteresis (Note 6)	$V_{CM} = 0V$				50		mV
I_{IN}	Line Input Current (V_{CC} = 4.75V, 5.25V, 0V)	Other Input = 0V, DE = V_{IH} (Note 7)	$V_I = +12V$			0.7	1.0	mA
			$V_I = -7V$			-0.5	-0.8	mA
I_{OSR}	Short Circuit Current	$V_O = 0V$		RO	-5.0	-30	-85	mA
I_{OZ}	TRI-STATE® Leakage Current	$V_O = 0.4$ to 2.4V			-20		$+20$	μA
V_{OH}	Output High Voltage *(Figure 12)*	$V_{ID} = 0V$, $I_{OH} = -0.4$ mA			2.5	3.5		V
		V_{ID} = OPEN, $I_{OH} = -0.4$ mA			2.5	3.5		V
V_{OL}	Output Low Voltage *(Figure 12)*	$V_{ID} = -0.5V$, $I_{OL} = +8$ mA				0.25	0.6	V
		$V_{ID} = -0.5V$, $I_{OL} = +16$ mA				0.35	0.7	V
R_{IN}	Input Resistance				12	19		kΩ
DEVICE CHARACTERISTICS								
V_{IH}	High Level Input Voltage			DE, $\overline{RE}$, or DI	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage				GND		0.8	V
I_{IH}	High Level Input Current	$V_{IH} = 2.4V$					20	μA
I_{IL}	Low Level Input Current	$V_{IL} = 0.4V$					-100	μA
V_{CL}	Input Clamp Voltage	$I_{CL} = -18$ mA				-0.75	-1.5	V
I_{CC}	Output Low Voltage Supply Current (No Load)	DE = 3V, $\overline{RE}$ = 0V, DI = 0V				42	60	mA
I_{CCR}		DE = 0V, $\overline{RE}$ = 0V, DI = 0V				28	45	mA
I_{CCD}		DE = 3V, $\overline{RE}$ = 3V, DI = 0V				43	60	mA
I_{CCX}		DE = 0V, $\overline{RE}$ = 3V, DI = 0V				31	50	mA

Switching Characteristics

Over recommended Supply Voltage and Operating Temperature ranges, unless otherwise specified. (Note 4)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER CHARACTERISTICS						
t_{PLHD}	Diff. Prop. Delay Low to High	$R_L = 54\Omega$ $C_L = 50$ pF $C_D = 50$ pF *(Figures 4, 5)*	7	21	60	ns
t_{PHLD}	Diff. Prop. Delay High to Low		7	19	60	ns
t_{SKD}	Diff. Skew ($\lvert t_{PLHD} - t_{PHLD} \rvert$)			2	10	ns
t_r	Diff. Rise Time			12	50	ns
t_f	Diff. Fall Time			12	50	ns
t_{PLH}	Prop. Delay Low to High	$R_L = 27\Omega$, $C_L = 15$ pF *(Figures 6, 7)*		22	45	ns
t_{PHL}	Prop. Delay High to Low			22	45	ns
t_{PZH}	Enable Time Z to High	$R_L = 110\Omega$ $C_L = 50$ pF *(Figures 8–11)*		32	55	ns
t_{PZL}	Enable Time Z to Low			32	65	ns
t_{PHZ}	Disable Time High to Z			22	55	ns
t_{PLZ}	Disable Time Low to Z			16	55	ns
RECEIVER CHARACTERISTICS						
t_{PLH}	Prop. Delay Low to High	$V_{ID} = -1.5$V to $+1.5$V $C_L = 15$ pF *(Figures 13, 14)*	15	40	70	ns
t_{PHL}	Prop. Delay High to Low		15	42	70	ns
t_{SK}	Skew ($\lvert t_{PLH} - t_{PHL} \rvert$)			2	15	ns
t_{PZH}	Enable Time Z to High	$C_L = 15$ pF *(Figures 15, 16)*		15	50	ns
t_{PZL}	Enable Time Z to Low			17	50	ns
t_{PHZ}	Disable Time High to Z			24	50	ns
t_{PLZ}	Disable Time Low to Z			19	50	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

Note 3: $\Delta \lvert V_{T1} \rvert$ and $\Delta \lvert V_{OS} \rvert$ are changes in magnitude of V_{T1} and V_{OS}, respectively, that occur when the input changes state.

Note 4: All typicals are given for $V_{CC} = 5.0$V and $T_A = +25°C$.

Note 5: Threshold parameter limits specified as an algebraic value rather than by magnitude.

Note 6: Hysteresis defined as $V_{HST} = V_{TH} - V_{TL}$.

Note 7: I_{IN} includes the receiver input current and driver TRI-STATE leakage current.

Parameter Measurement Information

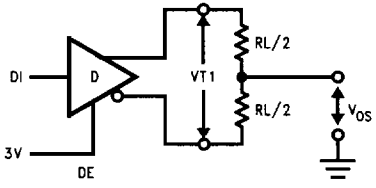

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FIGURE 1. Driver V_{T1} and V_{OS} Test Circuit

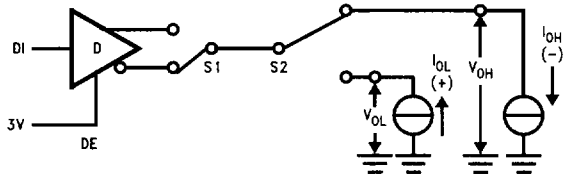

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FIGURE 2. Driver V_{OH} and V_{OL} Test Circuit

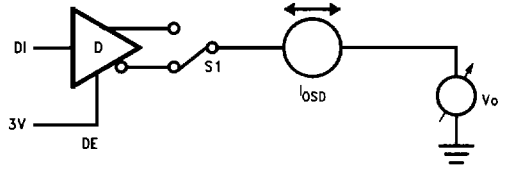

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FIGURE 3. Driver Short Circuit Test Circuit

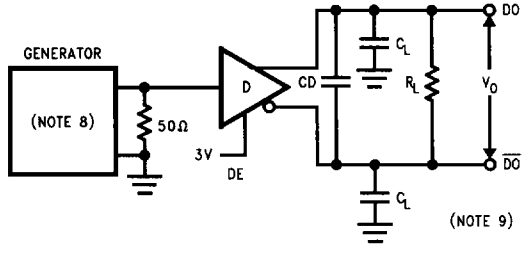

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FIGURE 4. Driver Differential Propagation Delay and Transition Time Test Circuit

Parameter Measurement Information (Continued)

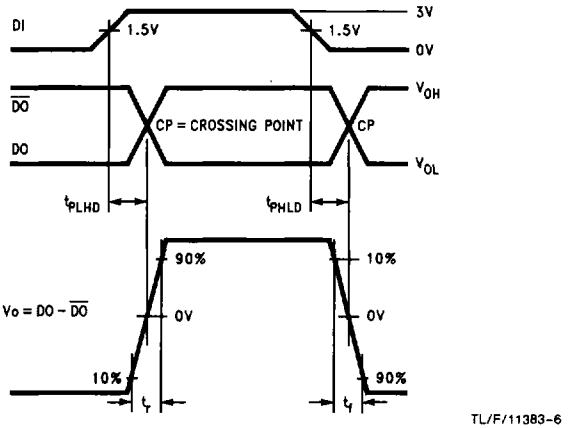

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FIGURE 5. Driver Differential Propagation Delays and Transition Times

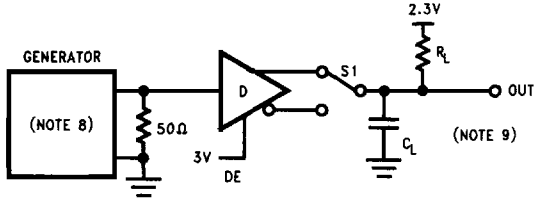

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FIGURE 6. Driver Propagation Delay Test Circuit

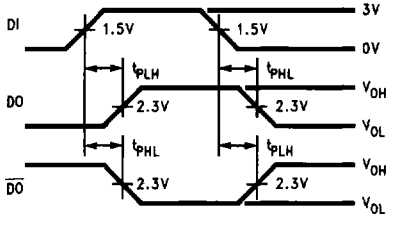

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FIGURE 7. Driver Propagation Delays

Parameter Measurement Information (Continued)

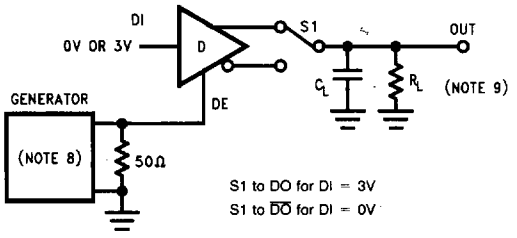

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FIGURE 8. Driver TRI-STATE Test Circuit (t_{PZH}, t_{PHZ})

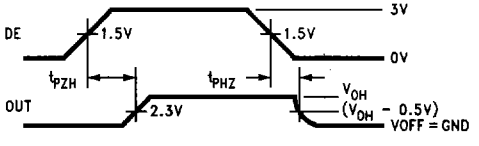

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FIGURE 9. Driver TRI-STATE Delays (t_{PZH}, t_{PHZ})

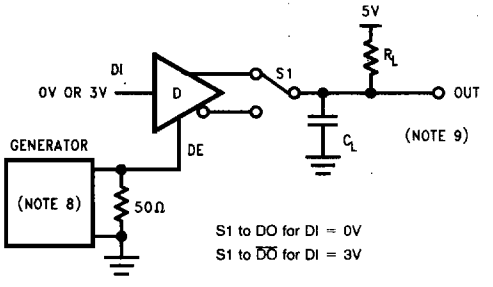

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FIGURE 10. Driver TRI-STATE Test Circuit (t_{PZL}, t_{PLZ})

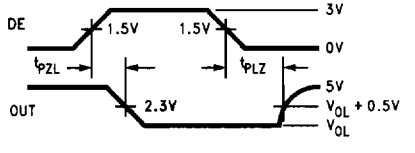

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FIGURE 11. Driver TRI-STATE Delays (t_{PZL}, t_{PLZ})

Parameter Measurement Information (Continued)

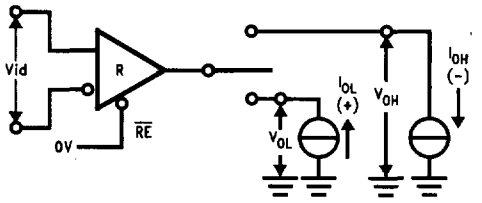

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FIGURE 12. Receiver V_{OH} and V_{OL}

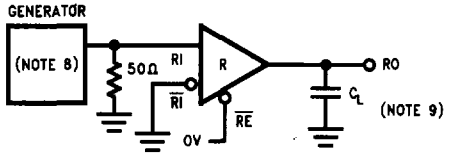

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FIGURE 13. Receiver Propagation Delay Test Circuit

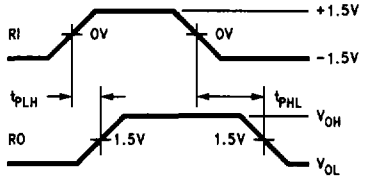

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FIGURE 14. Receiver Propagation Delays

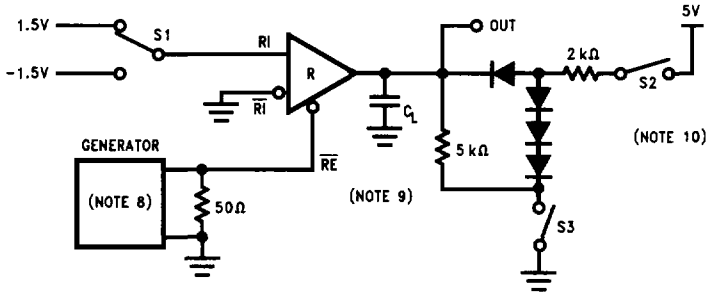

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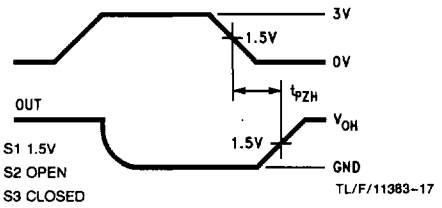
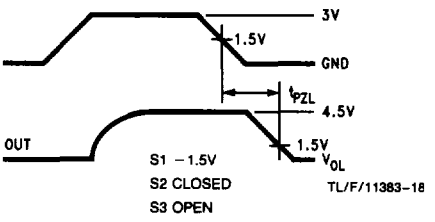
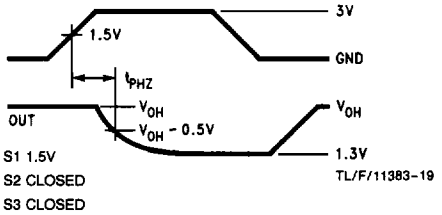
FIGURE 15. Receiver TRI-STATE Delay Test Circuit

Parameter Measurement Information (Continued)







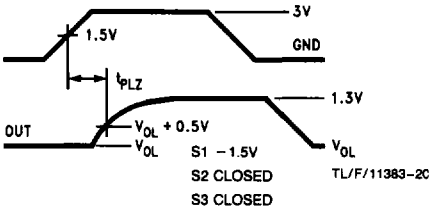


FIGURE 16. Receiver Enable and Disable Timing

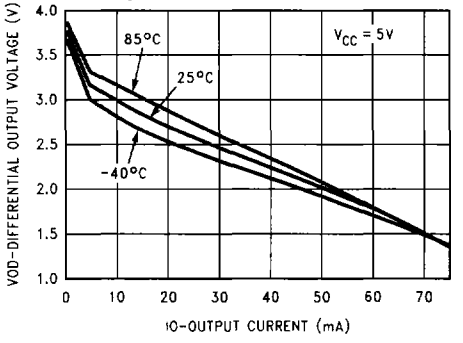
Note 8: The input pulse is supplied by a generator having the following characteristics: f = 1.0 MHz, 50% duty cycle, t_r and t_f < 6.0 ns, Z_O = 50Ω.

Note 9: C_L includes probe and stray capacitance.

Note 10: Diodes are 1N916 or equivalent.

Typical Performance Characteristics

Differential Output Voltage vs Output Current



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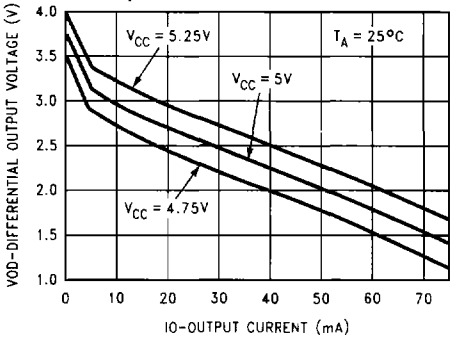
Differential Output Voltage vs Output Current



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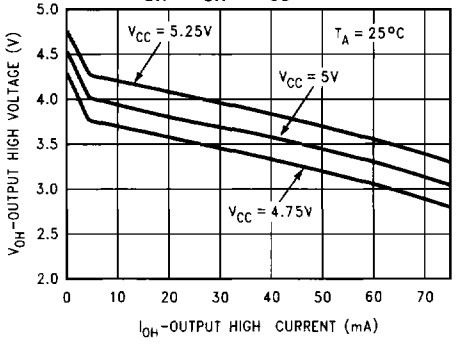
Driver V_{OH} vs I_{OH} vs V_{CC}



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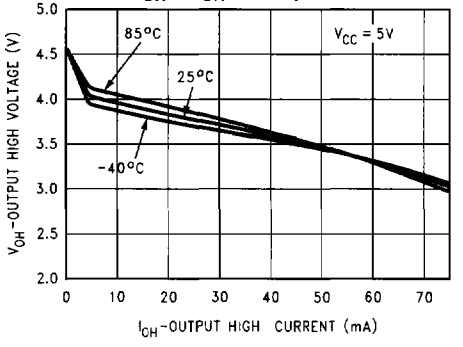
Driver V_{OH} vs I_{OH} vs Temperature



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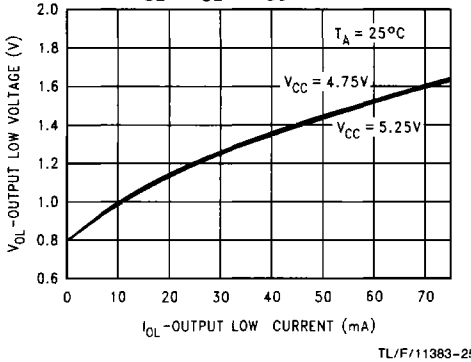
Driver V_{OL} vs I_{OL} vs V_{CC}



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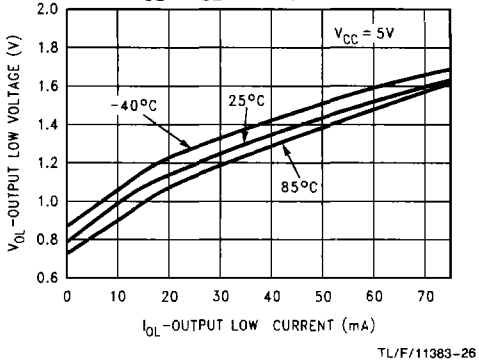
Driver V_{OL} vs I_{OL} vs Temperature



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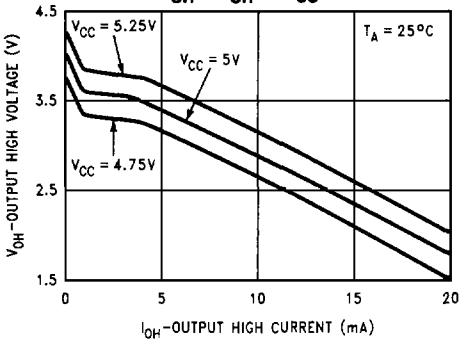
Typical Performance Characteristics (Continued)

Receiver V_{OH} vs I_{OH} vs V_{CC}



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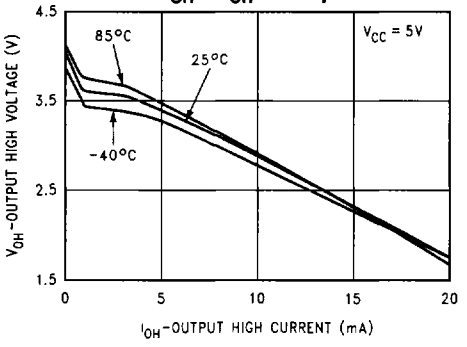
Receiver V_{OH} vs I_{OH} vs Temperature



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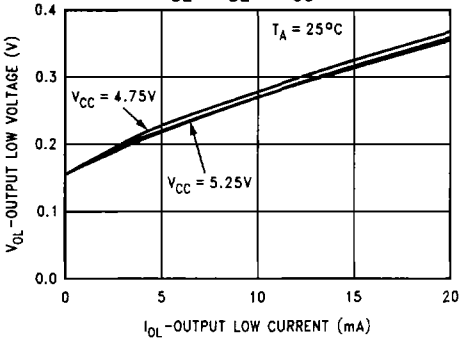
Receiver V_{OL} vs I_{OL} vs V_{CC}



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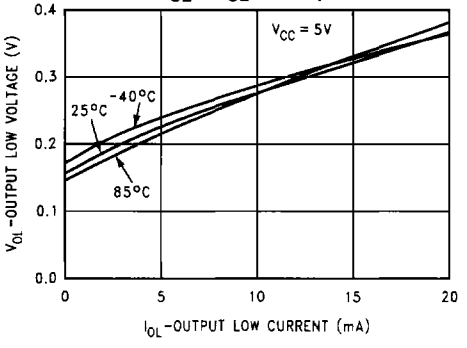
Receiver V_{OL} vs I_{OL} vs Temperature



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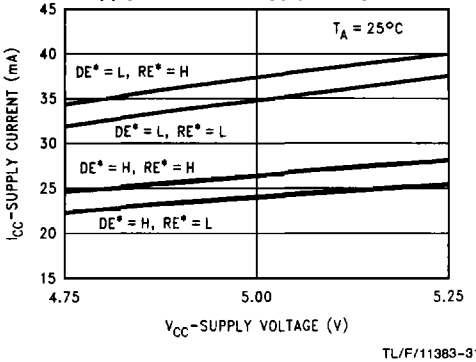
Supply Currrent vs Supply Voltage



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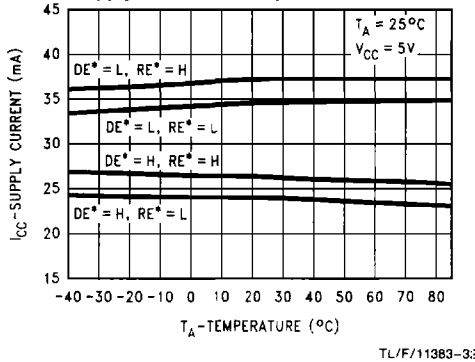
Supply Current vs Temperature



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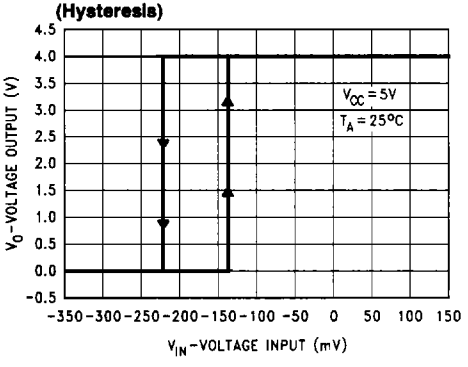
Typical Performance Characteristics (Continued)

Voltage Output vs Voltage Input (Hysteresis)



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