CYPRESS

CY2252

Mobile Pentium™ Processor Compatible Clock Synthesizer/Driver

Features

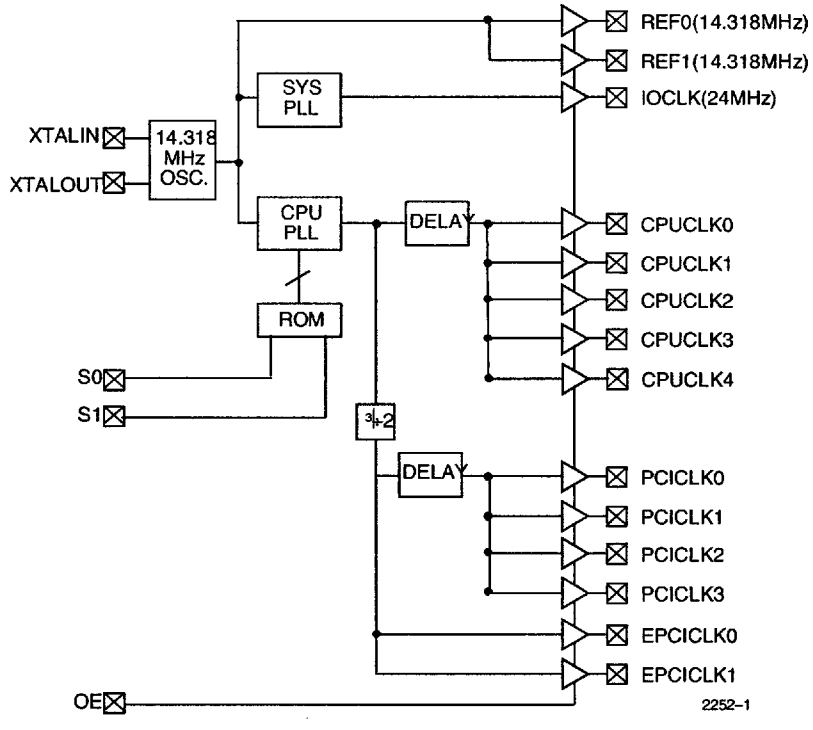
- **Multiple clock outputs to meet requirements of mobile systems using Pentium™ processors**
  - **— Five CPU clocks @ 66.66 MHz, 60.0 MHz, 50.0 MHz or 33.33 MHz pin selectable**
  - **— Six PCI clocks at 33.33 MHz, 30.0 MHz, 25 MHz or 16.6 MHz. Includes two Early PCI clocks which lead other PCI and CPU clocks by 3.5ns typically**
  - **— One I/O clock @ 24 MHz**
  - **— Two Ref. clocks @ 14.318 MHz**
  - **— Ref. 14.318 MHz Xtal oscillator input**
- **Doze Mode Support (33 MHz CPU clock)**
- **Early PCI clocks are ideal for docking station design**
- **CPU clock jitter ≤ 200 ps cycle-to-cycle**
- **Low skew outputs**
  - **— ≤ 250 ps between CPU clocks (CPUCLK)**
  - **— ≤ 250 ps between PCI clocks (PCICLK)**
  - **— ≤ 500 ps between CPU and PCI clocks**
- **Packaged in 28-pin SSOP for minimum board space**
- **3.3V operation**
- **Internal pull-up resistors on S0,S1, and OE inputs**

Functional Description

The CY2252 is a Clock Synthesizer/Driver chip for an Intel® Pentium processor based PC. It is optimized to address the needs of mobile Pentium designs with Doze mode support, and early PCI clocks; provides two "early" PCI clocks to compensate for clock delays caused by long traces in docking station designs; and has low-skew outputs (≤ 250 ps between the CPU clocks, ≤ 250 ps between the PCI clocks). In addition, the CY2252 CPU clock outputs have less than 200 ps cycle-to-cycle jitter. Finally, both the PCI and CPU clock outputs meet the 1V/ns slew rate requirement of Pentium processor based systems.

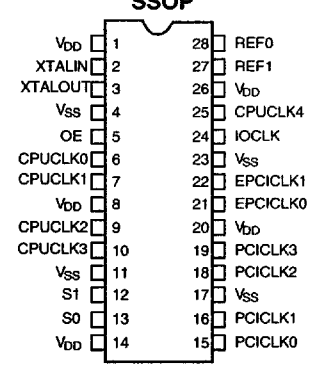
The CY2252 accepts a 14.318-MHz reference crystal as its input. The chip has two PLLs, one of which generates the CPU and PCI clocks while the other generates a 24 MHz I/O clock. The latter can drive a Floppy Disk Controller and Super I/O™ or Ultra I/O™ devices. The CY2252 runs off a 3.3V supply.

Logic Block Diagram



Pin Configuration

Top View
SSOP



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Super I/O is a trademark of National Semiconductor.
Ultra I/O is a trademark of Standard Microsystems Corp.

Pin Summary

Name	Number	Description
V_{DD}	1	Voltage supply
XTALIN[1]	2	Reference crystal input
XTALOUT[1]	3	Reference crystal feedback
V_{SS}	4	Ground
OE	5	Output Enable, Active HIGH (Internal pull-up resistor to V_{DD})
CPUCLK0	6	CPU clock output
CPUCLK1	7	CPU clock output
V_{DD}	8	Voltage supply
CPUCLK2	9	CPU clock output
CPUCLK3	10	CPU clock output
V_{SS}	11	Ground
S1	12	CPU clock select input, bit 1 (Internal pull-up resistor to V_{DD})
S0	13	CPU clock select input, bit 0 (Internal pull-up resistor to V_{DD})
V_{DD}	14	Voltage supply
PCICLK0	15	PCI clock output
PCICLK1	16	PCI clock output
V_{SS}	17	Ground
PCICLK2	18	PCI clock output
PCICLK3	19	PCI clock output
V_{DD}	20	Voltage supply
EPCICLK0	21	Early PCI clock output
EPCICLK1	22	Early PCI clock output
V_{SS}	23	Ground
IOCLK	24	I/O clock output (24 MHz)
CPUCLK4	25	CPU clock output
V_{DD}	26	Voltage supply
REF1	27	Reference clock output (14.318 MHz)
REF0	28	Reference clock output (14.318 MHz)

Notes:
1. For best accuracy, use a parallel-resonant crystal, C_{LOAD}=17 pF

Function Table

OE	S0	S1	XTALIN Input	CPUCLK	PCICLK	Ref. Clock Output	IOCLK
0	X	X	14.318 MHz	High-Z	High-Z	High-Z	High-Z
1	0	0	14.318 MHz	50 MHz	25 MHz	14.318 MHz	24 MHz
1	0	1	14.318 MHz	60 MHz	30 MHz	14.318 MHz	24 MHz
1	1	0	14.318 MHz	66 MHz	33.33 MHz	14.318 MHz	24 MHz
1	1	1	14.318 MHz	33.33 MHz	16.67 MHz	14.318 MHz	24 MHz

PCI Clock Driver Strength Requirements

- Matched impedances on both rising and falling edges on the output drivers
- Output impedance: 25Ω (typical) measured at 1.5V
- Maximum output impedance: 40Ω measured at 1.5V

CPU Clock Driver Strength Requirements

- Matched impedances on both rising and falling edges on the output drivers
- Output impedance: 25Ω (typical) measured at 1.5V
- Maximum output impedance: 40Ω measured at 1.5V

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage.....–0.5 to +7.0V

Input Voltage..... –0.5V to V_{DD}+0.5

Storage Temperature (Non-Condensing).... –65°C to +150°C

Max. Soldering Temperature (10 sec) ..... +260°C

Junction Temperature..... +150°C

Operating Conditions[2]

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	3.135	3.465	V
T_A	Ambient Temperature	0	70	°C
C_L	Max. Capacitive Load on CPUCLK EPCICLK, PCICLK IOCLK REF0 REF1		 20 30 20 30 15	pF
$f_{(REF)}$	Reference Frequency, Oscillator Nominal Value	14.318	14.318	MHz

Notes:

2. Electrical parameters are guaranteed with these operating conditions.

Electrical Characteristics V_{DD} = 3.3V ±5%, T_A = 0°C to +70°C

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{IH}	High-level Input Voltage	Except Crystal Inputs			2.0		V
V_{IL}	Low-level Input Voltage	Except Crystal Inputs				0.8	V
V_{OH}	High-level Output Voltage	$V_{DD} = V_{DD}$ Min.	I_{OH} = 6 mA	CPUCLK	2.4		V
			I_{OH} = 12 mA	EPCICLK, PCI-CLK, REF0			
			I_{OH} = 4 mA	IOCLK			
			I_{OH} = 8 mA	REF1			
V_{OL}	Low-level Output Voltage	$V_{DD} = V_{DD}$ Min.	I_{OL} = 6 mA	CPUCLK		0.4	V
			I_{OL} = 12 mA	EPCICLK, PCI-CLK, REF0			
			I_{OL} = 4 mA	IOCLK			
			I_{OL} = 8 mA	REF1			
I_{IH}	Input High Current	$V_{IH} = V_{DD}$				5	µA
I_{IL}	Input Low Current	V_{IL} = 0 V				100	µA
I_{OZ}	Output Leakage Current	Three-state Outputs			–10	+10	µA
I_{DD}	Power Supply Current	V_{DD} = 3.465, V_{IN} = 0 V or V_{DD}				90	mA

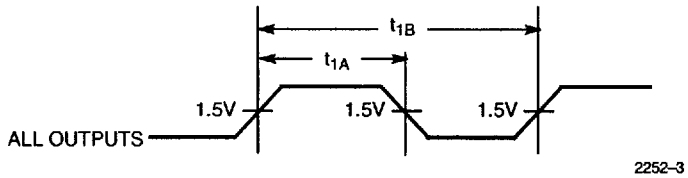
Switching Characteristics[3]

Parameter	Output	Name	Description	Min.	Max.	Unit
t_1	All	Output Duty Cycle	$t_1 = t_{1A} \div t_{1B}$, measured at 1.5V	45%	55%	
t_2	CPUCLK, PCI-CLK, EPCICLK	Output Slew Rate	Measured between 0.4V and 2.4V	1	4	V/ns
t_3	REF0, REF1 IOCLK	Rise Time	Measured between 0.4V and 2.4V		4	ns
t_4	REF0, REF1 IOCLK	Fall Time	Measured between 2.4V and 0.4V		4	ns
t_5	CPUCLK	CPU-CPU Skew	Measured at 1.5V		250	ps
t_6	PCICLK	PCI-PCI Skew	Measured at 1.5V		250	ps
t_7	CPUCLK, PCICLK	CPU-PCI Skew	Measured at 1.5V		500	ps
t_8	EPCICLK, PCI-CLK	EPCI-PCI Skew	Measured at 1.5V	2	5	ns
t_9	CPUCLK	Clock Jitter	Cycle-Cycle Clock Jitter		200	ps

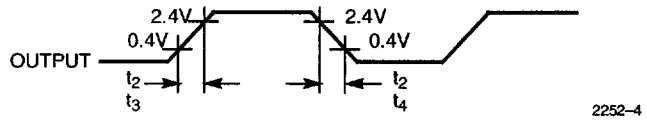
Notes:
3. All parameters specified with outputs fully loaded.

Switching Waveforms

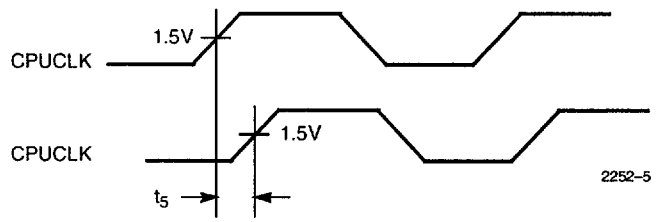
Duty Cycle Timing



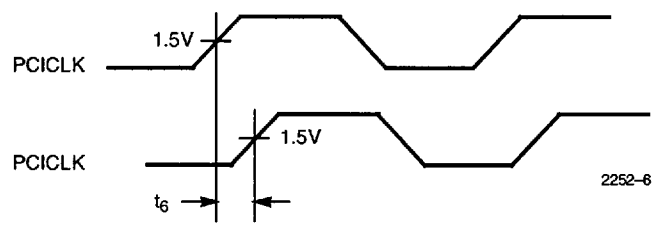
All Outputs Rise/Fall Time



CPU–CPU Clock Skew

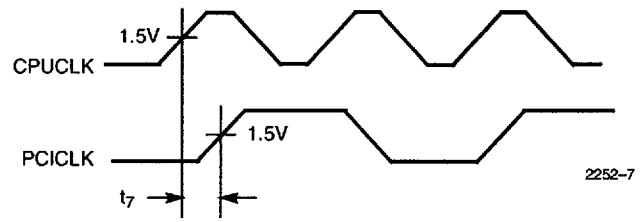


PCI–PCI Clock Skew

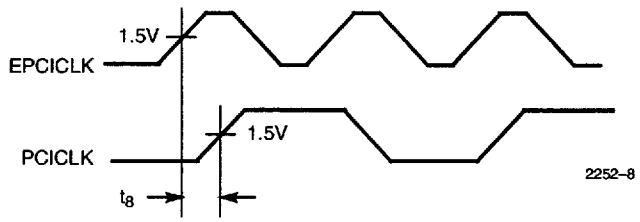


Switching Waveforms (continued)

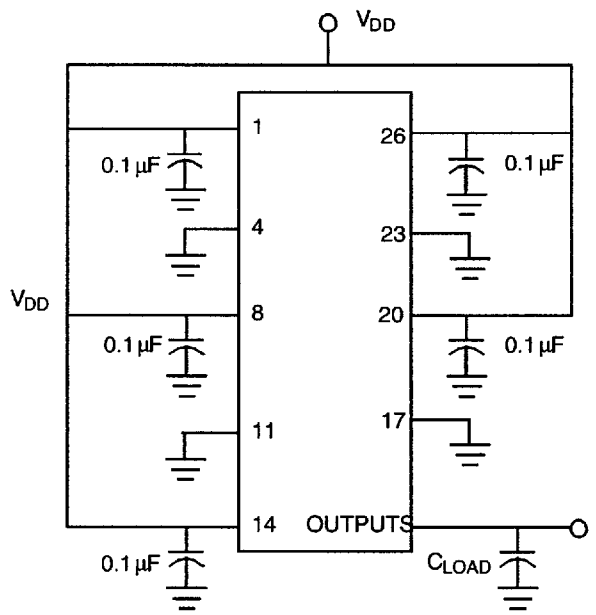
CPU–PCI Clock Skew



EPCI–PCI Clock Skew



Test Circuit



Note: All capacitors should be placed as close to each pin as possible

Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
CY2252PVC-1	O28	28-Pin SSOP	Commercial

Document #: 38-00503-A

Package Diagram

28-Lead Shrunk Small Outline Package O28