



CYPRESS SEMICONDUCTOR

T-46-23-10

CY7C164A
CY7C166A

16,384 x 4 Static R/W RAM

Features

- Automatic power-down when deselected
- Output Enable (OE) feature (7C166A)
- CMOS for optimum speed/power
- High speed
— $t_{AA} = 12$ ns
- Low active power
— 935 mW
- Low standby power
— 220 mW
- TTL-compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

Functional Description

The CY7C164A and CY7C166A are high-performance CMOS static RAMs organized as 16,384 by 4 bits. Easy memory expansion is provided by an active LOW chip enable (CE) and three-state drivers. The CY7C166A has an active low output enable (OE) feature. Both devices have an automatic power-down feature, reducing the power consumption by 60% when deselected.

Writing to the device is accomplished when the chip enable (CE) and write enable (WE) inputs are both LOW (and the output enable (OE) is LOW for the 7C166A). Data on the four input/output pins (I/O₀

through I/O₃) is written into the memory location specified on the address pins (A₀ through A₁₃).

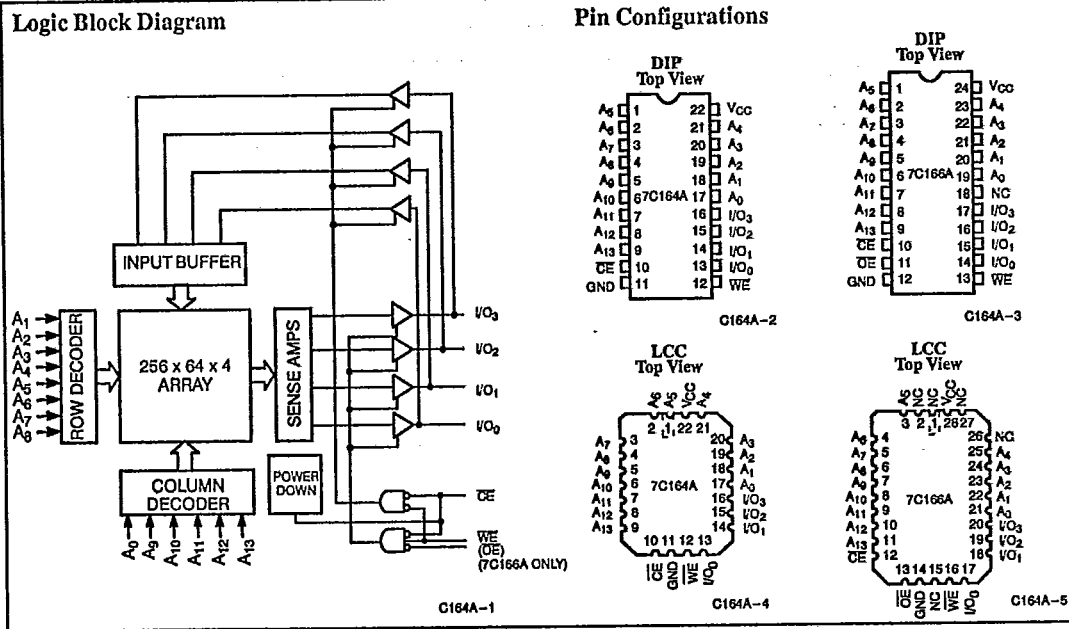
Reading the device is accomplished by taking chip enable (CE) LOW (and OE LOW for 7C166A), while write enable (WE) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

The I/O pins stay in high-impedance state when chip enable (CE) is HIGH, or write enable (OE) is HIGH for 7C166A.

A die coat is used to insure alpha immunity.



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Selection Guide^[1]

		7C164A-12 7C166A-12	7C164A-15 7C166A-15	7C164A-20 7C166A-20	7C164A-25 7C166A-25	7C164A-35 7C166A-35	7C164A-45 7C166A-45
Maximum Access Time (ns)		12	15	20	25	35	45
Maximum Operating Current (mA)	Military	170	160	100	100	100	100
Maximum Standby Current (mA)	Military	40/20	35/20	40/20	40/20	30/20	30/20

Shaded area contains advanced information.

Note:

1. For commercial specifications, see the CY7C164/CY7C166 datasheet.



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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

- Storage Temperature - 65°C to +150°C
- Ambient Temperature with Power Applied - 55°C to +125°C
- Supply Voltage to Ground Potential - 0.5V to +7.0V
- DC Voltage Applied to Outputs in High Z State - 0.5V to +7.0V
- DC Input Voltage - 3.0V to +7.0V

- Output Current into Outputs (Low) 20 mA
- Static Discharge Voltage >2001V (per MIL-STD-883, Method 3015)
- Latch-up Current >200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Military ^[2]	- 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[3]

Parameters	Description	Test Conditions	7C164A-12 7C166A-12		7C164A-15 7C166A-15		7C164A-20 7C166A-20		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 4.0 mA	2.4		2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[4]		-3.0	0.8	-3.0	0.8	-3.0	0.8	V
I _{Ix}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	-10	+10	-10	+10	µA
I _{oz}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-10	+10	-10	+10	-10	+10	µA
I _{os}	Output Short Circuit Current ^[5]	V _{CC} = Max., V _{OUT} = GND		-350		-350		-350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA		170		160		100	mA
I _{SB1}	Automatic \overline{CE} ^[6] Power Down Current	Max. V _{CC} , $\overline{CE} \geq V_{IH}$ Min. Duty Cycle = 100%		40		35		40	mA
I _{SB2}	Automatic \overline{CE} ^[6] Power Down Current	Max. V _{CC} , $\overline{CE} \geq V_{IH} - 0.3V$ V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V		20		20		20	mA

Shaded area contains advanced information.

Notes:

2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. V_{IL} min. = - 3.0V for pulse durations less than 30 ns.
5. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
6. A pull-up resistor to V_{CC} on the \overline{CE} input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.



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Electrical Characteristics Over the Operating Range^[3](continued)

Parameters	Description	Test Conditions	7C164A-25 7C166A-25		7C164A-35, 45 7C166A-35, 45		Units
			Min.	Max.	Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	2.2	V _{CC}	V
V _{IL}	Input LOW Voltage ^[4]		-3.0	0.8	-3.0	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+10	-10	+10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-10	+10	-10	+10	μA
I _{OS}	Output Short Circuit Current ^[5]	V _{CC} = Max., V _{OUT} = GND		-350		-350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA		100		100	mA
I _{SB1}	Automatic \overline{CE} ^[6] Power Down Current	Max. V _{CC} , $\overline{CE} \geq V_{IH}$ Min. Duty Cycle = 100%		40		30	mA
I _{SB2}	Automatic \overline{CE} ^[6] Power Down Current	Max. V _{CC} , $\overline{CE} \geq V_{IH} - 0.3V$ V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V		20		20	mA

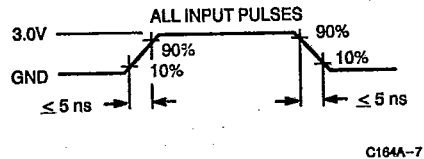
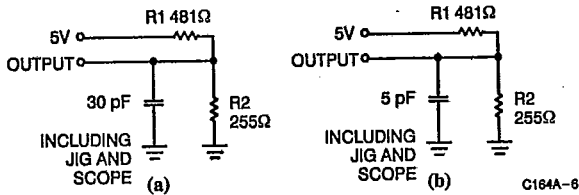
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Capacitance^[7]

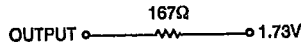
Parameters	Description	Test Conditions	Max.	Units
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	10	pF
C _{OUT}	Output Capacitance		10	pF

Note:
7. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT





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Switching Characteristics Over the Operating Range^{3, 8}

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Parameters	Description	7C164A-12 7C166A-12		7C164A-15 7C166A-15		7C164A-20 7C166A-20		7C164A-25 7C166A-25		7C164A-35 7C166A-35		7C164A-45 7C166A-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
t _{RC}	Read Cycle Time	12		15		20		25		35		45		ns
t _{AA}	Address to Data Valid		12		15		20		25		35		45	ns
t _{OHA}	Output Hold from Address Change	3		3		3		3		3		3		ns
t _{ACE}	\overline{CE} LOW to Data Valid		12		15		20		25		35		45	ns
t _{DOE}	\overline{OE} LOW to Data Valid (7C166A)		6		7		10		12		15		20	ns
t _{LZOE}	\overline{OE} LOW to Low Z (7C166A)	0		0		3		3		3		3		ns
t _{HZOE}	\overline{OE} HIGH to High Z (7C166A)		7		8		8		10		12		15	ns
t _{LZCE}	\overline{CE} LOW to Low Z ^[9]	3		3		5		5		5		5		ns
t _{HZCE}	\overline{CE} HIGH to High Z ^[9, 10]		7		8		8		10		15		15	ns
t _{PU}	\overline{CE} LOW to Power-Up	0		0		0		0		0		0		ns
t _{PD}	\overline{CE} HIGH to Power-Down		12		15		20		20		20		25	ns
WRITE CYCLE^[11]														
t _{WC}	Write Cycle Time	12		15		20		20		25		40		ns
t _{SCE}	\overline{CE} LOW to Write End	8		10		15		20		25		30		ns
t _{AW}	Address Set-Up to Write End	9		10		15		20		25		30		ns
t _{HA}	Address Hold from Write End	0		0		0		0		0		0		ns
t _{SA}	Address Set-Up to Write Start	0		0		0		0		0		0		ns
t _{PWE}	\overline{WE} Pulse Width	8		10		15		15		20		20		ns
t _{SD}	Data Set-Up to Write End	6		7		10		10		15		15		ns
t _{HD}	Data Hold from Write End	0		0		0		0		0		0		ns
t _{LZWE}	\overline{WE} HIGH to Low Z ^[9]	3		3		5		5		5		5		ns
t _{HZWE}	\overline{WE} LOW to High Z ^[9, 10]		6		7		7		7		10		15	ns

Shaded area contains advanced information.

Notes:

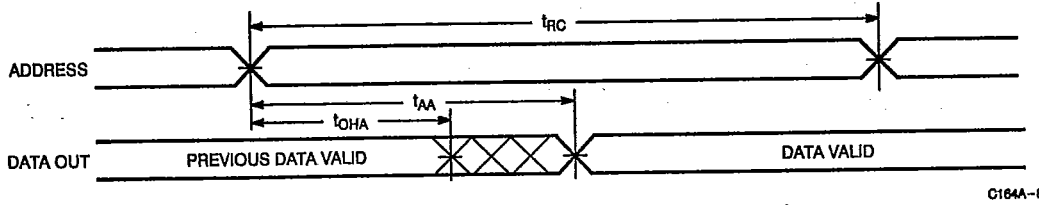
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device. These parameters are guaranteed and not 100% tested.
- t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) in AC Test Loads. Transition is measured ±500 mV from steady state voltage.
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.



Switching Waveforms

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Read Cycle No. 1^[12, 13]

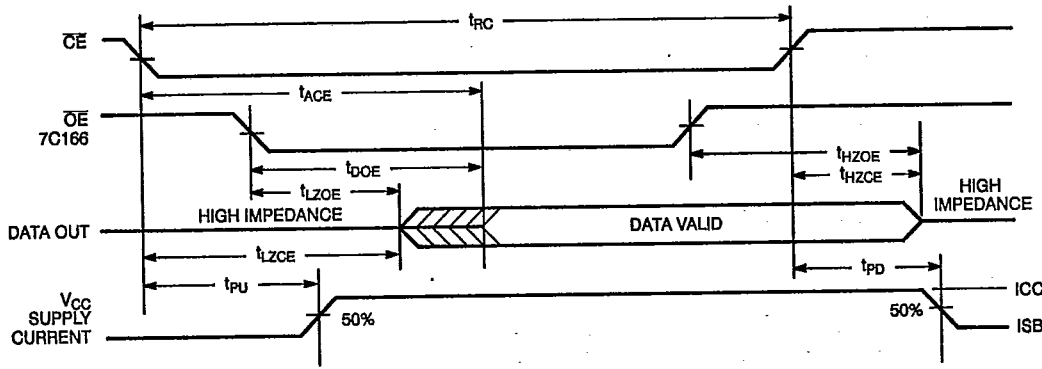


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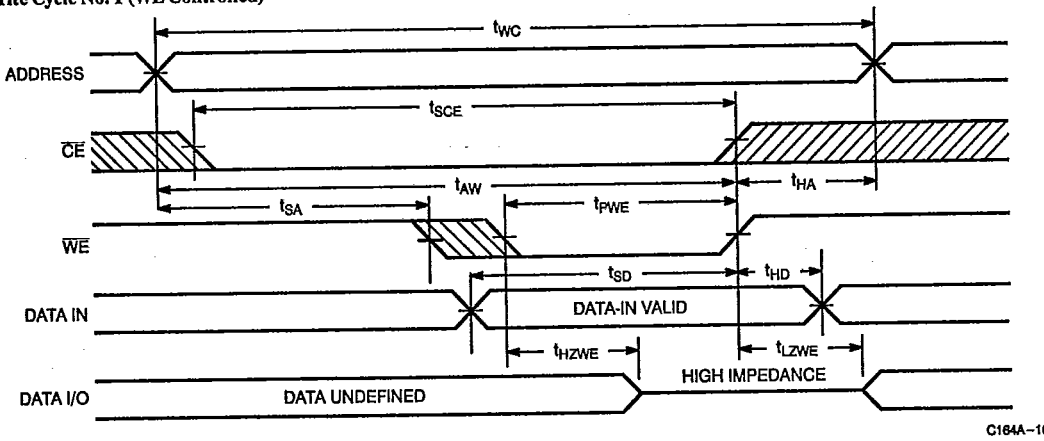
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Read Cycle No. 2^[12, 14]



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Write Cycle No. 1 (\overline{WE} Controlled)^[11, 15]



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Notes:

- 12. \overline{WE} is HIGH for read cycle.
- 13. Device is continuously selected, $\overline{CE} = V_{IL}$, (7C166A $\overline{OE} = V_{IL}$ also).
- 14. Address valid prior to or coincident with \overline{CE} transition LOW.
- 15. 7C166A only: Data I/O will be high impedance if $\overline{OE} = V_{IH}$.

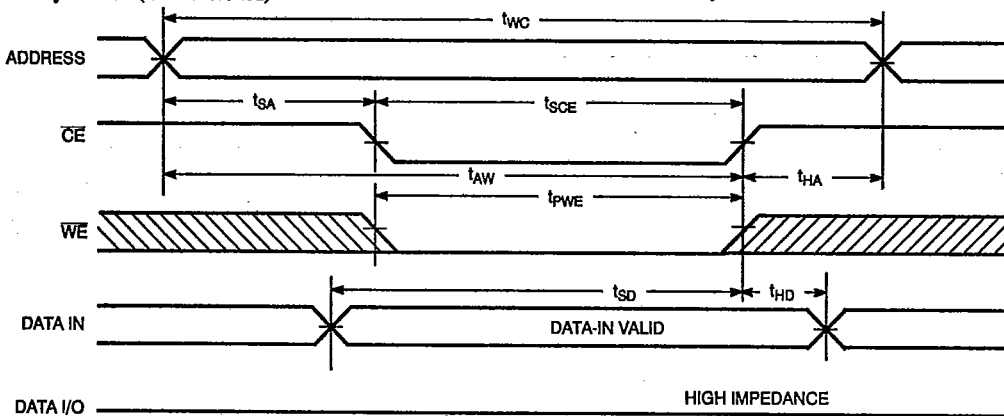


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Switching Waveforms (continued)

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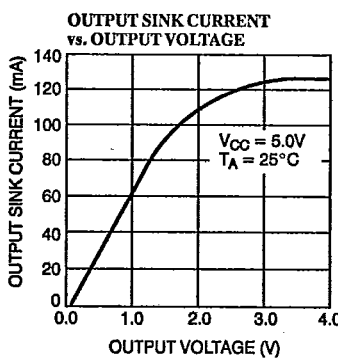
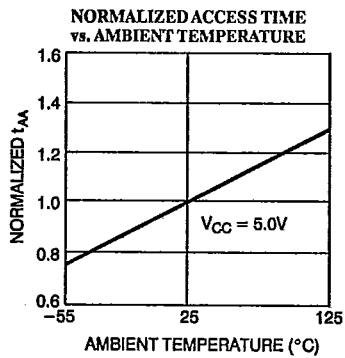
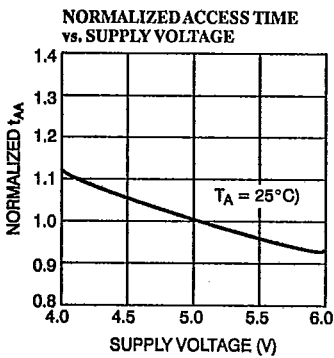
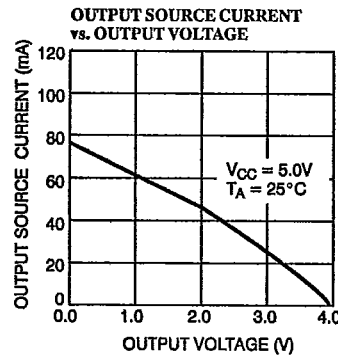
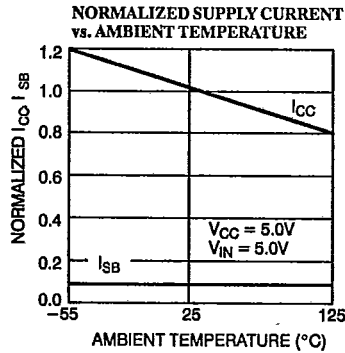
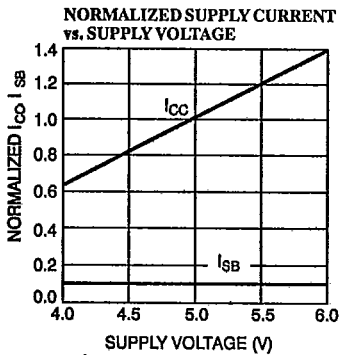
Write Cycle No. 2 (\overline{CE} Controlled) [11, 15, 16]



C164A-11

Note:
16. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics

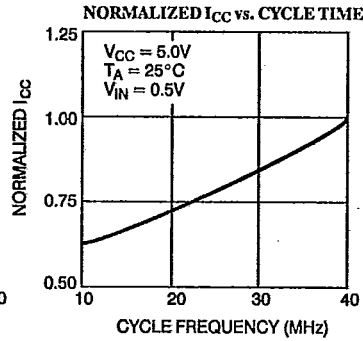
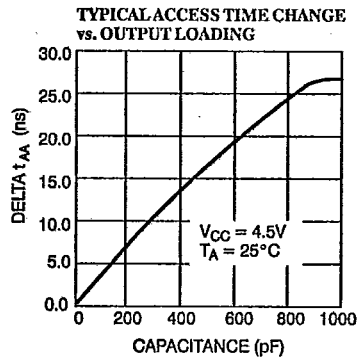
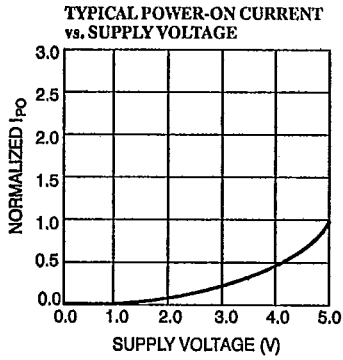




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Typical DC and AC Characteristics (continued)

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CY7C164A Truth Table

\overline{CE}	\overline{WE}	Inputs/Outputs	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

CY7C166A Truth Table

\overline{CE}	\overline{WE}	\overline{OE}	Inputs/Outputs	Mode
H	X	X	High Z	Deselect/Power-Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Address Designators

Address Name	Address Function	CY7C164A Pin Number	CY7C166A Pin Number
A5	X3	1	1
A6	X4	2	2
A7	X5	3	3
A8	X6	4	4
A9	X7	5	5
A10	Y5	6	6
A11	Y4	7	7
A12	Y0	8	8
A13	Y1	9	9
A0	Y2	17	19
A1	Y3	18	20
A2	X0	19	21
A3	X1	20	22
A4	X2	21	23



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Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
12	CY7C164A-12DMB	D10	Military
	CY7C164A-12KMB	K73	
	CY7C164A-12LMB	L52	
15	CY7C164A-15DMB	D10	Military
	CY7C164A-15KMB	K73	
	CY7C164A-15LMB	L52	
20	CY7C164A-20DMB	D10	Military
	CY7C164A-20KMB	K73	
	CY7C164A-20LMB	L52	
25	CY7C164A-25DMB	D10	Military
	CY7C164A-25KMB	K73	
	CY7C164A-25LMB	L52	
35	CY7C164A-35DMB	D10	Military
	CY7C164A-35KMB	K73	
	CY7C164A-35LMB	L52	
45	CY7C164A-45DMB	D10	Military
	CY7C164A-45KMB	K73	
	CY7C164A-45LMB	L52	

Speed (ns)	Ordering Code	Package Type	Operating Range
12	CY7C166A-15DMB	D14	Military
	CY7C166A-15KMB	K73	
	CY7C166A-15LMB	L54	
15	CY7C166A-15DMB	D14	Military
	CY7C166A-15KMB	K73	
	CY7C166A-15LMB	L54	
20	CY7C166A-20DMB	D14	Military
	CY7C166A-20KMB	K73	
	CY7C166A-20LMB	L54	
25	CY7C166A-25DMB	D14	Military
	CY7C166A-25KMB	K73	
	CY7C166A-25LMB	L54	
35	CY7C166A-35DMB	D14	Military
	CY7C166A-35KMB	K73	
	CY7C166A-35LMB	L54	
45	CY7C166A-45DMB	D14	Military
	CY7C166A-45KMB	K73	
	CY7C166A-45LMB	L54	

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MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL Max.}	1, 2, 3
I _{IX}	1, 2, 3
I _{OZ}	1, 2, 3
I _{OS}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB1}	1, 2, 3
I _{SB1}	1, 2, 3

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Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{OHA}	7, 8, 9, 10, 11
t _{ACE}	7, 8, 9, 10, 11
t _{DOE} ^[17]	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCE}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11

Note:
17. 7C166A only.