4-Wire Serial CMOS E²PROMs

1K (128 x 8 or 64 x 16)

2K (256 x 8 or 128 x 16)

4K (512 x 8 or 256 x 16)

Preliminary

Features

- **Low Voltage and Standard Voltage Operation**
  - **5.0 V (V_{CC} = 4.5 V to 5.5 V)**
  - **3.0 V (V_{CC} = 2.7 V to 5.5 V)**
- **User Selectable Internal Organization**
  - **1K: 128 x 8 or 64 x 16**
  - **2K: 256 x 8 or 128 x 16**
  - **4K: 512 x 8 or 256 x 16**
- **Four-Wire Serial Interface**
- **Self-Timed Write Cycle (10 ms Max)**
- **High Reliability**
  - **Endurance: 100,000 Cycles**
  - **Data Retention: 100 Years**
- **8-Pin PDIP and JEDEC SOIC Packages**

Description

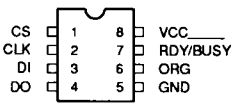
The AT59C11/12/13 provides 1024/2048/4096 bits of serial E²PROM (Electrically Erasable Programmable Read Only Memory) organized as 64/128/256 words of 16 bits each, when the ORG Pin is connected to V_{CC} and 128/256/512 words of 8 bits each when it is tied to ground. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT59C11/12/13 is available in space saving 8-pin PDIP and 8-pin JEDEC and SOIC packages.

The AT59C11/12/13 is enabled through the Chip Select pin (CS), and accessed via a 4-wire serial interface consisting of Data Input (DI), Data Output (DO), and Clock (CLK). Upon receiving a READ instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO, the WRITE cycle is completely self-timed and no separate ERASE cycle is required before WRITE. The WRITE cycle is only enabled when the part is in the ERASE/WRITE ENABLE state. Ready/$\overline{\text{Busy}}$ status can be monitored upon completion of a programming operation by polling the Ready/$\overline{\text{Busy}}$ pin.

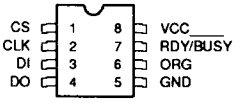
Atmel's E²PROMs are designed and tested for applications requiring extended endurance. Devices in this family are guaranteed for 100,000 ERASE/WRITE cycles and 100-year data retention. The AT59C11/12/13 is available in 5.0 V ± 10% and 2.7 V to 5.5 V versions. Data retention is specified to be greater than 100 years.

Pin Configurations

Pin Name	Function
CS	Chip Select
CLK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
V_{CC}	Power Supply
ORG	Internal Organization
RDY/$\overline{\text{BUSY}}$	Status Output



8-Pin PDIP



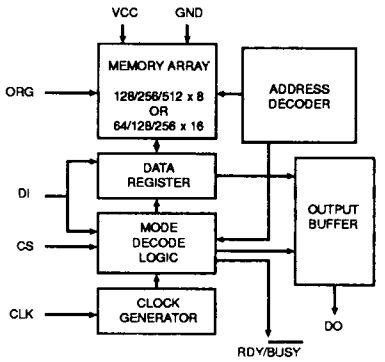
8-Pin SOIC

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0 V to +7.0 V
Maximum Operating Voltage	6.25 V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram (1)



Note:
1. When the ORG pin is connected to V_{CC}, the x 16 organization is selected. When it is connected to ground, the x 8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the x 16 organization.

D.C. Characteristics

Applicable over recommended operating range from: T_{AI} = -40°C to +85°C, V_{CC} = +2.7 V to +5.5 V, T_{AC} = 0°C to + 70°C, V_{CC} = +2.7 V to +5.5 V (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Max	Units
I_{CC1}	Operating Current CMOS Input Levels	CS = V_{IH},	CLK = 1.0 MHz(1) CLK = 0.5 MHz(1)		2 2	mA
I_{CC2}	Operating Current TTL Input Levels	CS = V_{IH},	CLK = 1.0 MHz(1) CLK = 0.5 MHz(1)		3 3	mA
I_{CC3}	Standby Current	CS = 0 V	CLK = 1.0 MHz(1) CLK = 0.5 MHz(1)		100 100	µA
I_{IL}	Input Leakage	V_{IN} = 0 V to V_{CC}		-2.5 -10	2.5 10	µA
I_{OL}	Output Leakage	V_{IN} = 0 V to V_{CC}		-2.5 -10	2.5 10	µA
V_{IL1} V_{IH1}	Input Low Voltage Input High Voltage	4.5 V ≤ V_{CC} ≤ 5.5 V		 2	0.8	V
V_{IL2} V_{IH2}	Input Low Voltage Input High Voltage	2.7 V ≤ V_{CC} ≤ 5.5 V		-0.1 2	0.6 VCC + 1	V
V_{OL1} V_{OH1}	Output Low Voltage Output High Voltage	4.5 V ≤ V_{CC} ≤ 5.5 V I_{OL} = 2.1 mA I_{OH} = -400 µA		 2.4	0.4	V V
V_{OL2} V_{OH2}	Output Low Voltage Output High Voltage	2.7 V ≤ V_{CC} ≤ 5.5 V I_{OL} = 10 µA I_{OH} = -10 µA		 V_{CC} - 0.2	0.2	V V

Note: 1. Devices operate at 1.0 MHz at VCC = 5.0 V ± 10% at commercial temperature. All low voltage and industrial parts operate at 0.5 MHz.

A.C. Characteristics

Applicable over recommended operating range from T_A = -40°C to + 85°C, V_{CC} = +2.7 V to +5.5 V, CL = 1 TTL Gate and 100 pF (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Max	Units
f_{CLK}	CLK Clock Frequency		0 0	1 0.5	MHz
t_{CKH}	CLK High Time	Note 1 Note 2	500 500		ns
t_{CKL}	CLK Low Time	Note 1 Note 2	250 500		ns
t_{CS}	Minimum CS Low Time	Note 3 Note 4	250 500		ns
t_{CSS}	CS Setup Time	Relative to CLK	50 100		ns
t_{DIS}	DI Setup Time	Relative to CLK	100 200		ns
t_{CSH}	CS Hold Time	Relative to CLK	0		ns
t_{DIH}	DI Hold Time	Relative to CLK	100 200		ns
t_{PD}	Output Delay	AC Test		500 1000	ns
t_{RBD}	CS to Status Valid	AC Test		500 1000	ns
t_{CZ}	CS to DO in High Impedance	AC Test CS = V_{IL}		100 200	ns
t_{WC}	Write Cycle Time			10	ms
	Endurance	Number of Data Changes per Bit	Typical 100,000		Cycles

Notes:

1. The CLK frequency specification for Commercial parts specifies a minimum CLK clock period of 1 µs, therefore in an CLK clock cycle $t_{CKH} + t_{CKL}$ must be greater than or equal to 2 µs. For example if t_{CKL} = 250 ns then the minimum t_{CKH} = 750 ns in order to meet the CLK frequency specification.
2. The CLK frequency specification for extended Temperature parts specifies a minimum CLK clock period of 2 µs, therefore in an CLK clock cycle $t_{CKH} + t_{CKL}$ must be greater than or equal to 2 µs. For example, if the t_{CKL} = 500 ns then the minimum t_{CKH} = 1.5 µs in order to meet the CLK frequency specification.
3. For Commercial parts CS must be brought low for a minimum of 250 ns (t_{CS}) between consecutive instruction cycles.
4. For Extended Temperature parts CS must be brought low for a minimum of 500 ns (t_{CS}) between consecutive instruction cycles.

Pin Capacitance [1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0 V (unless otherwise noted)

	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (DO)	5	pF	V_{OUT} = 0 V
C_{IN}	Input Capacitance (CS, CLK, DI, RDY/$\overline{BUSY}$)	5	pF	V_{IN} = 0 V

Note: 1. This parameter is characterized and is not 100% tested.

Functional Description

The AT59C11/12/13 are accessed via a simple and versatile 4-wire serial communication interface. Device operation is controlled by 6 instructions issued by the host processor. A valid instruction consists of a Start Bit (logic '1') followed by the appropriate Op Code and the desired memory Address location.

READ (READ): The Read (READ) instruction contains the Address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock CLK. It should be noted that a dummy bit (logic '0') precedes the 8- or 16-bit data output string.

ERASE/WRITE (EWEN): To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the Erase/Write Enable state, programming remains enabled until an Erase/Write Disable (EWDS) instruction is executed or V_{CC} power is removed from the part.

WRITE (WRITE): The Write (WRITE) instruction contains the 8 or 16 bits of data to be written into the specified memory location. The self-timed programming cycle starts after the last bit of data is received at serial data input pin DI. The Ready/$\overline{\text{Busy}}$ status of the AT59C11/12/13 can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin. A logic '0' at DO indicates that programming is still in progress. A logic '1' indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions.

ERASE ALL (ERAL): The Erase All (ERAL) instruction programs every bit in the memory array to the logic '1' state and is primarily used for testing purposes. The Ready/$\overline{\text{Busy}}$ status of the AT59C11/12/13 can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin. The ERAL instruction is valid only at V_{CC} = 5.0 V ± 10%.

WRITE ALL (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The Ready/$\overline{\text{Busy}}$ status of the AT59C11/12/13 can be determined by polling the RDY/$\overline{\text{BUSY}}$ pin. The WRAL instruction is valid only at V_{CC} = 5.0 V ± 10%.

ERASE/WRITE DISABLE (EWDS): To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the READ instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

Instruction Set for the AT59C11

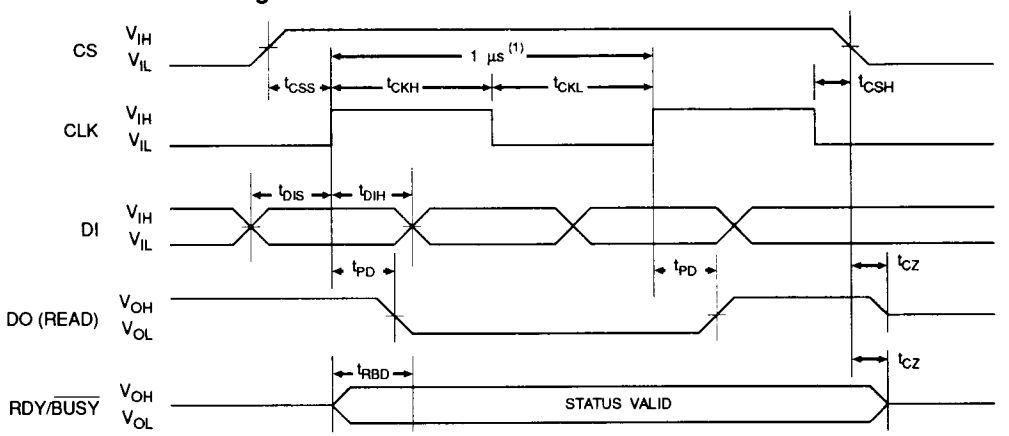
Instruction	SB	Op Code	Address x 8	Address x 16	Data x 8	Data x 16	Comments
READ	1	10XX	A_6-A_0	A_5-A_0			Reads data stored in memory, at specified address.
EWEN	1	0011	0000000	000000			Write enable must precede all programming modes.
WRITE	1	X1XX	A_6-A_0	A_5-A_0	D_7-D_0	D_{15}-D_0	Writes memory location A_n - A_0.
ERAL	1	0010	0000000	000000			Erases all memory locations. Valid only at V_{CC} = 4.5 V to 5.5 V.
WRAL	1	0001	0000000	000000	D_7-D_0	D_{15}-D_0	Writes all memory locations. Valid only at V_{CC} = 4.5 V to 5.5 V.
EWDS	1	0000	0000000	000000			Disables all programming instructions.

Instruction Set for the AT59C12 and AT59C13

Instruction	SB	Op Code	Address x 8	Address x 16	Data x 8	Data x 16	Comments
READ	1	10XX	A_8-A_0	A_7-A_0			Reads data stored in memory, at specified address.
EWEN	1	0011	000000000	00000000			Write enable must precede all programming modes.
WRITE	1	X1XX	A_8-A_0	A_7-A_0	D_7-D_0	D_{15}-D_0	Writes memory location A_n - A_0.
ERAL	1	0010	000000000	00000000			Erases all memory locations. Valid only at V_{CC} = 4.5 V to 5.5 V.
WRAL	1	0001	000000000	00000000	D_7-D_0	D_{15}-D_0	Writes all memory locations. Valid when V_{CC} = 5.0 V ± 10% and Disable Register cleared.
EWDS	1	0000	000000000	00000000			Disables all programming instructions.

Timing Diagrams

Synchronous Data Timing



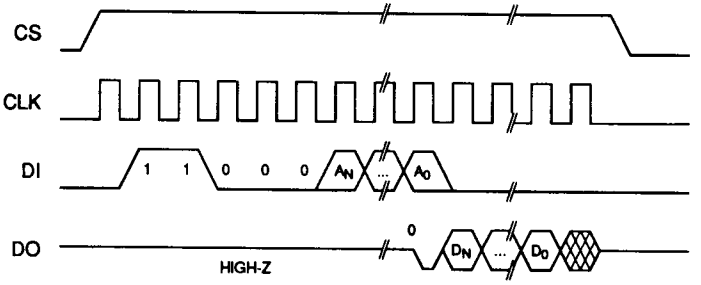
Note: 1. This is the minimum CLK period.

Organization Key for Timing Diagrams

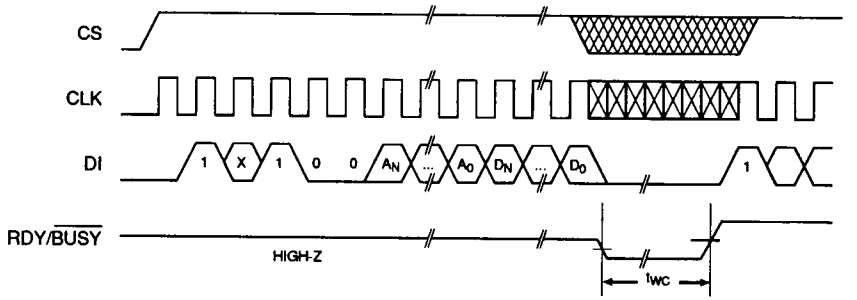
I/O	Density 1K x 8	Density 1K x 16	Density 2K x 8	Density 2K x 16	Density 4K x 8	Density 4K x 16
A_N	A_6	A_5	A_8	A_7	A_8	A7
D_N	D_7	D15	D7	D15	D7	D15

Timing Diagrams (Continued)

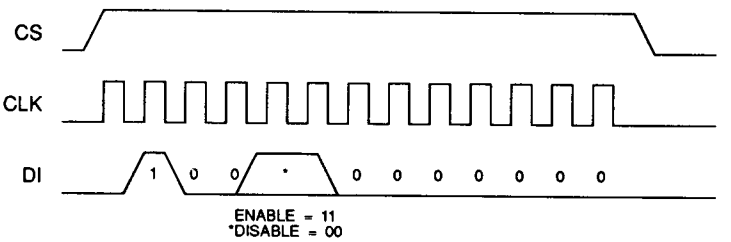
READ Timing



WRITE Timing

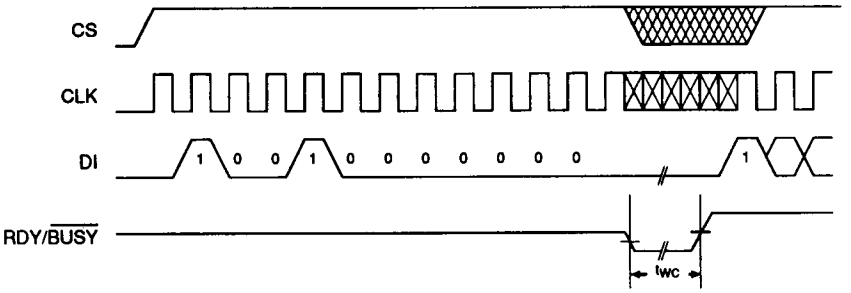


EWEN/EWDS Timing

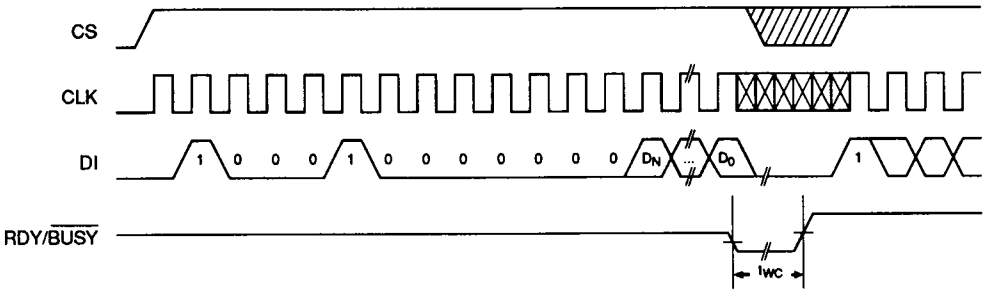


Timing Diagrams (Continued)

ERAL Timing



WRAL Timing



Ordering Information

twc (ms)	Icc (mA)	fMAX (kHz)	Ordering Code	Package	Operation Range
10	3.0	1000	AT59C11-10PC (-2.7) AT59C11-10SC (-2.7)	8P3 8S1	Commercial (0°C to 70°C)
			AT59C11-10PI (-2.7) AT59C11-10SI (-2.7)	8P3 8S1	Industrial (-40°C to 85°C)
			AT59C11-10PM	8P3	Military (-55°C to 125°C)
10	3.0	1000	AT59C12-10PC (-2.7) AT59C12-10SC (-2.7)	8P3 8S1	Commercial (0°C to 70°C)
			AT59C12-10PI (-2.7) AT59C12-10SI (-2.7)	8P3 8S1	Industrial (-40°C to 85°C)
			AT59C12-10PM	8P3	Military (-55°C to 125°C)
10	3.0	1000	AT59C13-10PC (-2.7) AT59C13-10SC (-2.7)	8P3 8S1	Commercial (0°C to 70°C)
			AT59C13-10PI (-2.7) AT59C13-10SI (-2.7)	8P3 8S1	Industrial (-40°C to 85°C)
			AT59C13-10PM	8P3	Military (-55°C to 125°C)

Package Type	
8P3	8 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S1	8 Lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
Options	
Blank	Standard Device (4.5 V to 5.5 V)
-2.7	Low Voltage (2.7 V to 5.5 V)