Document Title

128Kx36 & 256Kx18-Bit Synchronous Burst SRAM

Revision History

Rev. No.	History	Draft Date	Remark
0.0	Initial draft	jan. 22. 2000	Preliminary
0.1	1. Changed DC condition at Icc and I_{SB}. Icc ; from 320mA to 370mA at -65, from 300mA to 350mA at -75, from 280mA to 330mA at -80, from 260mA to 310mA at -90, I_{SB} ; from 130mA to 140mA at -65, from 120mA to 130mA at -75, from 110mA to 120mA at -80, from 100mA to 110mA at -90,	April. 03. 2000	Preliminary
1.0	Final spec release	May. 15. 2000	Final

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K7B403625A
K7B401825A
128Kx36 & 256Kx18 Synchronous SRAM

128Kx36 & 256Kx18-Bit Synchronous Burst SRAM

FEATURES

- Synchronous Operation.
- On-Chip Address Counter.
- Write Self-Timed Cycle.
- On-Chip Address and Control Registers.
- V_{DD}= 3.3V+0.3V/-0.165V Power Supply.
- V_{DDQ} Supply Voltage 3.3V+0.3V/-0.165V for 3.3V I/O or 2.5V+0.4V/-0.125V for 2.5V I/O.
- 5V Tolerant Inputs except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- Asynchronous Output Enable Control.
- $\overline{ADSP}$, ADSC, ADV Burst Control Pins.
- LBO Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention.
- TTL-Level Three-State Output.
- 100-TQFP-1420A

FAST ACCESS TIMES

PARAMETER	Symbol	-65	-75	-80	-90	Unit
Cycle Time	t_{CYC}	7.5	8.5	10	12	ns
Clock Access Time	t_{CD}	6.5	7.5	8.0	9.0	ns
Output Enable Access Time	t_{OE}	3.5	3.5	3.5	3.5	ns

GENERAL DESCRIPTION

The K7B403625A and K7B401825A are 4,718,592 bits Synchronous Static Random Access Memory designed to support zero wait state performance for advanced Pentium/Power PC based system. And with $\overline{CS}_1$ high, $\overline{ADSP}$ is blocked to control signals.

It can be organized as 128K(256K) words of 36(18) bits. And it integrates address and control registers, a 2-bit burst address counter and high output drive circuitry onto a single integrated circuit for reduced components counts implementation of high performance cache RAM applications.

Write cycles are internally self-timed and synchronous.

The self-timed write feature eliminates complex off chip write pulse shaping logic, simplifying the cache design and further reducing the component count.

Burst cycle can be initiated with either the address status processor($\overline{ADSP}$) or address status cache controller($\overline{ADSC}$) inputs. Subsequent burst addresses are generated internally in the system's burst sequence and are controlled by the burst address advance($\overline{ADV}$) input.

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The K7B403625A and K7B401825A are implemented with SAMSUNG's high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM

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K7B403625A
K7B401825A

128Kx36 & 256Kx18 Synchronous SRAM

PIN CONFIGURATION (TOP VIEW)

100 Pin TQFP
(20mm x 14mm)
K7B403625A(128Kx36)

PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A16	Address Inputs	32,33,34,35,36,37 44,45,46,47,48,49 50,81,82,99,100	VDD VSS	Power Supply(+3.3V) Ground	15,41,65,91 17,40,67,90
$\overline{ADV}$	Burst Address Advance	83	N.C.	No Connect	14,16,38,39,42,43,66
$\overline{ADSP}$	Address Status Processor	84			
$\overline{ADSC}$	Address Status Controller	85	DQa0~a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
CLK	Clock	89	DQb0~b7		68,69,72,73,74,75,78,79
$\overline{CS_1}$	Chip Select	98	DQc0~c7		2,3,6,7,8,9,12,13
$\overline{CS_2}$	Chip Select	97	DQd0~d7		18,19,22,23,24,25,28,29
CS2	Chip Select	92	DQPa~Pd		51,80,1,30
$\overline{WEx}$	Byte Write Inputs	93,94,95,96			
(x=a,b,c,d)			VDDQ	Output Power Supply (2.5V or 3.3V)	4,11,20,27,54,61,70,77
$\overline{OE}$	Output Enable	86			
$\overline{GW}$	Global Write Enable	88	VSSQ	Output Ground	5,10,21,26,55,60,71,76
BW	Byte Write Enable	87			
$\overline{ZZ}$	Power Down Input	64			
$\overline{LBO}$	Burst Mode Control	31			

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128Kx36 & 256Kx18 Synchronous SRAM

PIN CONFIGURATION(TOP VIEW)

Top pins (left to right): A6, A7, $\overline{CS_1}$, CS_2, N.C., N.C., $\overline{WEb}$, $\overline{WEa}$, $\overline{CS_2}$, V_{DD}, V_{SS}, CLK, $\overline{GW}$, $\overline{BW}$, $\overline{OE}$, $\overline{ADSC}$, $\overline{ADSP}$, $\overline{ADV}$, A8, A9

Left pins (top to bottom, 1–30): N.C. (1), N.C. (2), N.C. (3), V_{DDQ} (4), V_{SSQ} (5), N.C. (6), N.C. (7), DQb0 (8), DQb1 (9), V_{SSQ} (10), V_{DDQ} (11), DQb2 (12), DQb3 (13), N.C. (14), V_{DD} (15), N.C. (16), V_{SS} (17), DQb4 (18), DQb5 (19), V_{DDQ} (20), V_{SSQ} (21), DQb6 (22), DQb7 (23), DQPb (24), N.C. (25), V_{SSQ} (26), V_{DDQ} (27), N.C. (28), N.C. (29), N.C. (30)

Right pins (top to bottom, 80–51): A10 (80), N.C. (79), N.C. (78), V_{DDQ} (77), V_{SSQ} (76), N.C. (75), DQPa (74), DQa7 (73), DQa6 (72), V_{SSQ} (71), V_{DDQ} (70), DQa5 (69), DQa4 (68), V_{SS} (67), N.C. (66), V_{DD} (65), ZZ (64), DQa3 (63), DQa2 (62), V_{DDQ} (61), V_{SSQ} (60), DQa1 (59), DQa0 (58), N.C. (57), N.C. (56), V_{SSQ} (55), V_{DDQ} (54), N.C. (53), N.C. (52), N.C. (51)

Bottom pins (pins 31–50, left to right): $\overline{LBO}$ (31), A5 (32), A4 (33), A3 (34), A2 (35), A1 (36), A0 (37), N.C. (38), N.C. (39), V_{SS} (40), V_{DD} (41), N.C. (42), N.C. (43), A11 (44), A12 (45), A13 (46), A14 (47), A15 (48), A16 (49), A17 (50)

Center label:
100 Pin TQFP
(20mm x 14mm)
K7B401825A(256Kx18)

PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A17	Address Inputs	32,33,34,35,36,37, 44,45,46,47,48,49, 50,80,81,82,99,100	V_{DD} V_{SS} N.C.	Power Supply(+3.3V) Ground No Connect	15,41,65,91 17,40,67,90 1,2,3,6,7,14,16,25,28,29, 30,38,39,42,43,51,52,53, 56,57,66,75,78,79,95,96
$\overline{ADV}$	Burst Address Advance	83			
$\overline{ADSP}$	Address Status Processor	84			
$\overline{ADSC}$	Address Status Controller	85			
CLK	Clock	89	DQa0~a7	Data Inputs/Outputs	58,59,62,63,68,69,72,73
$\overline{CS_1}$	Chip Select	98	DQb0~b7		8,9,12,13,18,19,22,23
CS_2	Chip Select	97	DQPa, Pb		74,24
$\overline{CS_2}$	Chip Select	92	V_{DDQ}	Output Power Supply	4,11,20,27,54,61,70,77
WEx	Byte Write Inputs	93,94		(2.5V or 3.3V)	
(x=a,b)			V_{SSQ}	Output Ground	5,10,21,26,55,60,71,76
$\overline{OE}$	Output Enable	86			
$\overline{GW}$	Global Write Enable	88			
$\overline{BW}$	Byte Write Enable	87			
$\overline{ZZ}$	Power Down Input	64			
$\overline{LBO}$	Burst Mode Control	31			

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FUNCTION DESCRIPTION

The K7B403625A and K7B401825A are synchronous SRAM designed to support the burst address accessing sequence of the Pentium and Power PC based microprocessor. All inputs (with the exception of $\overline{OE}$, LBO and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by $\overline{ADSC}$, $\overline{ADSP}$ and $\overline{ADV}$ and chip select pins.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with $\overline{ADSP}$(or $\overline{ADSC}$) using the new external address clocked into the on-chip address register when both $\overline{GW}$ and $\overline{BW}$ are high or when $\overline{BW}$ is low and $\overline{WEa}$, $\overline{WEb}$, $\overline{WEc}$, and $\overline{WEd}$ are high. When $\overline{ADSP}$ is sampled low, the chip selects are sampled active, and the output buffer is enabled with $\overline{OE}$. the data of cell array accessed by the current address are projected to the output pins.

Write cycles are also initiated with $\overline{ADSP}$(or $\overline{ADSC}$) and are differentiated into two kinds of operations; All byte write operation and individual byte write operation.
All byte write occurs by enabling $\overline{GW}$(independent of $\overline{BW}$ and $\overline{WEx}$.), and individual byte write is performed only when $\overline{GW}$ is high and $\overline{BW}$ is low. In KM736V787, a 128Kx36 organization, $\overline{WEa}$ controls DQa0 ~ DQa7 and DQPa, $\overline{WEb}$ controls DQb0 ~ DQb7 and DQPb, $\overline{WEc}$ controls DQc0 ~ DQc7 and DQPc and $\overline{WEd}$ controls DQd0 ~ DQd7 and DQPd.

$\overline{CS}_1$ is used to enable the device and conditions internal use of $\overline{ADSP}$ and is sampled only when a new external address is loaded.

$\overline{ADV}$ is ignored at the clock edge when $\overline{ADSP}$ is asserted, but can be sampled on the subsequent clock edges. The address increases internally for the next access of the burst when $\overline{ADV}$ is sampled low.

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO pin. When this pin is Low, linear burst sequence is selected. And this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE
(Interleaved Burst)

$\overline{LBO}$ PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A$_1$	A$_0$	A$_1$	A$_0$	A$_1$	A$_0$	A$_1$	A$_0$
First Address		0	0	0	1	1	0	1	1
↓		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

Note : 1. $\overline{LBO}$ pin must be tied to high or low, and floating state must not be allowed.

(Linear Burst)

$\overline{LBO}$ PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A$_1$	A$_0$	A$_1$	A$_0$	A$_1$	A$_0$	A$_1$	A$_0$
First Address		0	0	0	1	1	0	1	1
↓		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

Note : 1. $\overline{LBO}$ pin must be tied to high or low, and floating state must not be allowed.

ASYNCHRONOUS TRUTH TABLE
(See Notes 1 and 2):

OPERATION	ZZ	$\overline{OE}$	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffersmust be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

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TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CS_1}$	CS₂	$\overline{CS_2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	ADDRESS ACCESSED	OPERATION
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

Notes : 1. X means "Don't Care".   2. The rising edge of clock is symbolized by ↑.

3. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.

$\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.

4. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE(x36)

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	$\overline{WEc}$	$\overline{WEd}$	OPERATION
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTEs
L	X	X	X	X	X	WRITE ALL BYTEs

Notes : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

WRITE TRUTH TABLE(x18)

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	OPERATION
H	H	X	X	READ
H	L	H	H	READ
H	L	L	H	WRITE BYTE a
H	L	H	L	WRITE BYTE b
H	L	L	L	WRITE ALL BYTEs
L	X	X	X	WRITE ALL BYTEs

Notes : 1. X means "Don't Care".

2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

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K7B403625A
K7B401825A   128Kx36 & 256Kx18 Synchronous SRAM

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.3 to 4.6	V
Voltage on V_{DDQ} Supply Relative to V_{SS}	V_{DDQ}	-0.3 to 4.6	V
Voltage on Input Pin Relative to V_{SS}	V_{IN}	-0.3 to V_{DD}+0.5	V
Voltage on I/O Pin Relative to V_{SS}	V_{IO}	-0.3 to V_{DDQ}+0.5	V
Power Dissipation	P_D	1.4	W
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_{OPR}	0 to 70	°C
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	°C

*Note : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS at 3.3V I/O (0°C≤ T_A≤70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V_{DD}	3.135	3.3	3.6	V
	V_{DDQ}	3.135	3.3	3.6	V
Ground	V_{SS}	0	0	0	V

OPERATING CONDITIONS at 2.5V I/O (0°C ≤ T_A ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V_{DD}	3.135	3.3	3.6	V
	V_{DDQ}	2.375	2.5	2.9	V
Ground	V_{SS}	0	0	0	V

CAPACITANCE*(T_A=25°C, f=1MHz)

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	7	pF

*Note : Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS(TA=0 to 70°C, VDD=3.3V+0.3V/-0.165V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNIT
Input Leakage Current(except ZZ)	IIL	VDD=Max , VIN=VSS to VDD		-2	+2	μA
Output Leakage Current	IOL	Output Disabled, VOUT=VSS to VDDQ		-2	+2	μA
Operating Current	ICC	Device Selected, IOUT=0mA, ZZ≤VIL, All Inputs=VIL or VIH Cycle Time ≥ tCYC min	-65	-	370	mA
			-75	-	350	
			-80	-	330	
			-90	-	310	
Standby Current	ISB	Device deselected, IOUT=0mA, ZZ≤VIL, f=Max, All Inputs≤0.2V or ≥ VDD-0.2V	-65	-	140	mA
			-75	-	130	
			-80	-	120	
			-90	-	110	
	ISB1	Device deselected, IOUT=0mA, ZZ≤0.2V, f=0, All Inputs=fixed (VDD-0.2V or 0.2V)		-	100	mA
	ISB2	Device deselected, IOUT=0mA, ZZ≥VDD-0.2V, f=Max, All Inputs≤VIL or ≥VIH		-	50	mA
Output Low Voltage(3.3V I/O)	VOL	IOL = 8.0mA		-	0.4	V
Output High Voltage(3.3V I/O)	VOH	IOH = -4.0mA		2.4	-	V
Output Low Voltage(2.5V I/O)	VOL	IOL = 1.0mA		-	0.4	V
Output High Voltage(2.5V I/O)	VOH	IOH = -1.0mA		2.0	-	V
Input Low Voltage(3.3V I/O)	VIL			-0.5*	0.8	V
Input High Voltage(3.3V I/O)	VIH			2.0	VDD+0.5**	V
Input Low Voltage(2.5V I/O)	VIL			-0.3*	0.7	V
Input High Voltage(2.5V I/O)	VIH			1.7	VDD+0.5**	V

*   VIL(Min)=-2.0(Pulse Width ≤ tCYC/2)

** VIH(Max)=4.6(Pulse Width ≤ tCYC/2)

** In Case of I/O Pins, the Max. VIH=VDDQ+0.5V

TEST CONDITIONS
(VDD=3.3V+0.3V/-0.165V,VDDQ=3.3V+0.3/-0.165V or VDD=3.3V+0.3V/-0.165V,VDDQ=2.5V+0.4V/-0.125V, TA=0 to 70°C)

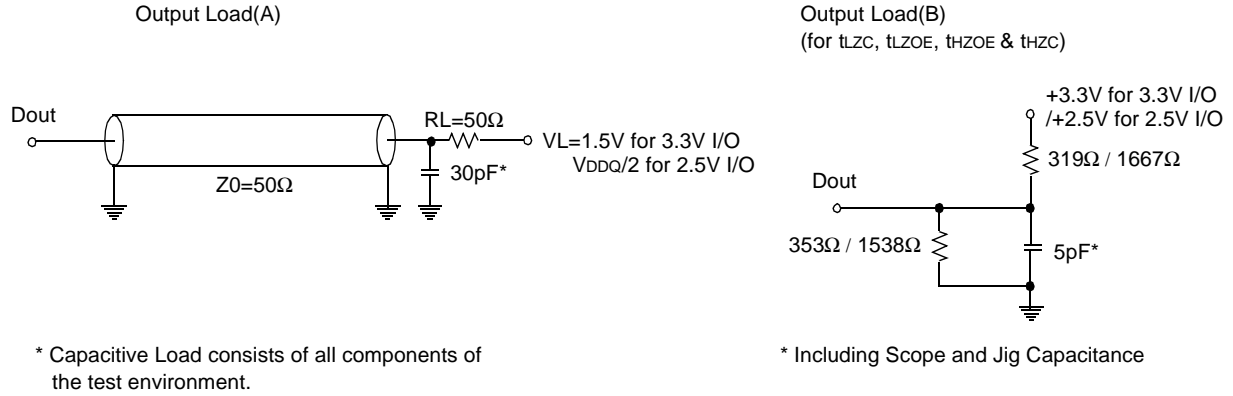| PARAMETER	VALUE
Input Pulse Level(for 3.3V I/O)	0 to 3V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 0.3V and 2.7V for 3.3V I/O)	1ns
Input Rise and Fall Time(Measured at 0.3V and 2.1V for 2.5V I/O)	1ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	VDDQ/2
Output Load	See Fig. 1

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Output Load(A)

Output Load(B)
(for t_{LZC}, t_{LZOE}, t_{HZOE} & t_{HZC})

Dout

RL=50Ω

VL=1.5V for 3.3V I/O
V_{DDQ}/2 for 2.5V I/O

Z0=50Ω

30pF*

+3.3V for 3.3V I/O
/+2.5V for 2.5V I/O

319Ω / 1667Ω

Dout

353Ω / 1538Ω

5pF*

* Capacitive Load consists of all components of
the test environment.

* Including Scope and Jig Capacitance

Fig. 1

AC TIMING CHARACTERISTICS (T_A=0 to 70°C, V_{DD}=3.3V+0.3V/-0.165V)

PARAMETER	Symbol	-65		-75		-80		-90		UNIT
		Min	Max	Min	Max	Min	Max	Min	Max	
Cycle Time	t_{CYC}	7.5	-	8.5	-	10	-	12	-	ns
Clock Access Time	t_{CD}	-	6.5	-	7.5	-	8.0	-	9.0	ns
Output Enable to Data Valid	t_{OE}	-	3.5	-	3.5	-	3.5	-	3.5	ns
Clock High to Output Low-Z	t_{LZC}	0	-	0	-	0	-	0	-	ns
Output Hold from Clock High	t_{OH}	2.5	-	2.5	-	2.5	-	2.5	-	ns
Output Enable Low to Output Low-Z	t_{LZOE}	0	-	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	t_{HZOE}	-	3.5	-	3.5	-	3.5	-	3.5	ns
Clock High to Output High-Z	t_{HZC}	2	3.5	2	3.5	2	3.5	2	3.5	ns
Clock High Pulse Width	t_{CH}	2.5	-	3	-	4	-	4.5	-	ns
Clock Low Pulse Width	t_{CL}	2.5	-	3	-	4	-	4.5	-	ns
Address Setup to Clock High	t_{AS}	1.5	-	2.0	-	2.0	-	2.0	-	ns
Address Status Setup to Clock High	t_{SS}	1.5	-	2.0	-	2.0	-	2.0	-	ns
Data Setup to Clock High	t_{DS}	1.5	-	2.0	-	2.0	-	2.0	-	ns
Write Setup to Clock High($\overline{GW}$, $\overline{BW}$, $\overline{WEx}$)	t_{WS}	1.5	-	2.0	-	2.0	-	2.0	-	ns
Address Advance Setup to Clock High	t_{ADVS}	1.5	-	2.0	-	2.0	-	2.0	-	ns
Chip Select Setup to Clock High	t_{CSS}	1.5	-	2.0	-	2.0	-	2.0	-	ns
Address Hold from Clock High	t_{AH}	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	t_{SH}	0.5	-	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	t_{DH}	0.5	-	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High($\overline{GW}$, $\overline{BW}$, $\overline{WEx}$)	t_{WH}	0.5	-	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	t_{ADVH}	0.5	-	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	t_{CSH}	0.5	-	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	t_{PDS}	2	-	2	-	2	-	2	-	cycle
ZZ Low to Power Up	t_{PUS}	2	-	2	-	2	-	2	-	cycle

Notes : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and
CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
2. Both chip selects must be active whenever ADSC or ADSP is sampled low in order for the this device to remain enabled.
3. ADSC or ADSP must not be asserted for at least 2 Clock after leaving ZZ state.
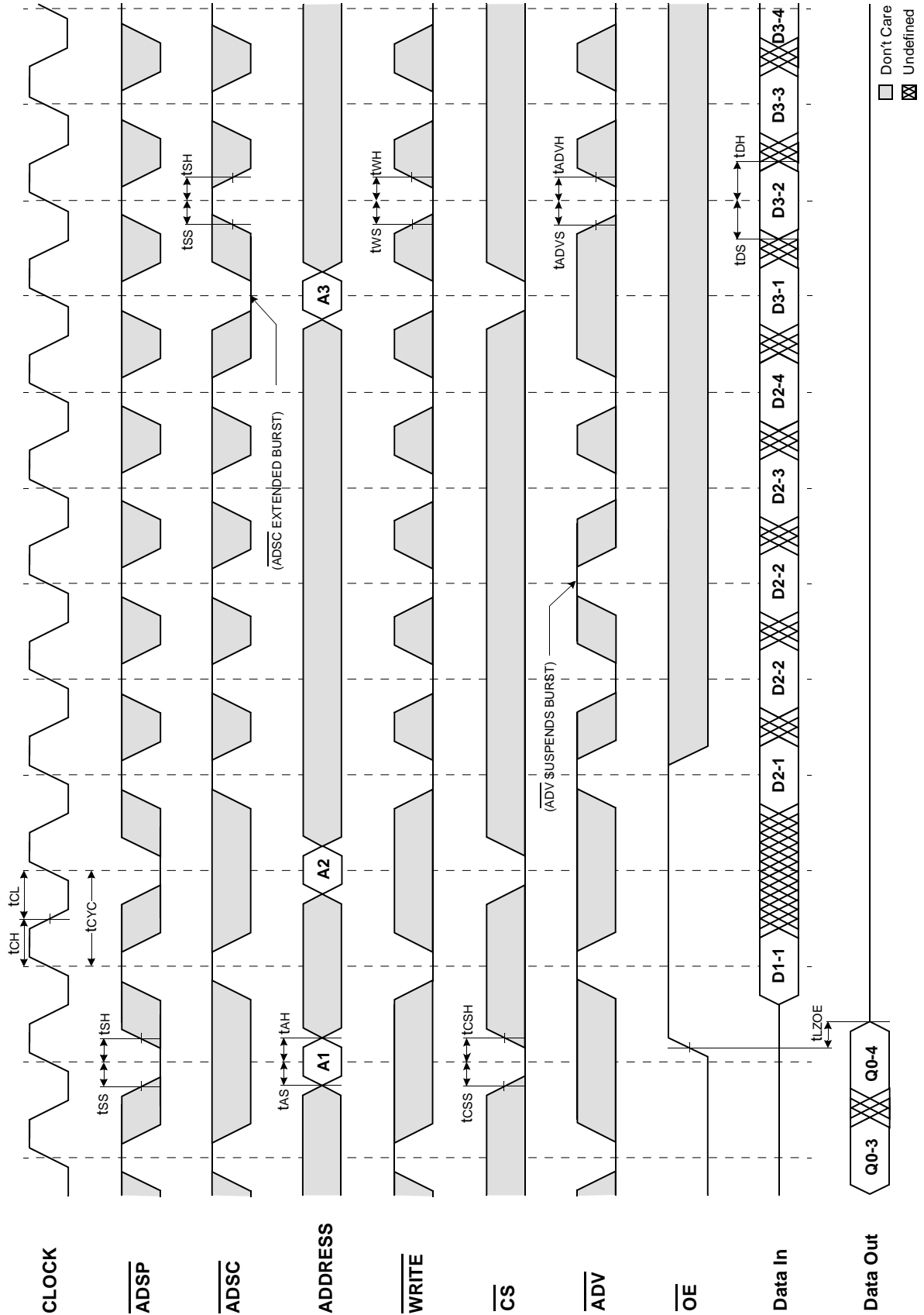4. At any given voltage and temperature, t_{HZC} is less than t_{LZC}.

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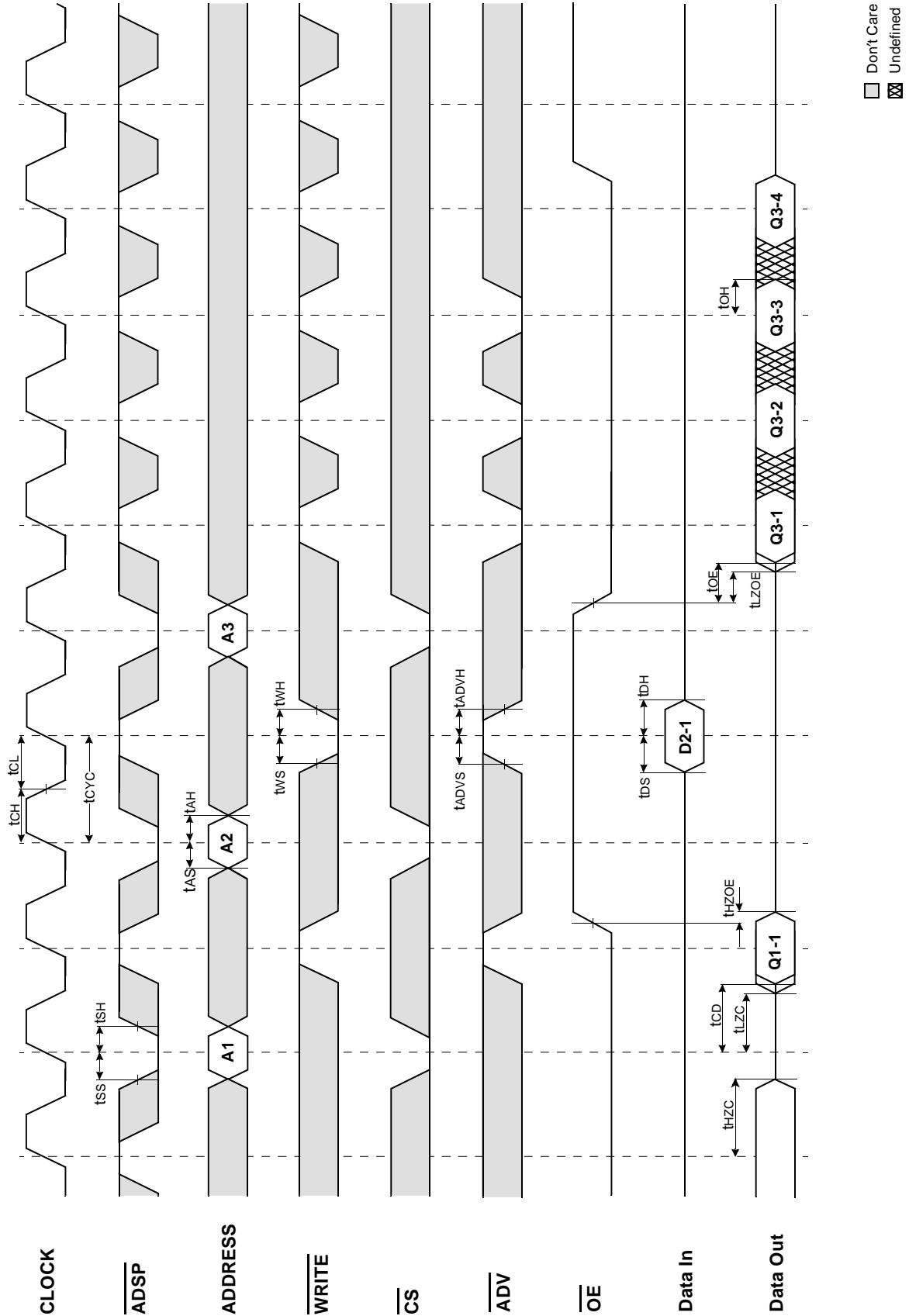**TIMING WAVEFORM OF READ CYCLE**
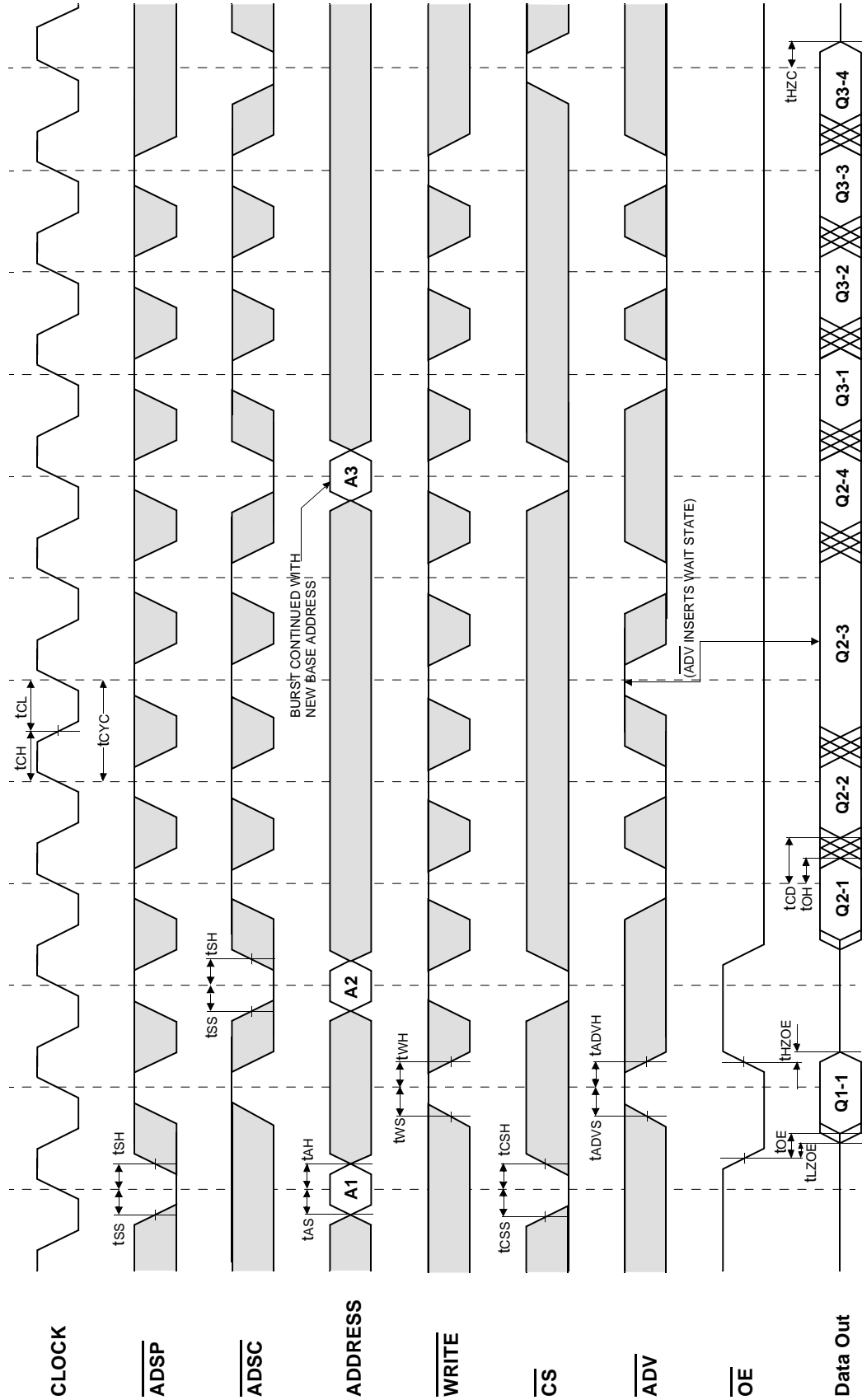
NOTES : WRITE = L means GW = L, or GW = H, BW = L, WEx = L
CS = L means CS1 = L, CS2 = H and CS2 = L
CS = H means CS1 = H, or CS1 = L and CS2 = H, or CS1 = L, and CS2 = L

Don't Care
Undefined

K7B403625A
K7B401825A

128Kx36 & 256Kx18 Synchronous SRAM

TIMING WAVEFORM OF WRITE CYCLE

CLOCK
$\overline{ADSP}$
$\overline{ADSC}$
ADDRESS
$\overline{WRITE}$
$\overline{CS}$
$\overline{ADV}$
$\overline{OE}$
Data In
Data Out

SAMSUNG
ELECTRONICS

May 2000
Rev 1.0

TIMING WAVEFORM OF COMBINATION READ/WRITE CYCLE(ADSP CONTROLLED, ADSC=HIGH)

Don't Care
Undefined

CLOCK

ADSP

ADDRESS

WRITE

CS

ADV

OE

Data In

Data Out

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TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSC CONTROLLED, ADSP=HIGH)

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Rev 1.0

TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSP CONTROLLED, ADSC=HIGH)

Signal rows: CLOCK, ADSP, ADDRESS, WRITE, CS, ADV, OE, Data Out, Data In

Address values: A1, A2, A3, A4, A5, A6, A7, A8, A9

Data Out values: Q1-1, Q2-1, Q3-1, Q4-1, Q8-1, Q9-1

Data In values: D5-1, D6-1, D7-1

Timing parameters: tSS, tSH, tCH, tCL, tCYC, tAS, tAH, tCSS, tCSH, toE, tLZOE, tHZOE, tCD, toH, tDS, tDH

Legend: Don't Care, Undefined
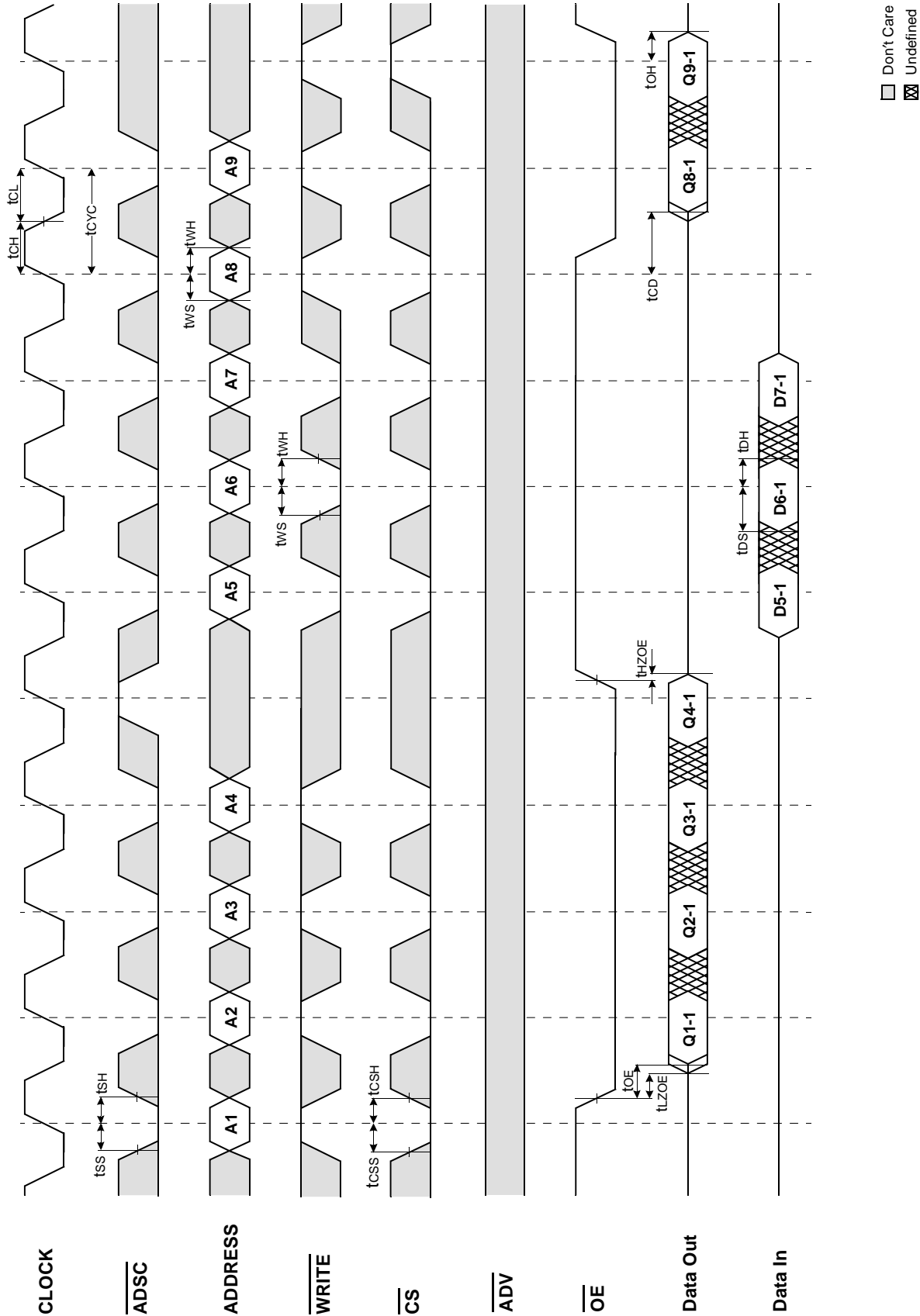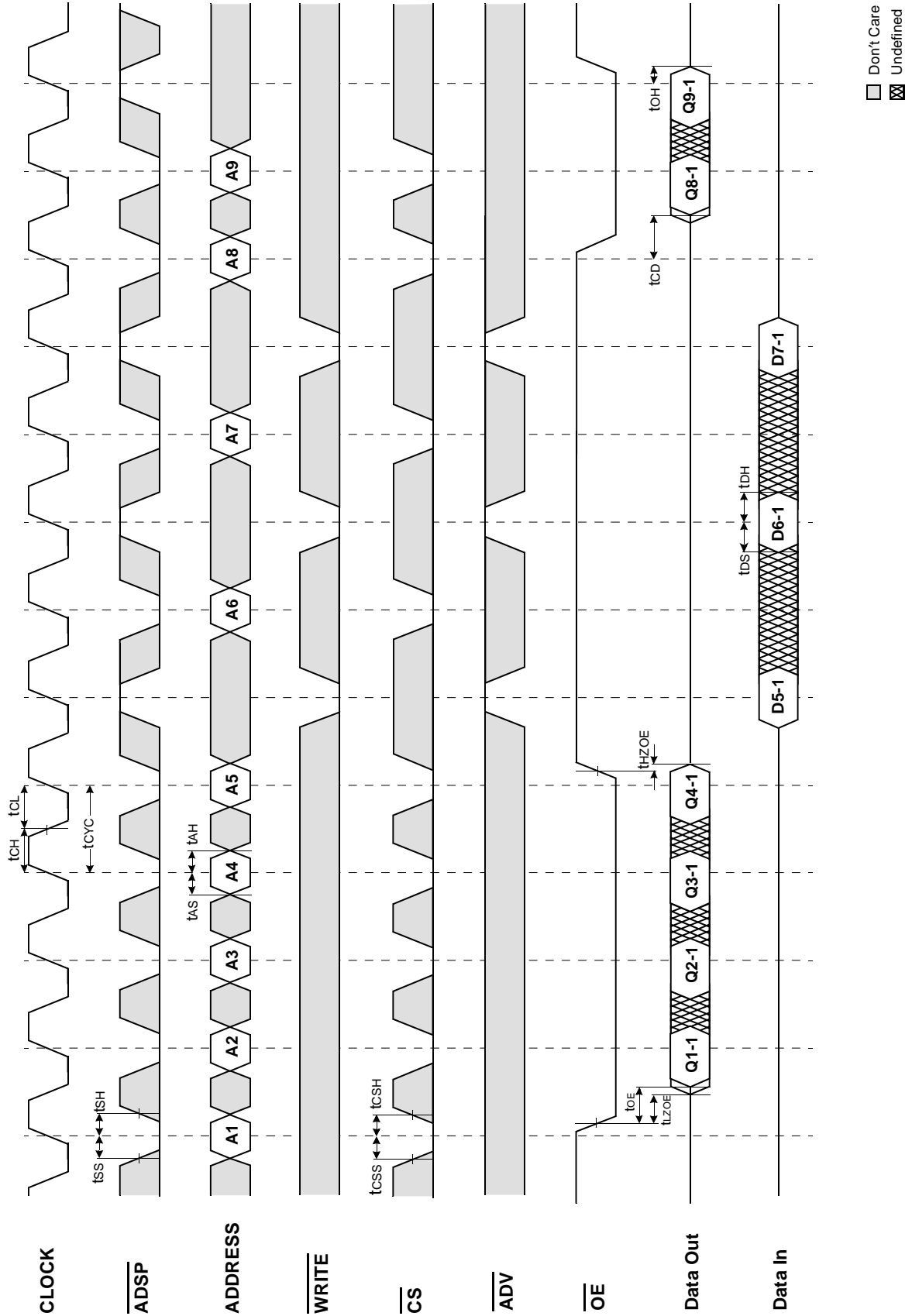
TIMING WAVEFORM OF POWER DOWN CYCLE

CLOCK

$\overline{ADSP}$

$\overline{ADSC}$

ADDRESS

$\overline{WRITE}$

$\overline{CS}$

$\overline{ADV}$

OE

Data In

Data Out

ZZ

tSS, tSH, tAS, tAH, tCSS, tCSH, tOE, tLZOE, tCH, tCL, tCYC, tWS, tWH, tHZOE, tHZC, tPDS, tPUS

A1, A2, Q1-1, D2-1, D2-2

ZZ Setup Cycle, Sleep State, ZZ Recovery Cycle, Normal Operation Mode

Don't Care

Undefined

SAMSUNG

ELECTRONICS
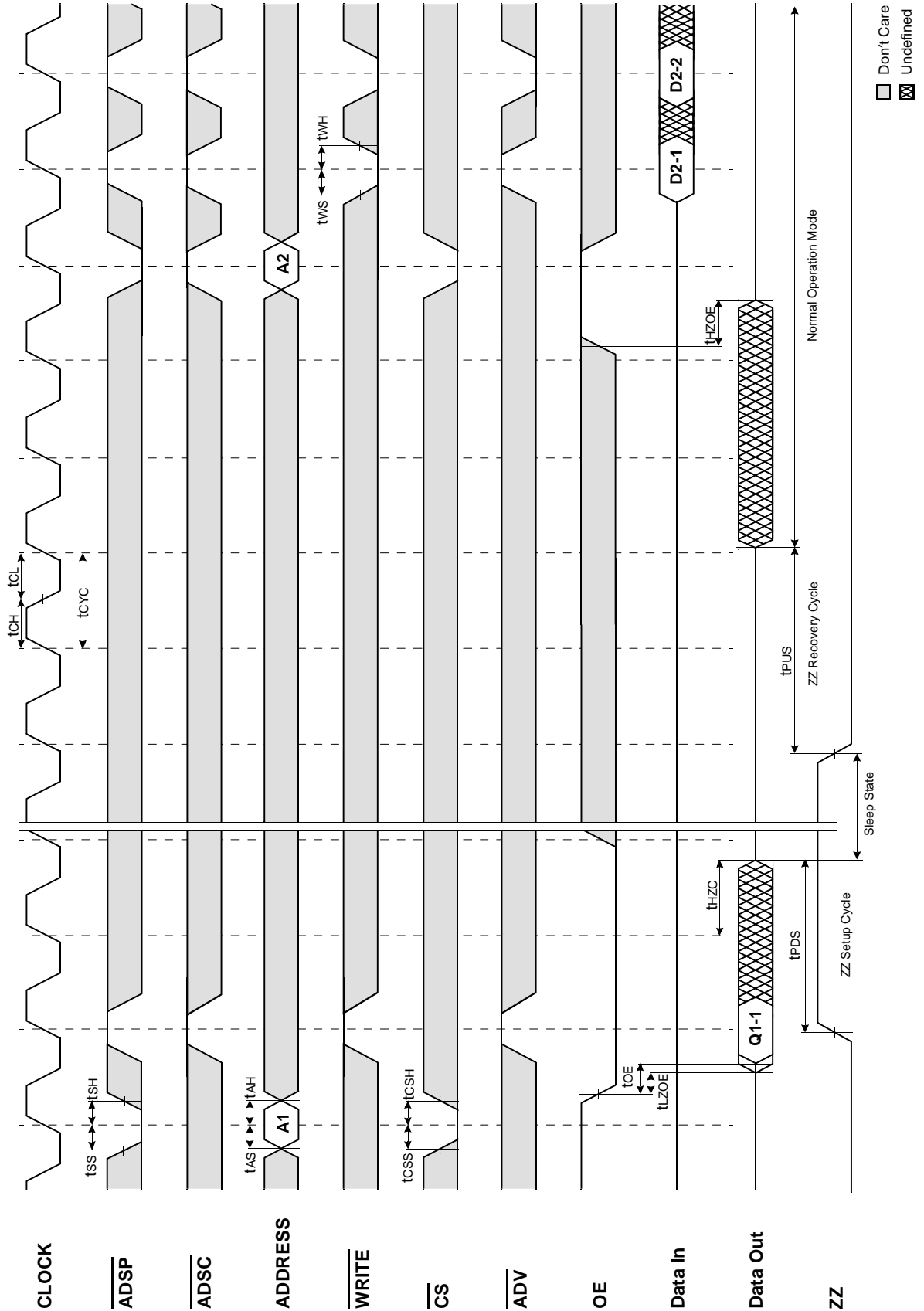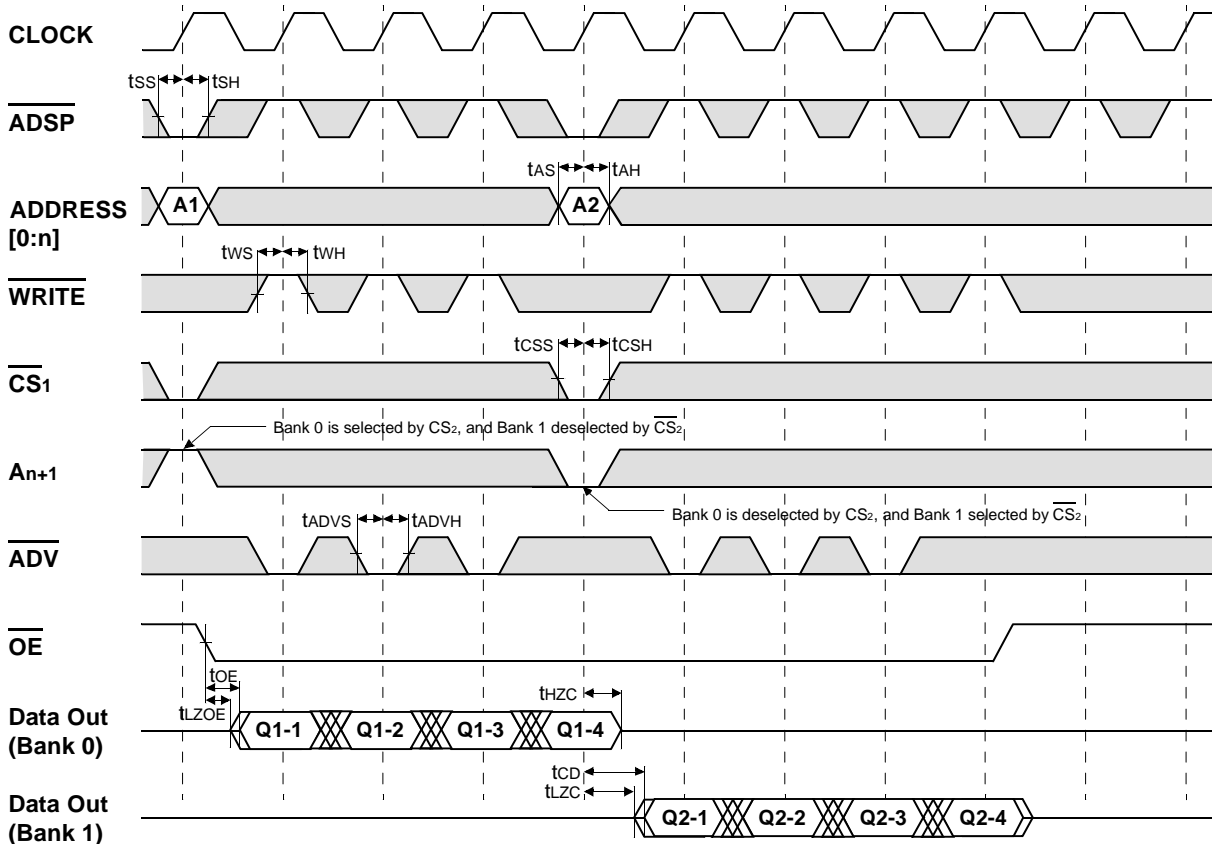
APPLICATION INFORMATION

DEPTH EXPANSION

The Samsung 128Kx36 Synchronous Burst SRAM has two additional chip selects for simple depth expansion.
This permits easy secondary cache upgrades from 128K depth to 256K depth without extra logic.
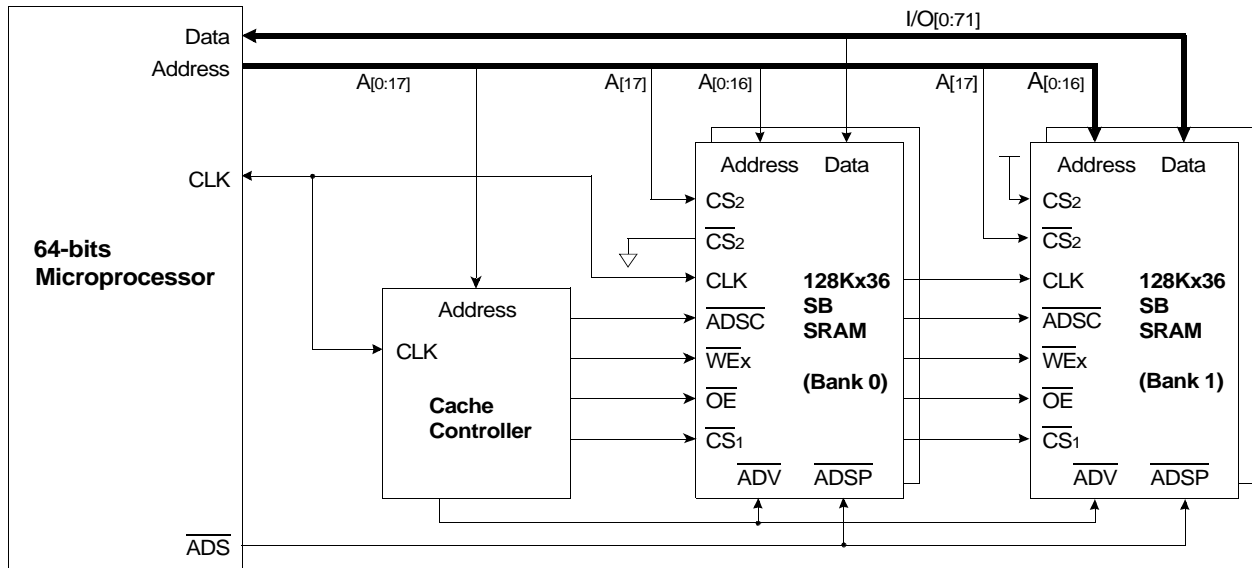
INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

(ADSP CONTROLLED , ADSC=HiGH)

*Notes : n = 14 32K depth, 15 64K depth, 16 128K depth, 17 256K depth

☐ Don't Care   ☒ Undefined

PACKAGE DIMENSIONS

100-TQFP-1420A   Units:millimeters/inches

22.00 ±0.30

20.00 ±0.20

16.00 ±0.30

14.00 ±0.20

(0.83)

#1

0.65

0.30 ±0.10

0.10 MAX

(0.58)

0~8°

0.127 $^{+0.10}_{-0.05}$

0.10 MAX

0.50 ±0.10

1.40 ±0.10   1.60 MAX

0.05 MIN

0.50 ±0.10