Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS 9-BIT REGISTER

ADVANCE INFORMATION
IDT54/74FBT823A
IDT54/74FBT823B
IDT54/74FBT823C

FEATURES:

- IDT54/74FBT823A equivalent to 54/74BCT823A
- **IDT54/74FBT823B 25% faster than the 823A**
- **IDT54/74FBT823C 10% faster than the 823B**
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- Low power in all three states
- ±10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

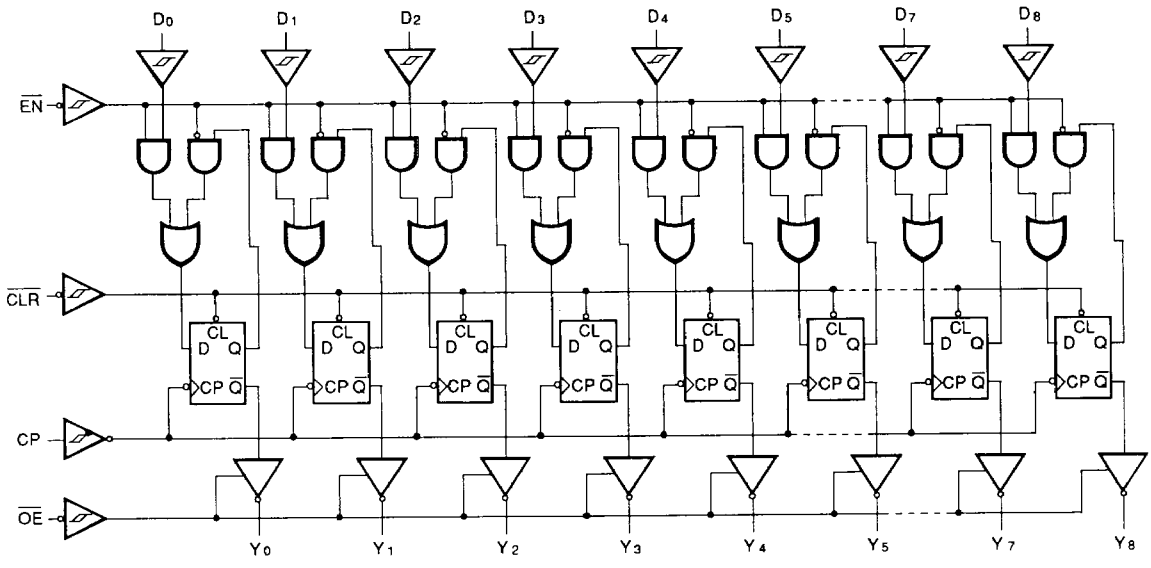
DESCRIPTION:

The FBT series of BiCMOS buffers and bus drivers are built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

The IDT54/74FBT823 is a 9-bit wide buffered register with Clock Enable ($\overline{EN}$) and Clear ($\overline{CLR}$). The '823 is ideal for parity bus interfacing in high-peformance microprogrammed systems.

The FBT series of buffers are ideal for use in designs needing to drive large capacitive loads with low static (DC) current loading. All data inputs have a 200mV typical input hysteresis for improved noise rejection.

FUNCTIONAL BLOCK DIAGRAM



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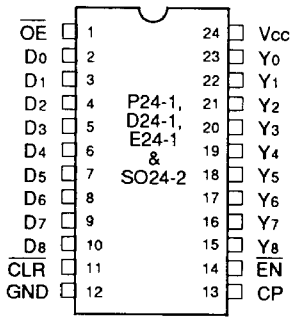
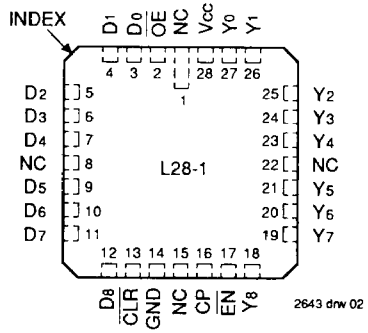
PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTION

Name	I/O	Description
D_{0-8}	I	The D flip-flop data inputs.
$\overline{CLR}$	I	For both inverting and non-inverting registers, when the clear input is LOW, the Q_I outputs are LOW. When the clear input is HIGH, data can be entered into the register.
CP	I	Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.
Y_0- Y_8	O	The register three-state outputs.
$\overline{EN}$	I	Clock Enable. When the Clock Enable is LOW, data on the D_I input is transferred to the Q_I output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q_I outputs do not change state, regardless of the data or clock input transitions.
$\overline{OE}$	I	Output Control. When the $\overline{OE}$ input is HIGH, the Y_I outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_I outputs.

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FUNCTION TABLE[1]

Inputs					Internal Outputs		
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_I	CP	Q_I	Y_I	Function
H	H	L	L	↑	L	Z	High Z
H	H	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

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NOTE:
1. H = HIGH
   L = LOW
   X = Don't Care
   NC = No Change
   ↑ = LOW-to-HIGH Transition
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE: 2643 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE: 2643 tbl 02

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%; Military: T_A = -55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_I = 2.7V		—	—	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_I = .5V		—	—	-10	µA
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = 2.7V	—	—	50	µA
I_{OZL}			V_O = .5V	—	—	-50	
I_I	Input HIGH Current	V_{CC} = Max., V_I = 5.5V		—	—	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		—	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND(3)		-75	—	-225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -12mA MIL. I_{OH} = -15mA COM'L.	2.4	3.3	—	V
			I_{OH} = -18mA MIL. I_{OH} = -24mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage		I_{OL} = 32mA MIL. I_{OL} = 48mA COM'L.	—	0.3	0.5	V
V_H	Input Hysteresis	V_{CC} = 5V		—	200	—	mV
I_{OFF}	Bus Leakage Current	V_{CC} = 0V, V_O = 4.5V		—	—	100	µA
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

NOTES: 2643 tbl 05

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	V_{CC} = Max., Outputs Open V_{IN} = 3.4V[3]		—	—	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}$ = $\overline{GND}$ One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	4.0	mA
		$\overline{OE}$ = $\overline{GND}$ One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	5.0	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	—	7.2[5]	
		$\overline{OE}$ = $\overline{GND}$ Eight Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	—	16.2[5]	

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NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient, and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	IDT54/74FBT823A				IDT54/74FBT823B				IDT54/74FBT823C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPLH tPHL	Propagation Delay Clock to Yi ($\overline{OE}$ = LOW)	CL = 50pF RL = 500Ω	—	10	—	—	—	7.5	—	—	—	6.0	—	—	ns
tSU	Data to CP Set-up Time		7	—	—	—	3	—	—	—	3	—	—	—	ns
tH	Data CP Hold Time		1.5	—	—	—	1.5	—	—	—	1.5	—	—	—	ns
tSU	Enable ($\overline{EN}$) to CP Set-up Time		6	—	—	—	3	—	—	—	3	—	—	—	ns
tH	Enable ($\overline{EN}$) to CP Hold Time		0	—	—	—	0	—	—	—	0	—	—	—	ns
tPHL	Propagation Delay, Clear to Yi		—	12	—	—	—	9	—	—	—	8.0	—	—	ns
tREM	Clear Recovery ($\overline{CLR}$)Time		6	—	—	—	6	—	—	—	6	—	—	—	ns
tW	Clock Pulse Width		7	—	—	—	6	—	—	—	6	—	—	—	ns
tW	Clear ($\overline{CLR}$=LOW) Pulse Width		6	—	—	—	6	—	—	—	6	—	—	—	ns
tPZH tPZL	Output EnableTime $\overline{OE}$ to Yi		—	12	—	—	—	8	—	—	—	7.0	—	—	ns
tPHZ tPLZ	Output Disable Time $\overline{OE}$ to Yi		—	8	—	—	—	7.5	—	—	—	6.5	—	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

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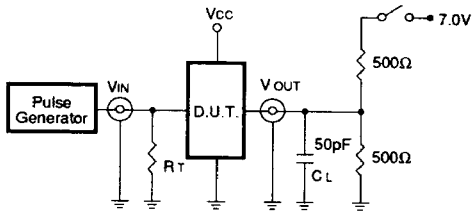
TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



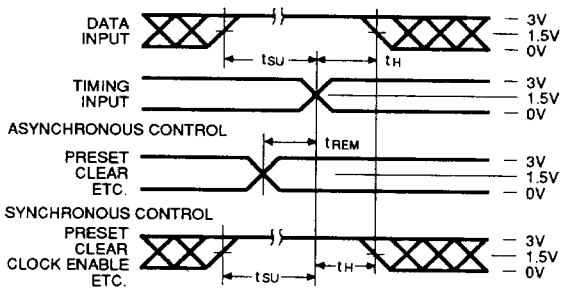
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

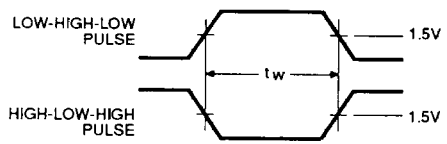
DEFINITIONS: 2643 tbl 08

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

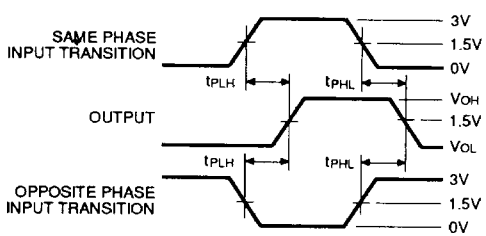
SET-UP, HOLD AND RELEASE TIMES



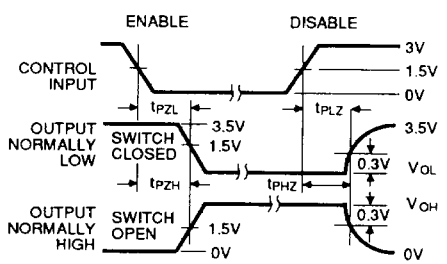
PULSE WIDTH



PROPAGATION DELAY



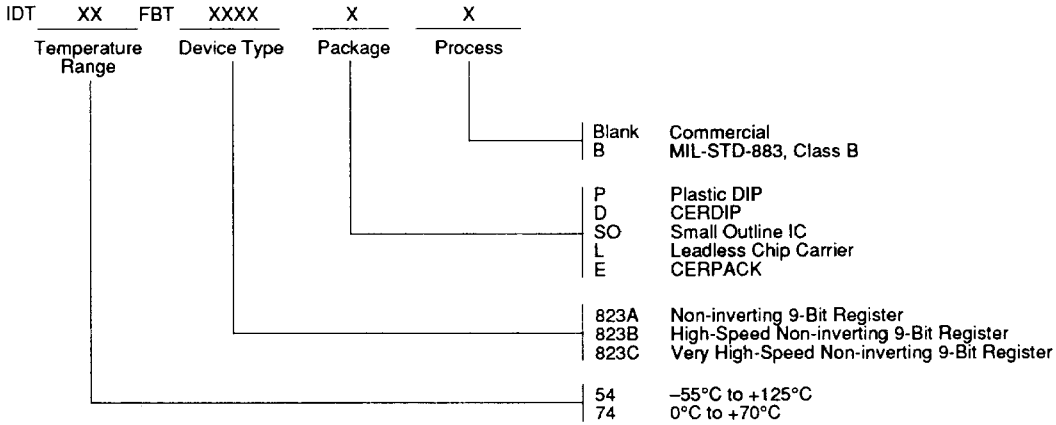
ENABLE AND DISABLE TIMES



NOTES 2643 drw 04

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Z_O ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



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