GD54/74LS109A

DUAL POSITIVE-EDGE-TRIGGERED J-K FLIP-FLOPS

Feature

- Positive Edge-Triggering
- · Direct Set and reset inputs
- J and K inputs
- Q and Q outputs

Description

This device contains two independent positive-edge-triggered J- \overline{K} flip-flops with complementary outputs. The J and \overline{K} data is accepted by the flip-flop on the rising edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the J and \overline{K} inputs may be changed while the clock is high or low as long as setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Function Table

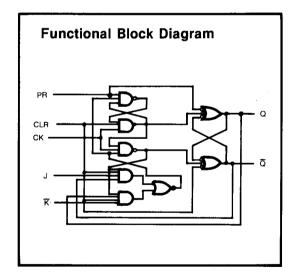
	Outputs					
PR	CLR	CLK	J	ĸ	Q	₫
L	Н	х	х	х	Н	L
Н	L	X	Х	X	L	Н
L	L	X	Х	×	Н*	H*
н	н	t	L	L	L	Н
н	н	†	Н	L	Toggle	
н	н	t	L	н	Q _o	\overline{Q}_{o}
н	н	t	н	н	н	L
н	н	. L	х	×	Q_{o}	ಠ₀

- X = Either Low or High Logic Level
- ↑ = Rising Edge of Pulse
- = This configuration is nonstable; that is, it will not persist
 when preset and/or clear inputs return to their inactive
 (high) state.

 $\mathbf{Q}_{o}=$ The output logic level of \mathbf{Q} before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each active transition of the clock pulse.

Pin Configuration ĸ2 CLK2 PR2 QŽ CLR₂ .12 Ω2 16 13 10 9 14 12 3 8 <u>0</u>1 GND Suffix-Blank: Plastic Dual In Line Package Suffix-J Ceramic Dual In Line Package



Absolute Maximum Ratings

•	Supply voltage, V _{CC}		7V
•	Input voltage	••••••	7V
		54LS	
		74LS	0°C to 70°C
•	Storage temperature range		-65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		54	4.5	5	5.5	V
-00			74	4.75	5	5.25	·
I _{OH}	High-level output current		54,74			-400	μΑ
l _{OL}	Low-level output current		54			4	mA
·OL			74			8	
f _{clock}	Clock frequency			0		25	MHz
	Clock Hig		gh	18			
$t_{\mathbf{W}}$	Pulse Width	Preset L	ow	15			ns
	Clear L		w	15			
t _{SU}	Setup Time Data High Data Low		h	30↑			ns
-50			v	201			
t _H	Hold Time		01			ns	
T _A	Operating free-air temperature		54	-55		125	°C
· M			74	0		70	_

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	TYP (Note 1)	MAX	UNIT	
V _{iH}	High-level input voltage				2			V	
V _{IL}	Low-level input voltage			54			0.7	V	
"-				74			0.8		
V _{IK}	Input clamp voltage	V _{CC} =Min, I	_I = – 18mA				-1.5	V	
V_{OH}	High level output voltage	V _{CC} =Min, V	_{IL} =Max	54	2.5	3.4		V	
	VOH Trigit level output voltage		I _{OH} =Max, V _{IH} =Min 74		2.7	3.4	·		
V	Low-level output voltage	V _{CC} =Min V _{IL} =Max	I _{OL} =4mA	54,74		0.25	0.4	V	
V _{OL}	Low-level output voltage	V _{IH} =Min	I _{OL} =8mA	74		0.35	0.5		
	Input current at maximum input voltage	V _{CC} =Max V _I =7V	J,K				0.1		
l _i			Clock				0.1	mA	
1			Preset				0.2		
	,		Clear				0.2		
			J,K				20		
l _{iH}	High-level	V _{CC} =Max V _I =2.7V	Clock				20		
""	input current		Preset				40	,	
			Clear				40		
		V _{CC} =Max V _I =0.4V	J,K				-0.4		
I _{IL}			Clock				-0.4	mA	
			Present			•	-0.8		
		Clear					-0.8		
los	Short-circuit output current	V _{CC} =Max (Note 2)			-20		-100	mA	
I _{cc}	Supply current	V _{CC} =Max (Note 3)			4	8	mA	

Note 1: All typical values are at $V_{CC}=5V$, $T_A=25\,^{\circ}C$.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where $V_{CC}=2.25V$ and 2. 125V for 54 and 74 series, respectively, with the minimum and and maximum limits reduced by one half from their stated values. This is very useful when using automastic test equipment.

Note 3: With all outputs open, I_{CC} is measured with the Q and \overline{Q} outputs high in turn. At the time of measurement the clock is grounded

Switching Characteristics, $V_{CC} = 5V$, $T_A = 25$ °C

PARAMETER*	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN TYP	MAX	UNIT
f _{max}				25 33		MHz
t _{PLH}	Clock	Q or Q		17	25	ns
t _{PHL}				22	30	ns
t _{PLH}	Clear	۵	C ₁ = 15nF	17	25	
t _{PHL}		Q	C _L =15pF, R _L =2kΩ	22	30	ns
t _{PLH}	Preset	Q		16	25	ns
t _{PHL}		ã		22	30	1 113

 $[\]begin{array}{lll} ^{\star} f_{\text{max}} &=& \text{maximum clock frequency.} \\ f_{\text{PLH}} &=& \text{propagation delay time, low-to-level output.} \\ t_{\text{PLH}} &=& \text{propagation delay time, high-to-low-level output.} \end{array}$