CY7B134
CY7B135
CY7B1342

4K x 8 Dual-Port Static RAMs and 4K x 8 Dual-Port Static RAM with Semaphores

Features

- **0.8-micron BiCMOS for high performance**
- **High-speed access**
  - **— 15 ns (commercial)**
  - **— 25 ns (military)**
- **Automatic power-down**
- **Fully asynchronous operation**
- **7B1342 includes semaphores**
- **7B134 available in 48-pin DIP**
- **7B135/7B1342 available in 52-pin LCC/PLCC**

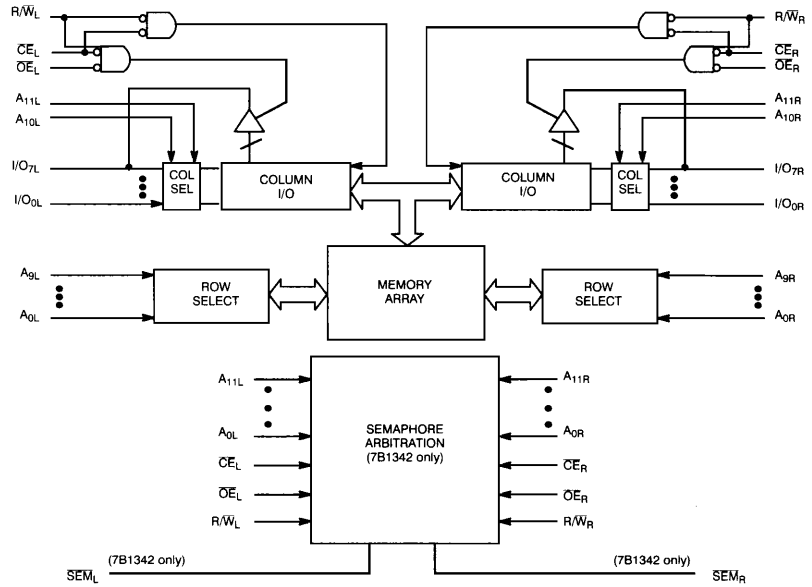
Functional Description

The CY7B134, CY7B135, and CY7B1342 are high-speed BiCMOS 4K x 8 dual-port static RAMs. The CY7B1342 includes semaphores that provide a means to allocate portions of the dual-port RAM or any shared resource. Two ports are provided permitting independent, asynchronous access for reads and writes to any location in memory. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: chip enable ($\overline{CE}$), read or write enable ($R/\overline{W}$), and output enable ($\overline{OE}$). The CY7B134/135 are suited for those systems that do not require on-chip arbitration or are intolerant of wait states. Therefore, the user must be aware that simultaneous access to a location is possible. Semaphores are offered on the CY7B1342 to assist in arbitrating between ports. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power-down feature is controlled independently on each port by a chip enable ($\overline{CE}$) pin or $\overline{SEM}$ pin (CY7B1342 only).

The CY7B134 is available in 48-pin DIP. The CY7B135 and CY7B1342 are available in 52-pin LCC/PLCC.

Logic Block Diagram

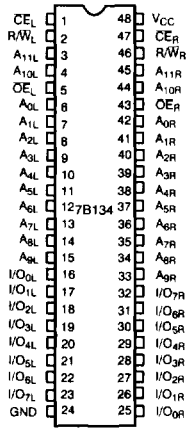


Selection Guide

		7B135–15 7B1342–15	7B134–20 7B135–20 7B1342–20	7B134–25 7B135–25 7B1342–25	7B134–35 7B135–35 7B1342–35	7B134–55 7B135–55 7B1342–55
Maximum Access Time (ns)		15	20	25	35	55
Maximum Operating Current (mA)	Commercial	260	240	220	210	210
	Military			260	250	250
Maximum Standby Current (mA)	Commercial	110	100	95	90	90
	Military			100	95	95

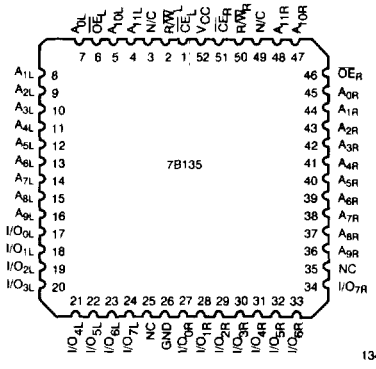
Pin Configurations

DIP
Top View



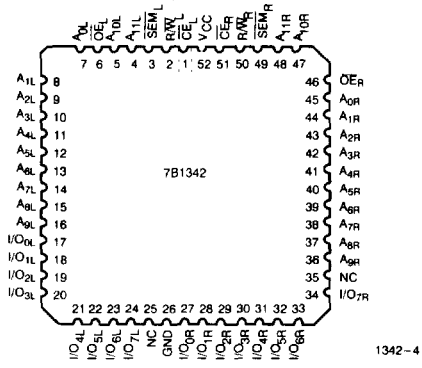
1342-2

LCC/PLCC
Top View



1342-3

LCC/PLCC
Top View



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Pin Definitions

Left Port	Right Port	Description
A_{0L-11L}	A_{0R-11R}	Address Lines
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{SEM}_L$ (CY7B1342 only)	$\overline{SEM}_R$ (CY7B1342 only)	Semaphore Enable. When asserted LOW, allows access to eight semaphores. The three least significant bits of the address lines will determine which semaphore to write or read. The I/O_0 pin is used when writing to a semaphore. Semaphores are requested by writing a 0 into the respective location.

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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 48 to Pin 24) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage[1] ..... −3.0V to +7.0V

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	−40°C to +85°C	5V ± 10%
Military[2]	−55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7B135−15 7B1342−15 Min.	7B135−15 7B1342−15 Max.	7B134−20 7B135−20 7B1342−20 Min.	7B134−20 7B135−20 7B1342−20 Max.	7B134−25 7B135−25 7B1342−25 Min.	7B134−25 7B135−25 7B1342−25 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2		2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8		0.8	V
I_{IX}	Input Load Current	$GND \le V_I \le V_{CC}$		−10	+10	−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	Outputs Disabled, $GND \le V_O \le V_{CC}$		−10	+10	−10	+10	−10	+10	µA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		260		240		220	mA
			Mil/Ind						260	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R \ge V_{IH}$, f = f_{MAX}[4]	Com'l		110		100		95	mA
			Mil/Ind						100	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ and $\overline{CE}_R \ge V_{IH}$, f = f_{MAX}[4]	Com'l		165		155		145	mA
			Mil/Ind						170	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R \ge V_{CC}$ − 0.2V, $V_{IN} \ge V_{CC}$ − 0.2V or $V_{IN} \le$ 0.2V, f = 0[4]	Com'l		15		15		15	mA
			Mil/Ind						30	
I_{SB4}	Standby Current (One Port CMOS Level)	One Port $\overline{CE}_L$ or $\overline{CE}_R \ge V_{CC}$ − 0.2V, $V_{IN} \ge V_{CC}$ − 0.2V or $V_{IN} \le$ 0.2V, Active Port Outputs, f = f_{MAX}[4]	Com'l		160		150		140	mA
			Mil/Ind						160	

Notes:

1. Pulse width < 20 ns.
2. T_A is the "instant on" case temperature.
3. See the last page of this specification for Group A subgroup testing information.
4. $f_{MAX} = 1/t_{RC}$ = All inputs cycling at f = $1/t_{RC}$ (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}.

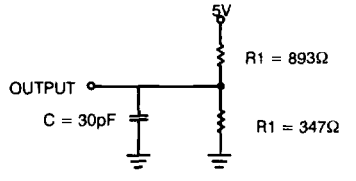
Electrical Characteristics Over the Operating Range[3](continued)

Parameter	Description	Test Conditions		7B134–35 7B135–35 7B1342–35 Min.	7B134–35 7B135–35 7B1342–35 Max.	7B134–55 7B135–55 7B1342–55 Min.	7B134–55 7B135–55 7B1342–55 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	Outputs Disabled, GND ≤ V_O ≤ V_{CC}		−10	+10	−10	+10	μA
I_{CC}	Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Com'l		210		210	mA
			Mil/Ind		250		250	
I_{SB1}	Standby Current (Both Ports TTL Levels)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[4]	Com'l		90		90	mA
			Mil/Ind		95		95	
I_{SB2}	Standby Current (One Port TTL Level)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[4]	Com'l		135		135	mA
			Mil/Ind		160		160	
I_{SB3}	Standby Current (Both Ports CMOS Levels)	Both Ports $\overline{CE}$ and $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, f = 0[4]	Com'l		15		15	mA
			Mil/Ind		30		30	
I_{SB4}	Standby Current (One Port CMOS Level)	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} − 0.2V, V_{IN} ≥ V_{CC} − 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs, f = f_{MAX}[4]	Com'l		130		130	mA
			Mil/Ind		140		140	

Capacitance[5]

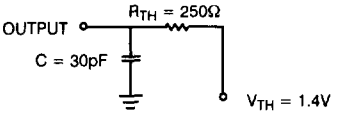
Parameter	Description	Test Conditions	Max.[6]	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms



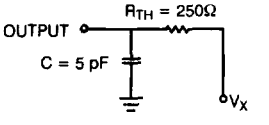
(a) Normal Load (Load 1)

1342-5



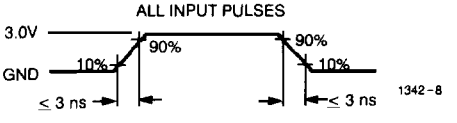
(b) Thévenin Equivalent (Load 1)

1342-6



(c) Three-State Delay (Load 3)

1342-7



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Notes:

5. Tested initially and after any design or process changes that may affect these parameters.
6. For all packages except DIP and cerDIP (D26, P25), which have maximums of C_{IN} = 15 pF, C_{OUT} = 15 pF.

Switching Characteristics Over the Operating Range[7, 8]

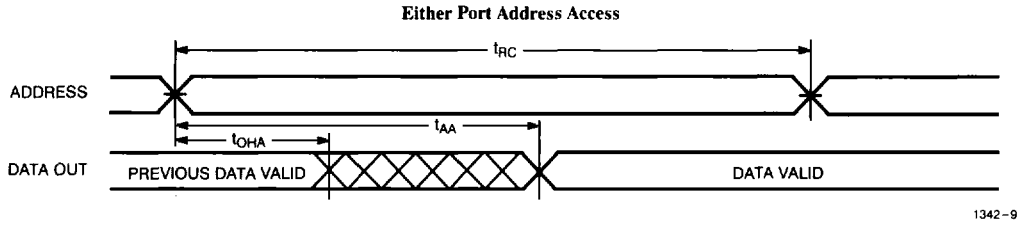
Parameter	Description	7B135–15 7B1342–15		7B134–20 7B135–20 7B1342–20		7B134–25 7B135–25 7B1342–25		7B134–35 7B135–35 7B1342–35		7B134–55 7B135–55 7B1342–55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE												
t_{RC}	Read Cycle Time	15		20		25		35		55		ns
t_{AA}	Address to Data Valid		15		20		25		35		55	ns
t_{OHA}	Output Hold From Address Change	3		3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		15		20		25		35		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		10		13		15		20		25	ns
t_{LZOE}[9, 10]	$\overline{OE}$ Low to Low Z	3		3		3		3		3		ns
t_{HZOE}[9, 10]	$\overline{OE}$ HIGH to High Z		10		13		15		20		25	ns
t_{LZCE}[9, 10]	$\overline{CE}$ LOW to Low Z	3		3		3		3		3		ns
t_{HZCE}[9, 10]	$\overline{CE}$ HIGH to High Z		10		13		15		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down		15		20		25		35		55	ns
WRITE CYCLE												
t_{WC}	Write Cycle Time	15		20		25		35		55		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		15		20		30		50		ns
t_{AW}	Address Set-Up to Write End	12		15		20		30		50		ns
t_{HA}	Address Hold from Write End	2		2		2		2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		ns
t_{PWE}	Write Pulse Width	12		15		20		25		50		ns
t_{SD}	Data Set-Up to Write End	10		13		15		15		25		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		ns
t_{HZWE}[10]	R/$\overline{W}$ LOW to High Z		10		13		15		20		25	ns
t_{LZWE}[10]	R/$\overline{W}$ HIGH to Low Z	3		3		3		3		3		ns
t_{WDD}[11]	Write Pulse to Data Delay		30		40		50		60		70	ns
t_{DDD}[11]	Write Data Valid to Read Data Valid		25		30		30		35		40	ns
SEMAPHORE TIMING[12]												
t_{SOP}	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10		10		10		15		15		ns
t_{SWRD}	SEM Flag Write to Read Time	5		5		5		5		5		ns
t_{SPS}	SEM Flag Contention Window	5		5		5		5		5		ns

Notes:

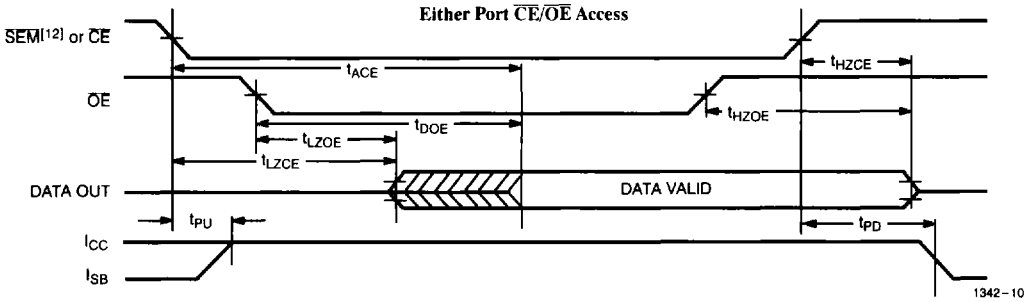
7. See the last page of this specification for Group A subgroup testing information.
8. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance
9. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
10. Test conditions used are Load 3.
11. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Read Timing with Port-to-Port Delay waveform.
12. Semaphore timing applies only to CY7B1342.

Switching Waveforms

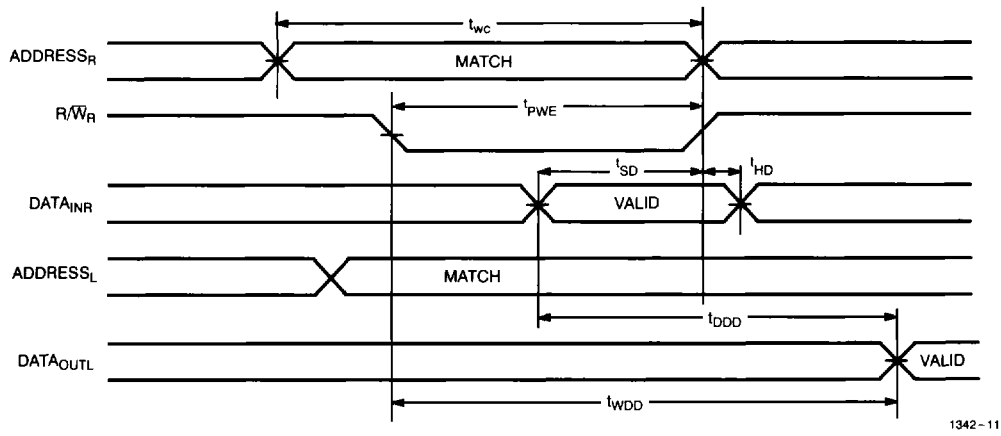
Read Cycle No. 1[13, 14]



Read Cycle No. 2[13, 15]



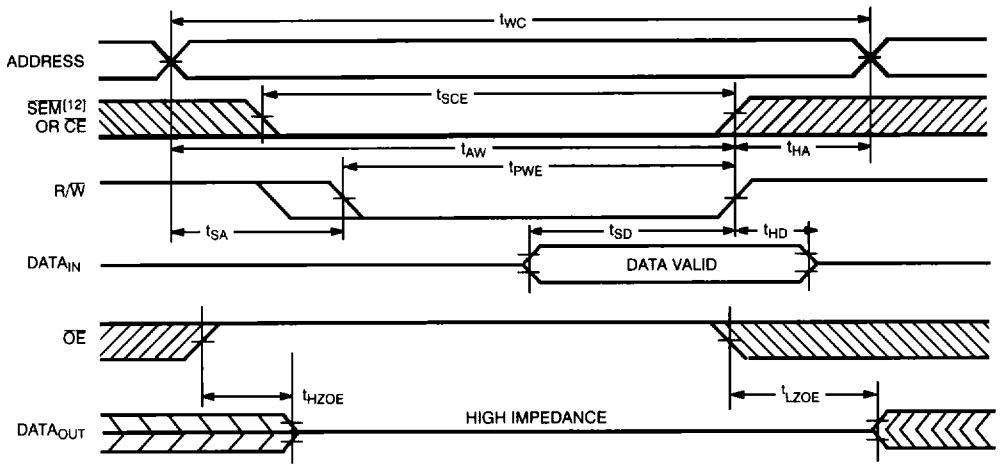
Read Timing with Port-to-Port Delay[16]



Notes:
13. R/$\overline{W}$ is HIGH for read cycle.
14. Device is continuously selected, $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IL}.
15. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
16. $\overline{CE}_L$ = $\overline{CE}_R$ =LOW; R/$\overline{W}_L$ = HIGH

Switching Waveforms (continued)

Write Cycle No. 1: $\overline{OE}$ Three-States Data I/Os (Either Port)[17, 18, 19]

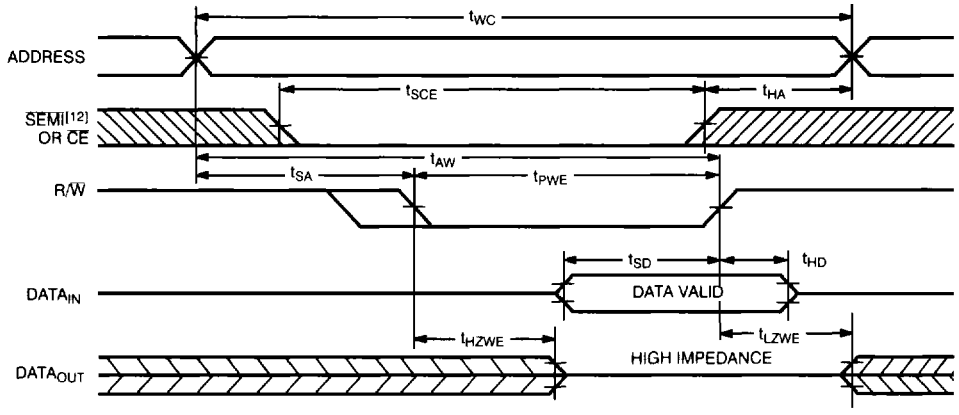


Notes:

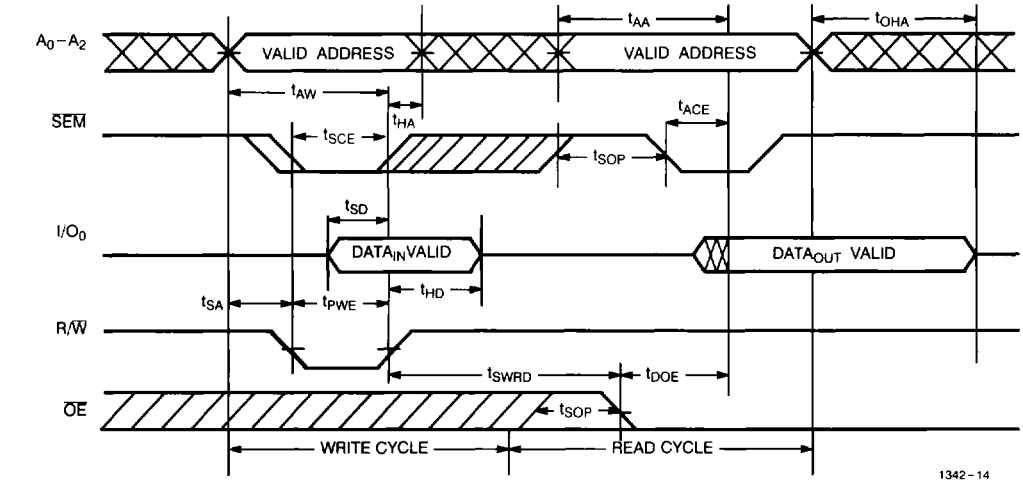
17. The internal write time of the memory is defined by the overlap of $\overline{CE}$ or $\overline{SEM}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
18. R/$\overline{W}$ must be HIGH during all address transactions.
19. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or (t_{HZWE} + t_{SD}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If $\overline{OE}$ is HIGH during a R/$\overline{W}$ controlled write cycle (as in this example), this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.

Switching Waveforms (continued)

Write Cycle No. 2: R/$\overline{W}$ Three-States Data I/Os (Either Port)[18, 20]



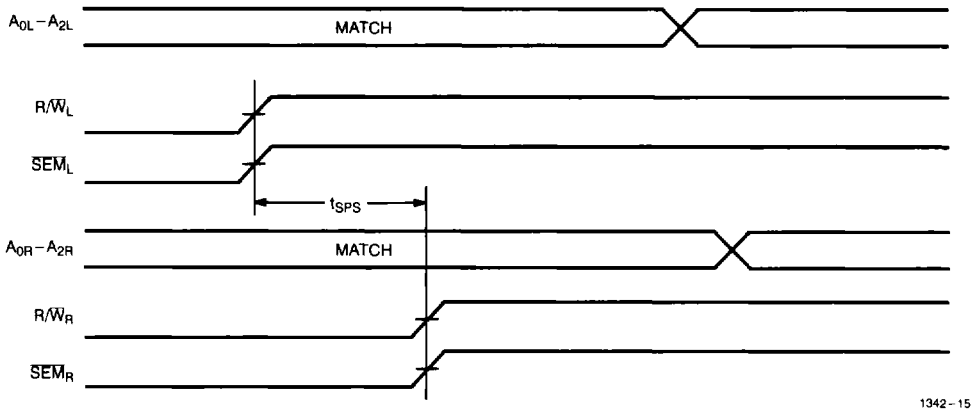
Semaphore Read After Write Timing, Either Side (CY7B1342 only)[21]



Notes:
20. Data I/O pins enter high-impedance when $\overline{OE}$ is held LOW during write.
21. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).

Switching Waveforms (continued)

Timing Diagram of Semaphore Contention (CY7B1342 only)[22, 23, 24]



Notes:
22. $I/O_{0R} = I/O_{0L}$ = LOW (request semaphore); $\overline{CE}_R = \overline{CE}_L$ = HIGH.
23. Semaphores are reset (available to both ports) at cycle start.
24. If t_{SPS} is violated, it is guaranteed that only one side will gain access to the semaphore.

Architecture

The CY7B134 and CY7B135 consist of an array of 4K words of 8 bits each of dual-port RAM cells, I/O and address lines, and control signals ($\overline{CE}$, $\overline{OE}$, R/$\overline{W}$). Two semaphore control pins exist for the CY7B1342 ($\overline{SEM}_{L/R}$).

Functional Description

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/$\overline{W}$ in order to guarantee a valid write. Since there is no on-chip arbitration, the user must be sure that a specific location will not be accessed simultaneously by both ports or erroneous data could result. A write operation is controlled by either the $\overline{OE}$ pin (see Write Cycle No. 1 timing diagram) or the R/$\overline{W}$ pin (see Write Cycle No. 2 timing diagram). Data can be written t_{HZOE} after the $\overline{OE}$ is deasserted or t_{HZWE} after the falling edge of R/$\overline{W}$. Required inputs for write operations are summarized in *Table 1*.

If a location is being written to by one port and the opposite port attempts to read the same location, a port-to-port flowthrough delay is met before the data is valid on the output. Data will be valid on the port wishing to read the location t_{DDD} after the data is presented on the writing port.

Read Operation

When reading the device, the user must assert both the $\overline{OE}$ and $\overline{CE}$ pins. Data will be available t_{ACE} after $\overline{CE}$ or t_{DOE} after $\overline{OE}$ are asserted. If the user of the CY7B1342 wishes to access a semaphore, the $\overline{SEM}$ pin must be asserted instead of the $\overline{CE}$ pin. Required inputs for read operations are summarized in *Table 1*.

Semaphore Operation

The CY7B1342 provides eight semaphore latches which are separate from the dual port memory locations. Semaphores are used to reserve resources which are shared between the two ports. The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a zero to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, $\overline{SEM}$ or $\overline{OE}$ must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value will be available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a zero), it assumes control over the shared resource, otherwise (reads a one) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a one), the left side will succeed in gaining control of the semaphore. If the left side no longer requires the semaphore, a one is written to cancel its request.

Semaphores are accessed by asserting $\overline{SEM}$ LOW. The $\overline{SEM}$ pin functions as a chip enable for the semaphore latches. $\overline{CE}$ must remain HIGH during $\overline{SEM}$ LOW. A_{0-2} represents the semaphore address. $\overline{OE}$ and R/$\overline{W}$ are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a 0 is written to the left port of an unused semaphore, a one will appear at the same semaphore address on the right port. That semaphore can now only be modified by the side showing a zero (the left port in this case). If the left port now relinquishes control by writing a one to the semaphore, the semaphore will be set to one for both sides. However, if the right port had requested the semaphore (written a zero) while the left port had control, the right port would immediately own the semaphore. *Table 2* shows sample semaphore operations.

When reading a semaphore, all eight data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports request a semaphore control by writing a 0 to a semaphore within t_{SPS} of each other, it is guaranteed that only one side will gain access to the semaphore.

Initialization of the semaphore is not automatic and must be reset during initialization program at power-up. All semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

Table 1. Non-Contending Read/Write

Inputs				Outputs	
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{SEM}$	$I/O_0 - I/O_7$	Operation
H	X	X	H	High Z	Power-Down
H	H	L	L	Data Out	Read $Data_{IN}$ Semaphore
X	X	H	X	High Z	I/O Lines Disabled
H	⎍	X	L	Data In	Write to Semaphore
L	H	L	H	Data Out	Read
L	L	X	H	Data In	Write
L	X	X	L		Illegal Condition

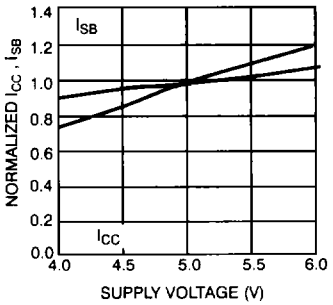
Table 2. Semaphore Operation Example

Function	I/O_0 Left	I/O_0 Right	Status
No Action	1	1	Semaphore free
Left port writes semaphore	0	1	Left port obtains semaphore
Right port writes 0 to semaphore	0	1	Right side is denied access
Left port writes 1 to semaphore	1	0	Right port is granted access to Semaphore
Left port writes 0 to semaphore	1	0	No change. Left port is denied access
Right port writes 1 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore address
Right port writes 0 to semaphore	1	0	Right port obtains semaphore
Right port writes 1 to semaphore	1	1	No port accessing semaphore
Left port writes 0 to semaphore	0	1	Left port obtains semaphore
Left port writes 1 to semaphore	1	1	No port accessing semaphore

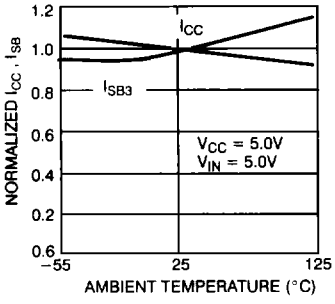
6

Typical DC and AC Characteristics

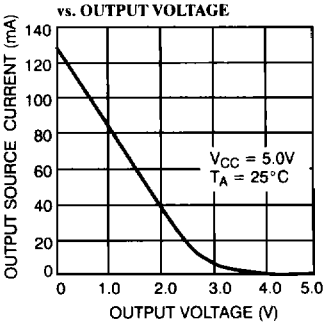
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



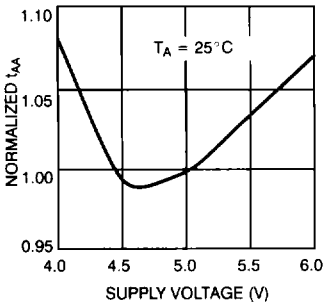
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



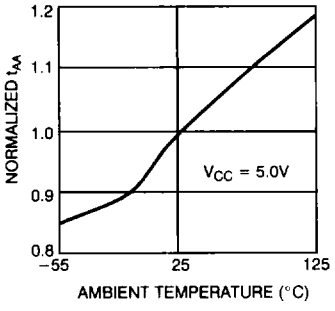
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



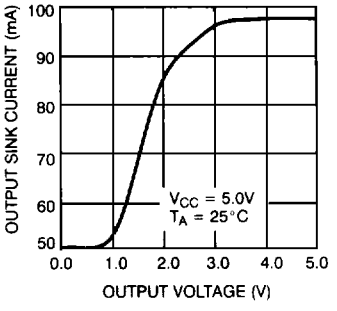
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



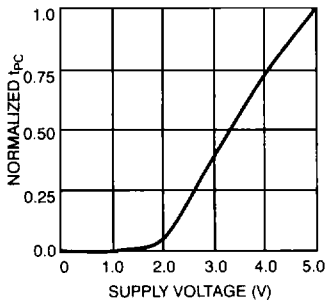
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



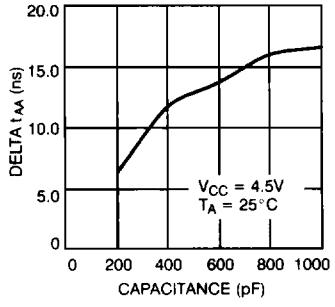
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



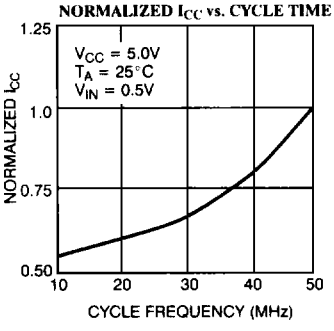
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
20	CY7B134-20PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
25	CY7B134-25PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7B134-25PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7B134-25DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
35	CY7B134-35PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7B134-35PI	P25	48-Lead (600-Mil) Molded DIP	Industrial
	CY7B134-35DMB	D26	48-Lead (600-Mil) Sidebraze DIP	Military
55	CY7B134-55PC	P25	48-Lead (600-Mil) Molded DIP	Commercial
	CY7B134-55PI	P25	48-Lead (600-Mil) Molded DIP	Industrial

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7B135-15JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
20	CY7B135-20JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
25	CY7B135-25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B135-25JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B135-25LMB	L69	52-Square Leadless Chip Carrier	Military
35	CY7B135-35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B135-35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B135-35LMB	L69	52-Square Leadless Chip Carrier	Military
55	CY7B135-55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B135-55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial

Speed (ns)	Ordering Code	Package Type	Package Type	Operating Range
15	CY7B1342-15JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
20	CY7B1342-20JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
25	CY7B1342-25JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B1342-25JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B1342-25LMB	L69	52-Square Leadless Chip Carrier	Military
35	CY7B1342-35JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B1342-35JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial
	CY7B1342-35LMB	L69	52-Square Leadless Chip Carrier	Military
55	CY7B1342-55JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B1342-55JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3
I_{SB3}	1, 2, 3
I_{SB4}	1, 2, 3

Switching Characteristics

Parameter	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
t_{DOE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
SEMAPHORE CYCLE	
t_{SOD}	7, 8, 9, 10, 11
t_{SWRD}	7, 8, 9, 10, 11
t_{SPS}	7, 8, 9, 10, 11

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