











SN74LVCR16245A

SCES427B - FEBRUARY 2003 - REVISED JUNE 2014

SN74LVCR16245A 16-Bit Bus Transceiver with 3-State Outputs

Features

- Member of the Texas Instruments Widebus™ Family
- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 4.8 ns at 3.3 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V V_{CC})
- All Inputs and Outputs Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required
- I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

2 Applications

- Servers
- PCs and Notebooks
- **Network Switches**
- Telecom Infrastructures

3 Description

This 16-bit (dual-octal) noninverting bus transceiver is designed for 1.65-V to 3.6-V V_{CC} operation.

The SN74LVCR16245A device is designed for asynchronous communication between data buses. All inputs and outputs have equivalent $26-\Omega$ resistors that will slow the edges of the output and reduce switching noise caused by long capacitive etch runs or cables.

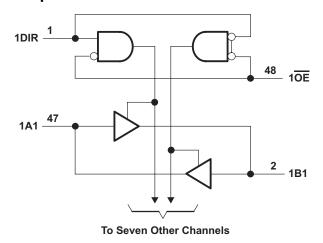
This device can be used as two 8-bit transceivers or one 16-bit transceiver. Active bus-hold circuitry holds unused or undriven data inputs at a valid logic state.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
	TSSOP (48)	12.50 mm × 6.1 mm
	TVSOP (48)	9.70 mm × 4.40 mm
SN74LVCR16245A	SSOP (48)	15.88 mm × 7.49 mm
	BGA MICROSTAR JUNIOR (56)	7.00 mm × 4.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



Pin numbers shown are for the DGG, DGV, and DL packages.

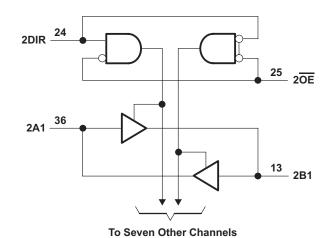




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5 Revision History

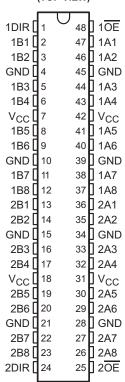
Cł	hanges from Revision A (November 2004) to Revision B	Page
•	Updated document to new TI data sheet standards.	
•	Deleted Ordering Information table.	
•	Updated I _{off} Feature bullet.	
•	Added Applications.	
	Added Handling Ratings table	
•	Changed MAX ambient temperature to 125°C.	
•	Added Thermal Information table.	
•	Added Typical Characteristics.	

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6 Pin Configuration and Functions

DGG, DGV, OR DL PACKAGE (TOP VIEW)



Pin Functions

	PIN	1/0	DECORPORA
NO.	NAME	1/0	DESCRIPTION
1	1DIR	I	Direction pin 1
2	1B1	I/O	1B1 input or output
3	1B2	I/O	1B2 input or output
4	GND	_	Ground pin
5	1B3	I/O	1B3 input or output
6	1B4	I/O	1B4 input or output
7	VCC	_	Power pin
8	1B5	I/O	1B5 input or output
9	1B6	I/O	1B6 input or output
10	GND	_	Ground pin
11	1B7	I/O	1B7 input or output
12	1B8	I/O	1B8 input or output
13	2B1	I/O	2B1 input or output
14	2B2	I/O	2B2 input or output
15	GND	_	Ground pin
16	2B3	I/O	2B3 input or output
17	2B4	I/O	2B4 input or output
18	VCC	_	Power pin
19	2B5	I/O	2B5 input or output
20	2B6	I/O	2B6 input or output
21	GND	_	Ground pin

Product Folder Links: SN74LVCR16245A



Pin Functions (continued)

	PIN	1/0	PEGGRIPTION
NO.	NAME	WO WO	DESCRIPTION
22	2B7	I/O	2B7 input or output
23	2B8	I/O	2B8 input or output
24	2DIR	1	Direction pin 2
25	2 OE	1	Output Enable 2
26	2A8	I/O	2A8 input or output
27	2A7	I/O	2A7 input or output
28	GND	_	Ground pin
29	2A6	I/O	2A6 input or output
30	2A5	I/O	2A5 input or output
31	VCC	_	Power pin
32	2A4	I/O	2A4 input or output
33	2A3	I/O	2A3 input or output
34	GND	_	Ground pin
35	2A2	I/O	2A2 input or output
36	2A1	I/O	2A1 input or output
37	1A8	I/O	1A8 input or output
38	1A7	I/O	1A7 input or output
39	GND	_	Ground pin
40	1A6	I/O	1A6 input or output
41	1A5	I/O	1A5 input or output
42	VCC	_	Power pin
43	1A4	I/O	1A4 input or output
44	1A3	I/O	1A3 input or output
45	GND	_	Ground pin
46	1A2	I/O	1A2 input or output
47	1A1	I/O	1A1 input or output
48	1 OE	1	Output Enable 1

GQL OR ZQL PACKAGE (TOP VIEW)

1 2 3 4 5 6 000000 000000 В 000000 С 000000 D \bigcirc \bigcirc Ε F \bigcirc \bigcirc 000000 G 000000 Н 000000 J 000000

Pin Assignments

	1	2	3	4	5	6
Α	1DIR	NC	NC	NC	NC	10E
В	1B2	1B1	GND	GND	1A1	1A2
С	1B4	1B3	Vcc	Vcc	1A3	1A4
D	1B6	1B5	GND	GND	1A5	1A6
E	1B8	1B7			1A7	1A8
F	2B1	2B2			2A2	2A1
G	2B3	2B4	GND	GND	2A4	2A3
Н	2B5	2B6	V _{CC}	V _{CC}	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2DIR	NC	NC	NC	NC	2OE

NC - No internal connection

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
V_{I}	Input voltage range (2)	nput voltage range ⁽²⁾			
Vo	Voltage range applied to any output in the h	-0.5	6.5	V	
Vo	Voltage range applied to any output in the h	-0.5	V _{CC} + 0.5	V	
I _{IK}	Input clamp current	V _I < 0		-50	mA
I _{OK}	Output clamp current	V _O < 0		-50	mA
IO	Continuous output current			±50	mA
	Continuous current through each V _{CC} or GN	D		±100	mA

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Handling Ratings

			MIN	MAX	UNIT
T _{stg}	Storage temperature rang	torage temperature range			
	Electrostatic discharge pins	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	0	2000	\/
V _(ESD)		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	0	1500	V

JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

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The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed. The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
17	Complexed to me	Operating	1.65	3.6	V
vcc	High-level input voltage Low-level input voltage Input voltage Output voltage High-level output current Low-level output current	Data retention only	1.5		V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		
V_{IH}	High-level input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
V _{IH} High-leve V _{IL} Low-level V _I Input volta V _O Output volta I _{OH} High-leve		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2		
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$		0.35 × V _{CC}	
V_{IL}	Low-level input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
V _{IL}		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$		0.8	
V _I	Input voltage		0	5.5	V
\/	Outrot valtage	High or low state	0	V _{CC}	V
۷O	Output voltage	3-state	0	5.5	V
		V _{CC} = 1.65 V		-2	
	V _{IL} Low-level input voltage V _I Input voltage V _O Output voltage OH High-level output current	V _{CC} = 2.3 V		-4	A
ЮН		V _{CC} = 2.7 V		-8	mA
		V _{CC} = 3 V		1.65 3.6 1.5 5 × V _{CC} 1.7 2 0.35 × V _{CC} 0.7 0.8 0 5.5 0 V _{CC} 0 5.5 -2 -4 -8 -12 2 4	
		V _{CC} = 1.65 V		2	
	Low lovel output ourrent	V _{CC} = 2.3 V		4	A
OL	Low-level output current	V _{CC} = 2.7 V	V _{CC} = 2.7 V		mA
		V _{CC} = 3 V		12	
Δt/Δν	Input transition rise or fall rate			10	ns/V
T _A	Operating free-air temperature		-40	125	°C

⁽¹⁾ All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

7.4 Thermal Information

	THERMAL METRIC ⁽¹⁾	DGG	DGV	DL	LINUT
	THERMAL METRIC**	48 PINS	48 PINS	48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	64.3	78.4	68.4	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.6	30.7	34.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	31.5	41.8	41.0	9 0 AA
ΨЈТ	Junction-to-top characterization parameter	1.1	3.8	12.3	°C/W
ΨЈВ	Junction-to-board characterization parameter	31.2	41.3	40.4	
R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

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7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

F	PARAMETER	TEST CONDITION	ONS	V _{cc}	MIN	TYP ⁽¹⁾	MAX	UNIT	
		I _{OH} = -100 μA		1.65 V to 3.6 V	V _{CC} - 0.2				
$V_{OH} \begin{tabular}{ll} $I_{OH} = -100 \ \mu A \\ $I_{OH} = -2 \ mA \\ $I_{OH} = -2 \ mA \\ $I_{OH} = -4 \ mA \\ \begin{tabular}{ll} $I_{OH} = -4 \ mA \\ \begin{tabular}{ll} $I_{OH} = -4 \ mA \\ \begin{tabular}{ll} $I_{OH} = -6 \ mA \\ \begin{tabular}{ll} $I_{OH} = -6 \ mA \\ \begin{tabular}{ll} $I_{OH} = -8 \ mA \\ \begin{tabular}{ll} $I_{OH} = -12 \ mA \\ tabul$	$I_{OH} = -2 \text{ mA}$	$I_{OH} = -2 \text{ mA}$							
	Ι 4 Δ	2.3 V	1.7						
			V						
		$I_{OH} = -6 \text{ mA}$		3 V	2.4				
	$I_{OH} = -8 \text{ mA}$	2.7 V	2						
		I _{OH} = -12 mA		3 V	2			V	
		I _{OL} = 100 μA		1.65 V to 3.6 V			0.2		
		I _{OL} = 2 mA	1.65 V			0.45			
		2.3 V			0.7	V			
	I _{OL} = 4 mA	2.7 V			0.4				
	I _{OL} = 6 mA	3 V			0.55				
	I _{OL} = 8 mA	2.7 V			0.6				
	I _{OL} = 12 mA		3 V			0.8			
I _I	Control inputs	V _I = 0 to 5.5 V		3.6 V			±5	μΑ	
I _{off}	·	V _I or V _O = 5.5 V		0			±10	μΑ	
$I_{OZ}^{(2)}$		V _O = 0 to 5.5 V		3.6 V			±5	μΑ	
		$V_I = V_{CC}$ or GND,					20	^	
ICC		$3.6 \text{ V} \le \text{V}_{\text{I}} \le 5.5 \text{ V}^{(3)}$	I _O = 0	3.6 V			20	Αμ μΑ	
Δl _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND		2.7 V to 3.6 V			500	μΑ	
C _i	Control inputs	$V_I = V_{CC}$ or GND		3.3 V		3		pF	
C _{io}	A or B ports	$V_O = V_{CC}$ or GND		3.3 V		12		pF	

7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted) (See Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1 ± 0.15	.8 V V	V _{CC} = ± 0.		V _{CC} = 2	2.7 V	V _{CC} = ± 0.3	3.3 V 3 V	UNIT	
		(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _p	od	A or B	B or A	1	7.8	1	5.8	1.5	5.7	1.5	4.8	ns
t _e	en	ŌE	A or B	1.5	10	1	8	1.5	7.9	1.5	6.3	ns
to	lis	ŌE	A or B	1.5	11.9	1	8.4	1.5	8.3	2.2	7.4	ns

7.7 Operating Characteristics

 $T_A = 25^{\circ}C$

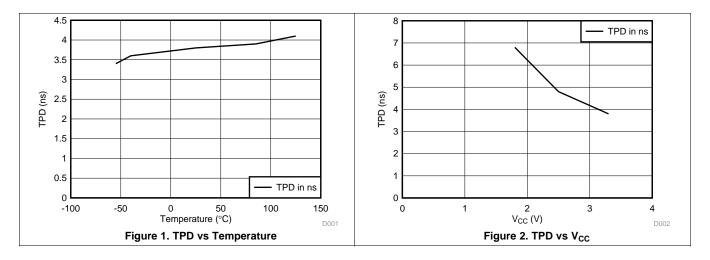
PARAMETER			TEST CONDITIONS	V _{CC} = 1.8 V TYP	V _{CC} = 2.7 V TYP	V _{CC} = 3.3 V TYP	UNIT	
C_{pd}	Power dissipation capacitance	Outputs enabled	f = 10 MHz	35	38	43	pF	
-ρu	per transceiver	Outputs disabled					ρ.	

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⁽¹⁾ All typical values are at $V_{CC} = 3.3 \text{ V}$, $T_A = 25^{\circ}\text{C}$. (2) For I/O ports, the parameter I_{OZ} includes the input leakage current. (3) This applies in the disabled state only.

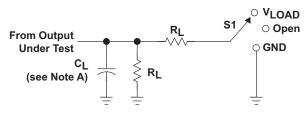


7.8 Typical Characteristics





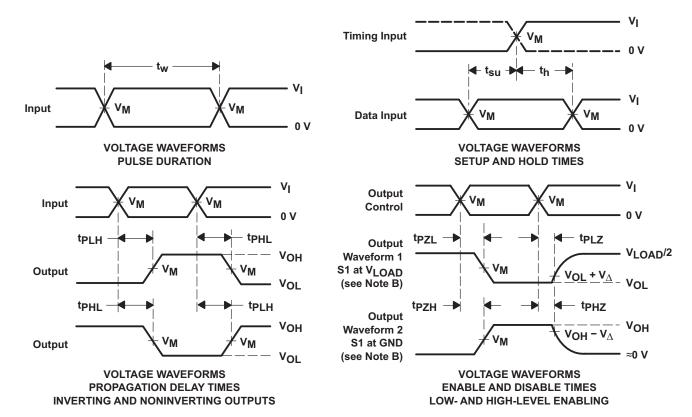
8 Parameter Measurement Information



TEST	S1
tPLH/tPHL	Open
tpLZ/tpZL	VLOAD
tPHZ/tPZH	GND

LOAD CIRCUIT

Vas	IN	PUT	V	V	C.	D.	V
Vcc	٧ _I	t _r /t _f	VM	V _{LOAD}	CL	R_{L}	$v_{\scriptscriptstyle\Delta}$
1.8 V ± 0.15 V	Vcc	≤2 ns	V _{CC} /2	VCC	30 pF	1 k Ω	0.15 V
2.5 V ± 0.2 V	VCC	≤2 ns	V _{CC} /2	Vcc	30 pF	500 Ω	0.15 V
2.7 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	2.7 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. tpLz and tpHz are the same as tdis.
- F. tpzL and tpzH are the same as ten.
- G. tpLH and tpHL are the same as tpd.
- H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

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9 Detailed Description

9.1 Overview

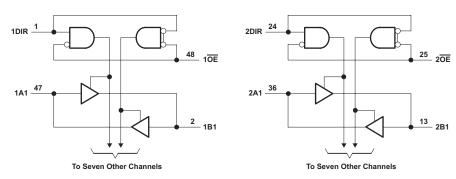
The SN74LVCR16245A device is designed for asynchronous communication between data buses. The logic levels of the direction-control (DIR) input and the output-enable (\overline{OE}) input activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports always is active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CC7} .

All inputs and outputs have equivalent $26-\Omega$ resistors that will slow the edges of the output and reduce switching noise caused by long capacitive etch runs or cables.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V_{CC} through a pullup resistor. The minimum value of the resistor is determined by the current-sinking capability of the driver. Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

9.2 Functional Block Diagram



Pin numbers shown are for the DGG, DGV, and DL packages.

Figure 4. Logic Diagram (Positive Logic)

9.3 Feature Description

- Wide operating voltage range
 - Operates from 1.65 V to 3.6 V
- Allows down voltage translation
 - Inputs accept voltages to 5.5 V
- I_{off} feature
 - Allows voltages on the inputs and outputs when V_{CC} is 0 V

9.4 Device Functional Modes

Table 1. Function Table (Each 8-Bit Section)

•		•
INF	PUTS	OPERATION
OE	DIR	OPERATION
L	L	B data to A bus
L	Н	A data to B bus
Н	Х	Isolation

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10 Application and Implementation

10.1 Application Information

The SN74LVCR16245A device is a 16-bit bidirectional transceiver. This device can be used as two 8-bit transceivers or one 16-bit transceiver. It allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so that the buses are effectively isolated. The device has 5.5V tolerant inputs at any valid V_{CC} which allows it to be used in multi-power systems and can be used for down translation.

10.2 Typical Application

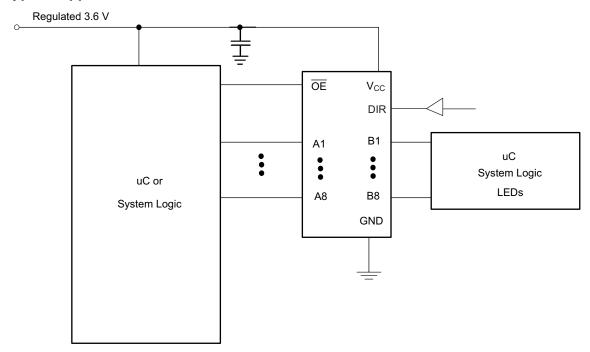


Figure 5. Typical Application Diagram

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads; therefore, routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

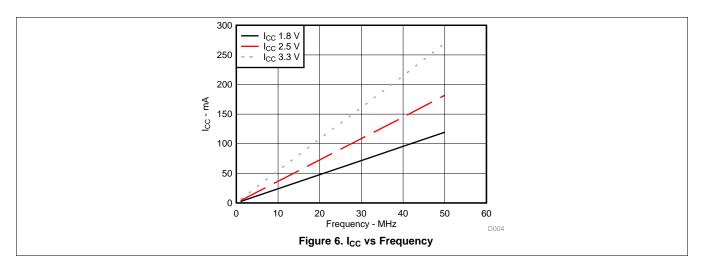
- Recommended Input Conditions
 - Rise time and fall time specs: See (Δt/ΔV) in Recommended Operating Conditions
 - Specified high and low levels: See (V_{IH} and V_{IL}) in Recommended Operating Conditions
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}
- 2. Recommend Output Conditions
 - Load currents should not exceed 25 mA per output and 50 mA total for the part
 - Outputs should not be pulled above V_{CC}

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TEXAS INSTRUMENTS

Typical Application (continued)

10.2.3 Application Curves



11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions* table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μ f is recommended; if there are multiple V_{CC} pins, then 0.01 μ f or 0.022 μ f is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μ f and a 1 μ f are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

12 Layout

12.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Figure 7 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

12.2 Layout Example

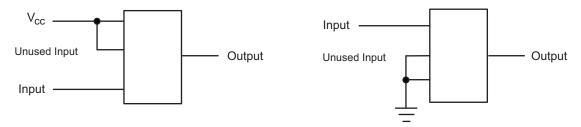


Figure 7. Layout Diagram

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13 Device and Documentation Support

13.1 Trademarks

Widebus is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGE OPTION ADDENDUM

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PACKAGING INFORMATION

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Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish (6)	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
74LVCR16245ADGGRG4	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCR16245A	Samples
SN74LVCR16245ADGGR	ACTIVE	TSSOP	DGG	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCR16245A	Samples
SN74LVCR16245ADGVR	ACTIVE	TVSOP	DGV	48	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LDR245A	Samples
SN74LVCR16245ADL	ACTIVE	SSOP	DL	48	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCR16245A	Samples
SN74LVCR16245ADLR	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCR16245A	Samples
SN74LVCR16245AZQLR	ACTIVE	BGA MICROSTAR JUNIOR	ZQL	56	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	LDR245A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.



PACKAGE OPTION ADDENDUM

10-Jun-2014

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

www.ti.com 6-May-2014

TAPE AND REEL INFORMATION





	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVCR16245ADGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	15.8	1.8	12.0	24.0	Q1
SN74LVCR16245ADGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74LVCR16245ADLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
SN74LVCR16245AZQLR	BGA MI CROSTA R JUNI OR	ZQL	56	1000	330.0	16.4	4.8	7.3	1.5	8.0	16.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVCR16245ADGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74LVCR16245ADGVR	TVSOP	DGV	48	2000	367.0	367.0	38.0
SN74LVCR16245ADLR	SSOP	DL	48	1000	367.0	367.0	55.0
SN74LVCR16245AZQLR	BGA MICROSTAR JUNIOR	ZQL	56	1000	336.6	336.6	28.6

ZQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MO-285 variation BA-2.
- D. This package is Pb-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

MicroStar Junior is a trademark of Texas Instruments



DGV (R-PDSO-G**)

24 PINS SHOWN

PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

D. Falls within JEDEC: 24/48 Pins – MO-153 14/16/20/56 Pins – MO-194

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.



DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold protrusion not to exceed 0,15.

D. Falls within JEDEC MO-153

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