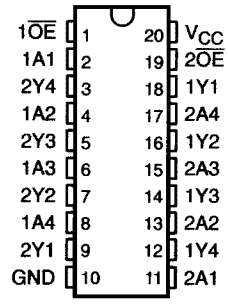
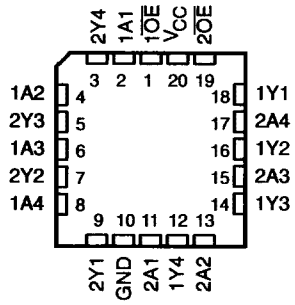
- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Package Options Include Plastic Small-Outline (SOIC), Shrink Small-Outline (SSOP), and Thin Shrink Small-Outline (TSSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs**

SN54LVT240 . . . J PACKAGE
SN74LVT240 . . . DB, DW, OR PW PACKAGE
(TOP VIEW)



SN54LVT240 . . . FK PACKAGE
(TOP VIEW)



description

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The 'LVT240 is organized as two 4-bit buffer/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

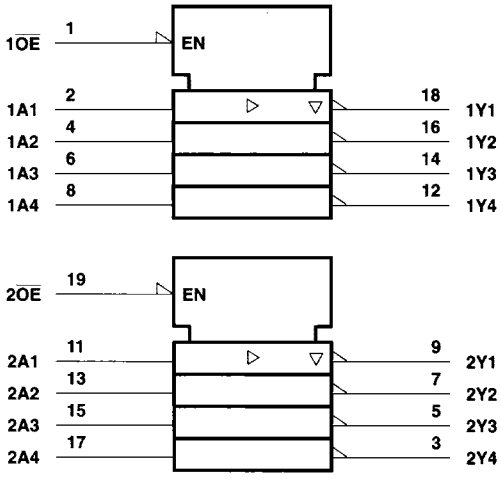
The SN74LVT240 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT240 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT240 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each buffer)

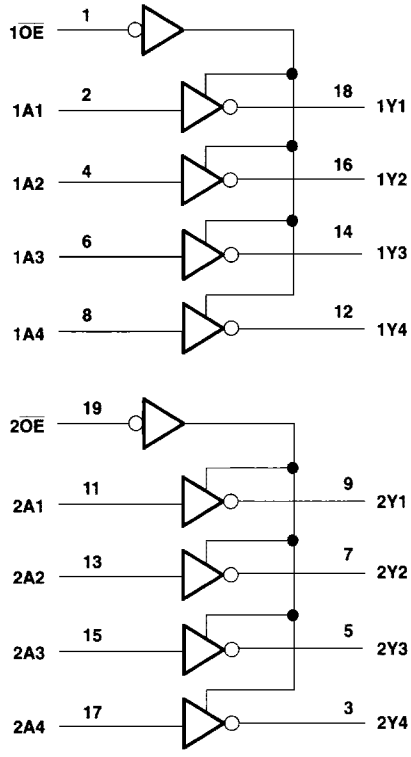
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} ..... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) ..... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT240 ..... 96 mA
SN74LVT240 ..... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT240 ..... 48 mA
SN74LVT240 ..... 64 mA
Input clamp current, I_{IK} ($V_I < 0$) ..... −50 mA
Output clamp current, I_{OK} ($V_O < 0$) ..... −50 mA
Maximum power dissipation at $T_A = 55°C$ (in still air): DB package ..... 0.65 W
DW package ..... 0.85 W
PW package ..... 0.6 W
Storage temperature range ..... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This current will only flow when the output is in the high state and $V_O > V_{CC}$.

recommended operating conditions

			SN54LVT240		SN74LVT240		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			24		32	mA
I_{OL}†	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

† Current duty cycle ≤ 50%, f ≥ 1 kHz

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

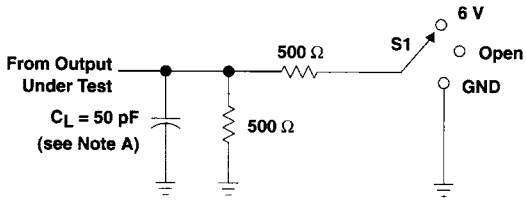
PARAMETER	TEST CONDITIONS			SN54LVT240			SN74LVT240			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 2.7 V,	I_I = –18 mA				–1.2			–1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = –100 µA		V_{CC}–0.2			V_{CC}–0.2			V
	V_{CC} = 2.7 V,	I_{OH} = – 8 mA		2.4			2.4			
	V_{CC} = 3 V,	I_{OH} = – 24 mA		2						
	V_{CC} = 3 V,	I_{OH} = –32 mA					2			
V_{OL}	V_{CC} = 2.7 V,	I_{OL} = 100 µA				0.2			0.2	V
	V_{CC} = 2.7 V,	I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 16 mA				0.4			0.4	
	V_{CC} = 3 V,	I_{OL} = 32 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 48 mA				0.55				
	V_{CC} = 3 V,	I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	µA
	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins			±1			±1	
	V_{CC} = 3.6 V,	V_I = V_{CC}	Data pins			1			1	
	V_{CC} = 3.6 V,	V_I = 0	Data pins			–5			–5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A inputs	75			75			µA
		V_I = 2 V	A inputs	–75			–75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				5			5	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				–5			–5	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.12	0.19		0.12	0.19	mA
			Outputs low		8.6	12		8.6	12	
			Outputs disabled		0.12	0.19		0.12	0.19	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, Other inputs at V_{CC} or GND	One input at V_{CC} – 0.6 V,				0.2			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_o	V_O = 3 V or 0				8			8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 1)

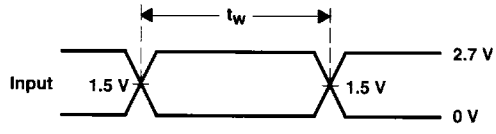
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT240			SN74LVT240				UNIT
			V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 2.7 V	V_{CC} = 3.3 V ± 0.3 V			V_{CC} = 2.7 V	
			MIN	MAX	MAX	MIN	TYP†	MAX	MAX	
t_{PLH}	A	Y	1	4.5	5.4	1	2.5	4.3	5.2	ns
t_{PHL}			1	4.5	5.2	1	2.5	4.3	5	
t_{PZH}	$\overline{OE}$	Y	1	5.4	6.5	1	2.7	5.2	6.3	ns
t_{PZL}			1	5.4	7.4	1	3.1	5.2	6.7	
t_{PHZ}	$\overline{OE}$	Y	2	5.6	6.5	2	3.9	5.6	6.3	ns
t_{PLZ}			1.6	5.3	5.8	1.6	3.2	5.1	5.6	

PARAMETER MEASUREMENT INFORMATION

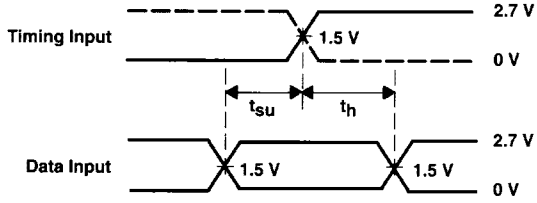


LOAD CIRCUIT FOR OUTPUTS

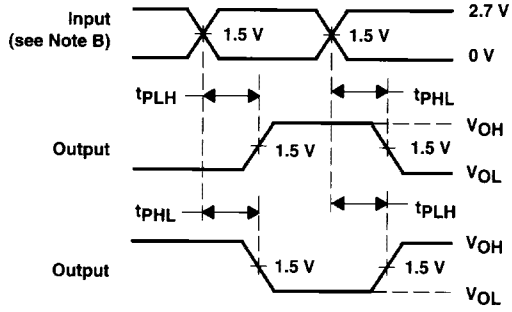
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



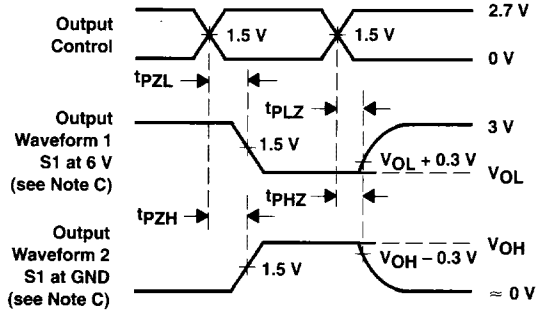
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms