47F010

1024K Bit Flash EPROM

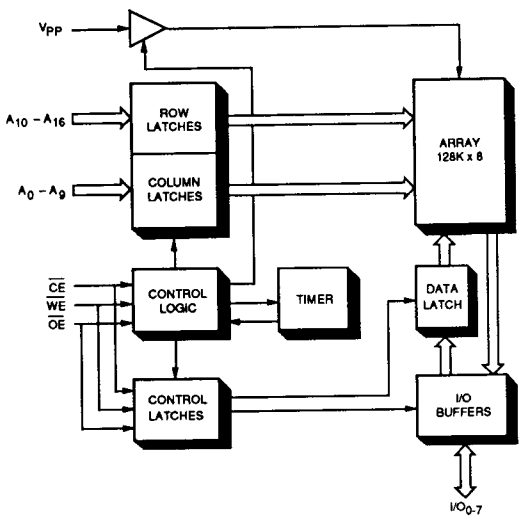
PRELIMINARY DATA SHEET

October 1989

Features

- ***128K Byte Flash Erasable Non-Volatile Memory***
- ***Input Latches for Writing and Erasing***
- ***Low Power CMOS Process***
- ***Flash EPROM Cell Technology***
- ***Fast Byte Write: 225 µs max***
- ***Ideal for Low-Cost Program Storage Applications***
  - *In-Circuit Alterable*
  - *100 Program/Erase Cycles*
  - *Minimum 10 Year Data Retention*
- ***Pinouts Upward Compatible Thru 2 Megabit Densities***
- ***JEDEC Standard Byte Wide Pinout***
  - *32 Pin PLCC*
  - *32 Pin Dip*
- ***Silicon Signature®***

Block Diagram

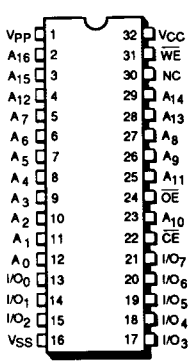


Pin Names

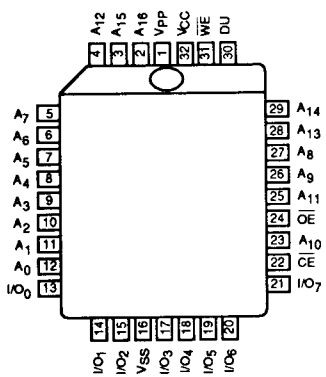
A_0-A_9	COLUMN ADDRESS INPUT
A_{10}-A_{16}	ROW ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O_{0-7}	DATA INPUT (WRITE)/OUTPUT (READ)
N.C.	NO INTERNAL CONNECTION
V_{PP}	WRITE/ERASE INPUT VOLTAGE
D.U.	DON'T USE

Pin Configuration

DUAL-IN-LINE
TOP VIEW



TOP VIEW
PLASTIC LEADED CHIP CARRIER



Silicon Signature is a registered trademark of SEEQ Technology.

Description

The 47F010 is a 1024K bit CMOS Flash EPROM organized as 128K x 8 bits. The 47F010 brings together the high density and cost effectiveness of UVEPROMs with the in-circuit reprogrammability and package options of full featured EEPROMs. SEEQ's patented split gate Flash EPROM cell design reduces both the time and cost required to alter code in program and data storage applications.

The 47F010's fast electrical erase and 0.2 ms/byte programming is 20 times faster than reprogramming of UVEPROMs. Electrical erase and reprogramming make the 47F010 ideal for applications with high density requirements, but where ultraviolet erasure is either impractical or impossible.

On chip latches and timers permit simplified microprocessor interface, freeing the microprocessor to perform other tasks once write/erase cycles have been initiated. Endurance, the number of times each byte can be written and erased, is specified at 100 cycles. Electrical erase allows the 47F010 to be packaged in a wide range of windowless plastic, ceramic and surface mount packages.

Read

Reading is accomplished by presenting a valid address on A_0 - A_{16} with chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) at V_{IL} and write enable ($\overline{WE}$) at V_{IH}. The V_{PP} pin can be at any TTL level or V_P during read operations. See page 5 for additional information on A.C. parameters and read timing waveforms.

Erase and Write

Erasing and writing of the 47F010 can only be accomplished when $V_{PP} = V_P$. Latches on address, data and control inputs, permit erasing and writing using normal microprocessor bus timing. Address inputs are latched on the falling edge of write enable or chip enable, whichever is later. While data inputs are latched on the rising edge of write enable or chip enable, whichever is earlier. The write enable input is noise protected; a pulse of less than 20 ns will not initiate a write or erase. In addition, chip enable, output enable and write enable pins must be in the proper state to initiate a write or erase. Timing diagrams depict write enable controlled writes; the timing also applies to chip enable controlled writes.

Byte Write

A byte write is used to change any 1 in a byte to a 0. Individual bytes, multiple bytes or the entire memory can be written at one time. If a bit in a byte needs to be changed from a 0 to a 1, the 47F010 must first be erased via chip erase and then reprogrammed with the desired data. Any byte write operation requires that the V_{PP} pin be at high voltage (V_P).

The 47F010 uses a software controlled looping algorithm (figure 1) to perform writes and verify successful byte programming. During a byte write operation, all non "FF"[1] bytes are incrementally written using a 75 µs minimum t_{WC}. Each byte write is automatically latched and timed on-chip, so that the microprocessor can perform other tasks once the write cycle has been initiated. Write cycle time duration can be controlled by the microprocessor, or the on-chip timer will automatically terminate t_{WC} after 150 µs. One write loop has been completed when all non "FF" data for all desired bytes have been written. After 3 programming loops, a read-verification cycle is performed. For any bytes which do not verify, a fill-in programming loop is performed.

Chip Erase

Chip Erase will change all bits in the memory to a logical 1. The 47F010 uses a two-step, software controlled looping algorithm to perform the chip erase operation. Each loop requires that a chip erase select be performed prior to the start of each chip erase cycle.

The chip erase select is activated by initiating a write cycle with the V_{PP} pin at V_{IH} or lower. During the chip erase select, address and data lines can be at any TTL level. Following a chip erase select, the 47F010 will start chip erase if all data inputs are "FF", $V_{PP} = V_P$ and a write cycle initiated. After 20 loops, a device erase verify is performed to insure all bytes = "FF". After erase, the V_{PP} pin can be brought to any TTL level or left at high voltage.

Refer to page 8 for chip erase timing diagram and figure 2 for the erase algorithm.

Power Up/Down Protection

This device contains a sense circuit which disables internal erase and write operations when V_{CC} is below 3.5 volts. In addition, erases and writes are prevented when any control input ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) is in the wrong state for writing /erasing (see mode table).

High Voltage Input Protection

The V_{PP} pin is at a high voltage for writing and erasing. There is an absolute maximum specification for the V_{PP}

[1] Only non "FF" bytes can be written.

pin which must not be exceeded, even briefly, or permanent device damage may result. To minimize switching transients on this pin, we recommend using a minimum 0.1 µf decoupling capacitor with good high frequency response connected from V_{PP} to ground at each device. In addition, sufficient bulk capacitance should be provided to minimize V_{PP} voltage sag when a device goes from standby to a write or erase cycle.

Silicon Signature

A row of fixed ROM is present in the 47F010 which contains the device's Silicon Signature. Silicon Signature contains data which identifies SEEQ as the manufacturer and gives the product code. This allows device programmers to match the programming specification against the product which is to be programmed.

Silicon Signature is read by raising address A_9 to 12 ± 0.5 volts and bringing all other address inputs, plus chip enable, and output enable to V_{IL} with V_{CC} at 5 V. The two Silicon Signature bytes are selected by address input A_0.

Silicon Signature Bytes

	A_0	Data (Hex)
SEEQ Code	V_{IL}	94
Product Code 47F010	V_{IH}	1C

Mode Selection Table

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	V_{PP}	A_{0-16}	D_{0-7}
Read	V_{IL}	V_{IL}	V_{IH}	X	Address	D_{OUT}
Standby	V_{IH}	X	X	X	X	High Z
Byte Write	V_{IL}	V_{IH}	V_{IL}	V_P	Address	D_{IN}
Chip Erase Select	V_{IL}	V_{IH}	V_{IL}	TTL	X	X
Chip Erase	V_{IL}	V_{IH}	V_{IL}	V_P	X	'FF'

Absolute Maximum Stress Range*

Temperature
Storage ..... −65°C to +125°C
Under Bias ..... −10°C to +85°C

All Inputs except V_{PP} and outputs with respect to V_{SS} .....+7 V to −0.5 V

V_{PP} and A_9 with respect to V_{SS} .....14 V

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

E.S.D. Characteristics*

Symbol	Parameter	Value	Test Condition
V_{ZAP}	E.S.D. Tolerance	>2000 V	MIL-STD 883 Method 3015

* Characterization data — not tested.

Operating Conditions

	47F010
V_{CC} Supply Voltage	5V ± 10%
Temperature Range (Read)	0°C to 70°C
Temperature Range (Write/Erase)	25°C ± 5°C

Capacitance * T_A = 25°C, f =1 MHz

Symbol	Parameter	Value	Test Condition
C_{IN}	Input Capacitance	6 pF	V_{IN} = 0 V
C_{OUT}	Output capacitance	12 pF	$V_{I/O}$ = 0 V

* This parameter is measured only for initial qualifications and after process or design changes which may affect capacitance.

DC Operating Characteristics Over specified V_{CC} and temperature range

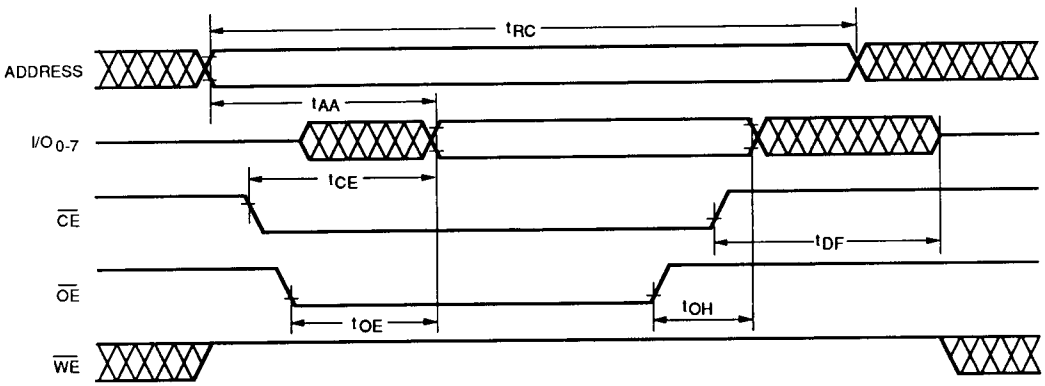
Symbol	Parameter	Limits			Test Condition
		Min.	Max.	Unit	
I_{LI}	Input Leakage		1	µA	V_{IN} = 0.1V to V_{CC}
I_{LO}	Output Leakage		10	µA	V_{IN} = 0.1 V to V_{CC}
V_P	Program/Erase Voltage	12.50	13.00	V	
V_{PR}	V_{PP} Voltage During Read	0	V_P	V	
I_{PP}	V_P Current				
	Standby Mode		200	µA	$\overline{CE}$ = V_{IH}, V_{PP} = V_{PR}
	Read Mode		200	µA	$\overline{CE}$ = V_{IL}, V_{PP} = V_{PR}
	Byte Write		30	mA	V_{PP} = V_P
	Chip Erase		60	mA	V_{PP} = V_P
I_{CC1}	Standby V_{CC} Current		400	µA	$\overline{CE}$ = V_{CC} –0.3V
I_{CC2}	Standby V_{CC} Current		5	mA	$\overline{CE}$ = V_{IH} min.
I_{CC3}	Active V_{CC} Current		40	mA	$\overline{CE}$ = V_{IL}
V_{IL}	Input Low Voltage	–0.3	0.8	V	
V_{IH}	Input High Voltage	2.0	7.0	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.1 ma
V_{OH1}	Output Level (TTL)	2.4		V	I_{OH} = –400 µA
V_{OH2}	Output Level (CMOS)	V_{CC} – 1.0		V	I_{OH} = –100 µA

READ
AC Characteristics

(Over specified V_{CC} and Temperature Range)

Symbol	Parameter	47F010 -200		47F010 -250		47F010 -300		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	200		250		300		ns
t_{AA}	Address to Data		200		250		300	ns
t_{CE}	$\overline{CE}$ to Data		200		250		300	ns
t_{OE}	$\overline{OE}$ to Data		75		100		150	ns
t_{DF}	$\overline{OE}/\overline{CE}$ to Data Float		50		60		100	ns
t_{OH}	Output Hold Time	0		0		0		ns

Read Timing



A.C. Test Conditions

Output Load: 1 TTL gate and C(load) = 100 pF
Input Rise and Fall Times: < 20 ns
Input Pulse Levels: 0.45V to 2.4V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

Byte Write

AC Characteristics

(Over specified V_{CC} and temperature range)

Symbol	Parameter	47F010		Unit
		Min.	Max.	
t_{VPS}	V_{PP} Setup Time	2		µs
t_{VPH}	V_{PP} Hold Time	150		µs
t_{CS}	$\overline{CE}$ Setup Time	0		ns
t_{CH}	$\overline{CE}$ Hold Time	0		ns
t_{OES}	$\overline{OE}$ Setup Time	10		ns
t_{OEH}	$\overline{OE}$ Hold Time	10		ns
t_{AS}	Address Setup Time	20		ns
t_{AH}	Address Hold Time	100		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	$\overline{WE}$ Pulse Width	100		ns
t_{WC}	Write Cycle Time	75		µs
t_{WR}	Write Recovery Time		1.5	ms

NOTE: In A.C. characteristics, all inputs to the device, e.g., setup time, hold time and cycle time, are tabulated as a minimum time; the user must provide a valid state on that input or wait for the state minimum time to assure proper operation. All outputs from the device, e.g. access time, erase time, recovery time, are tabulated as a maximum time, the device will perform the operation within the stated time.

Byte Write Timing

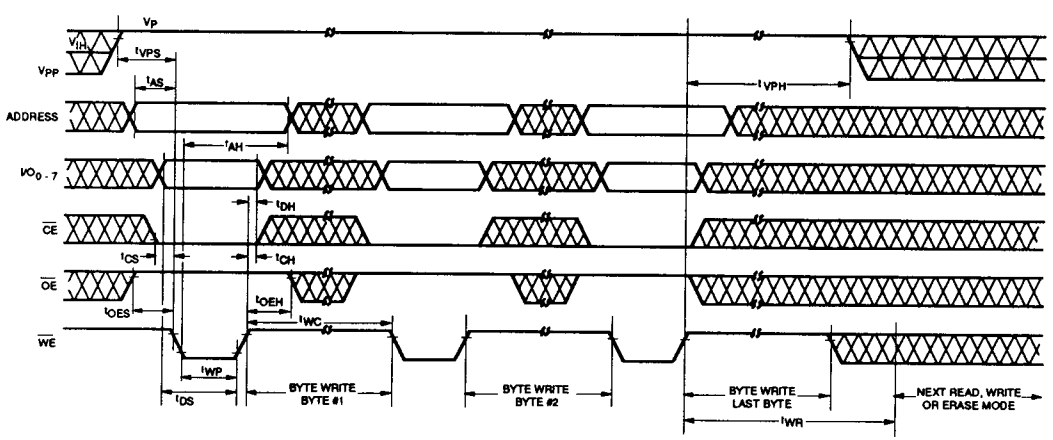
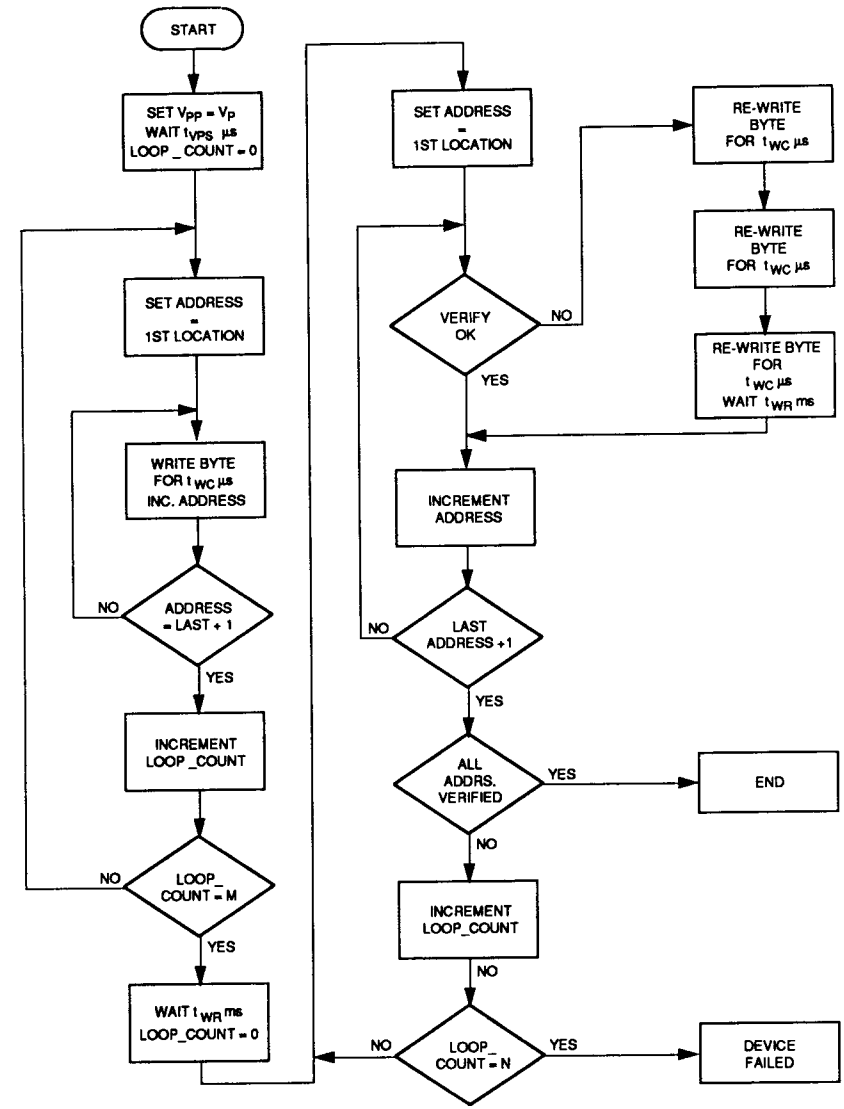


Figure 1
47F010 Write Algorithm



M = 3
N = 5

Chip Erase

AC Characteristics

(Over specified V_{CC} and temperature range)

Symbol	Parameter	47F010		Unit
		Min.	Max.	
t_{VPS}	V_{PP} Setup Time	2		µs
t_{VPH}	V_{PP} Hold Time	500		ms
t_{CS}	$\overline{CE}$ Setup Time	0		ns
t_{OES}	$\overline{OE}$ Setup Time	0		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}	Data Hold Time	0		ns
t_{WP}	$\overline{WE}$ Pulse Width	100		ns
t_{CH}	$\overline{CE}$ Hold Time	0		ns
t_{OEH}	$\overline{OE}$ Hold Time	0		ns
t_{ERASE}	Chip Erase Time	500		ms
t_{ER}	Erase Recovery Time		250	ms

Chip Erase Timing

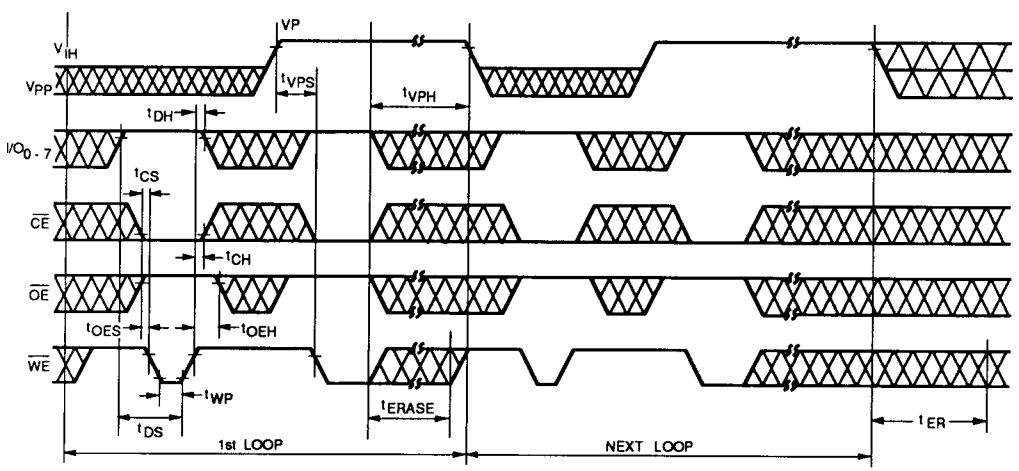
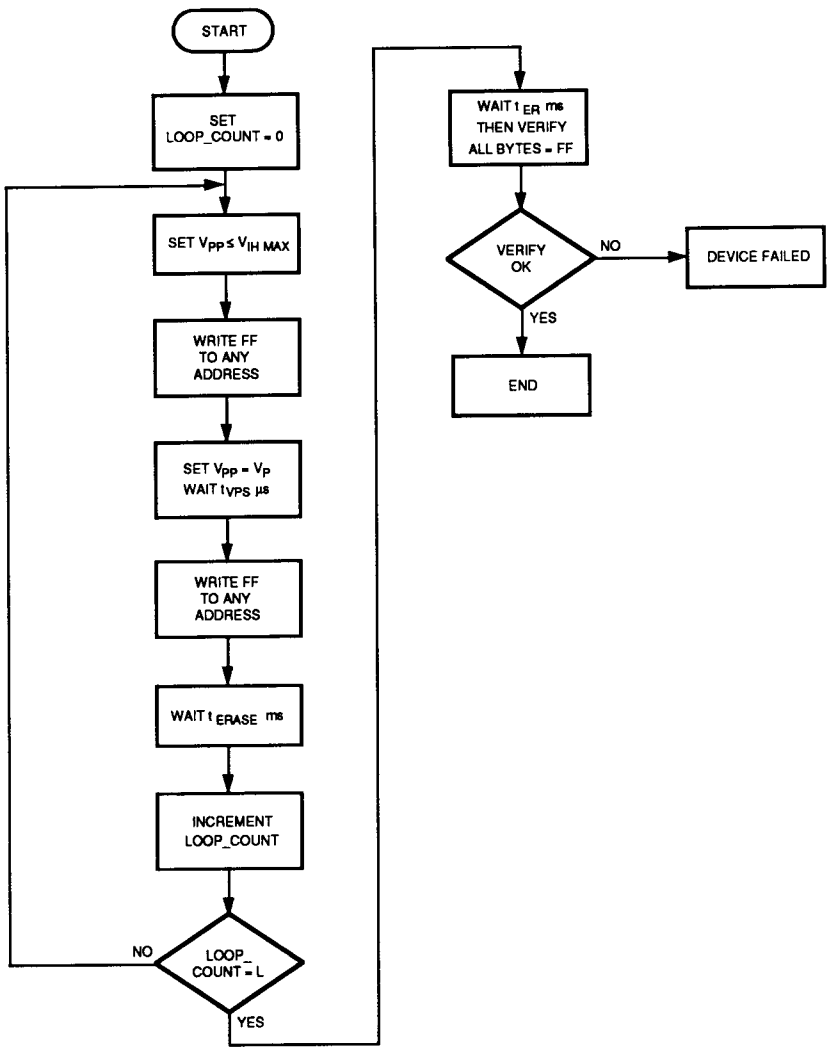


Figure 2
47F010 Chip Erase Algorithm



L = 20

Ordering Information

D	Q	47F010	– 200
Package Type	**Temperature Range (READ)**	**Device**	**Access Time**
D = Ceramic Dip P = Plastic Dip N = Plastic Leaded Chip Carrier	Q = 0 to 70° C	128K x 8 Flash EPROM	200 = 200 ns 250 = 250 ns 300 = 300 ns