DATA SHEET

BSP304; BSP304A
P-channel enhancement mode vertical D-MOS transistor

Product specification
Supersedes data of 1995 Apr 07
File under Discrete Semiconductors, SC13b

1997 Oct 22

Philips Semiconductors

PHILIPS

P-channel enhancement mode vertical D-MOS transistor

BSP304; BSP304A

FEATURES

- Direct interface to C-MOS, TTL etc.
- High speed switching
- No secondary breakdown.

APPLICATIONS

- Intended for use as a Line current interruptor in telephone sets and for applications in relay, high speed and line transformer drivers.

PINNING - TO-92 variant

PIN	SYMBOL	DESCRIPTION
BSP304		
1	g	gate
2	d	drain
3	s	source
BSP304A		
1	s	source
2	g	gate
3	d	drain

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a TO-92 variant package.

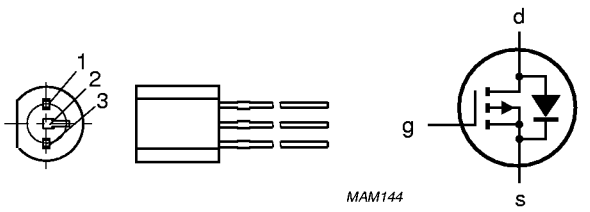


Fig.1 Simplified outline and symbol.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–300	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
V_{GSth}	gate-source threshold voltage	I_D = –1 mA; V_{DS} = V_{GS}	–1.95	–2.8	V
I_D	drain current (DC)		–	–170	mA
R_{DSon}	drain-source on-state resistance	I_D = –170 mA; V_{GS} = –10 V	–	17	Ω
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	1	W

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–300	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±20	V
I_D	drain current (DC)		–	–170	mA
I_{DM}	peak drain current		–	–0.75	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C; note 1	–	1	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

Note

1. Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for drain lead minimum 1 cm^2.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1	125	K/W

Note

1. Device mounted on a printed-circuit board, maximum lead length 4 mm; mounting pad for drain lead minimum 1 cm^2.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = –10 μA	–300	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = V_{GS}; I_D = –1 mA	–1.95	–	–2.8	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = –240 V	–	–	–100	nA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	±100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = –10 V; I_D = –170 mA	–	–	17	Ω
$\lvert y_{fs} \rvert$	forward transfer admittance	V_{DS} = –25 V; I_D = –170 mA	100	–	–	mS
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = –25 V; f = 1 MHz	–	60	90	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = –25 V; f = 1 MHz	–	15	30	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = –20 V; f = 1 MHz	–	5	15	pF
SWITCHING TIMES (see Figs 2 and 3)						
t_{on}	turn-on time	V_{GS} = 0 to –10 V; V_{DD} = –50 V; I_D = –250 mA	–	5	10	ns
t_{off}	turn-off time	V_{GS} = –10 to 0 V; V_{DD} = –50 V; I_D = –250 mA	–	15	30	ns

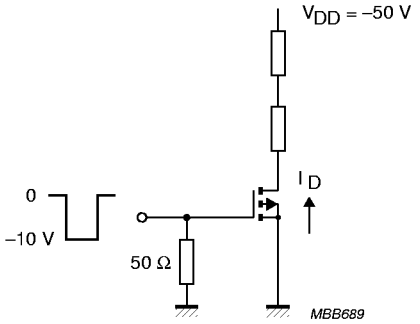


Fig.2 Switching time test circuit.

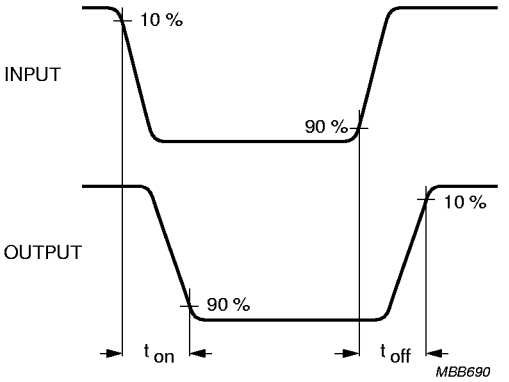


Fig.3 Input and output waveforms.

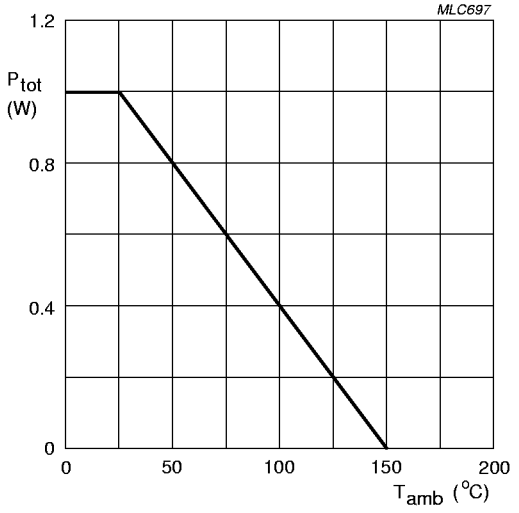
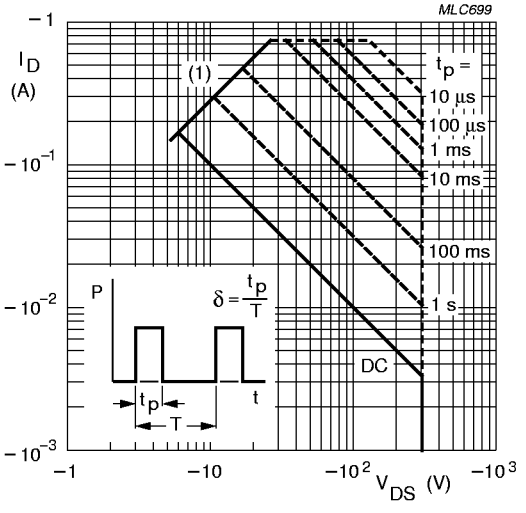
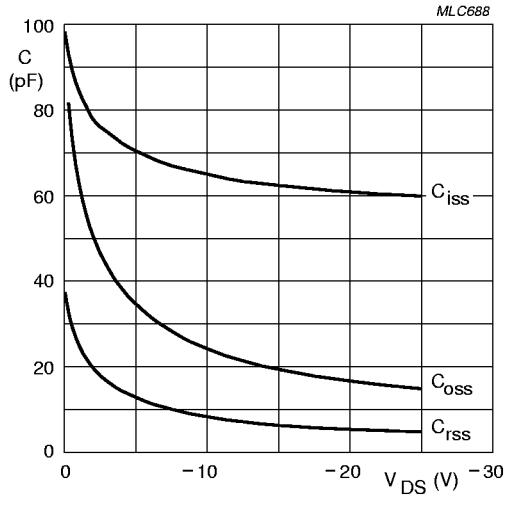


Fig.4 Power derating curve.



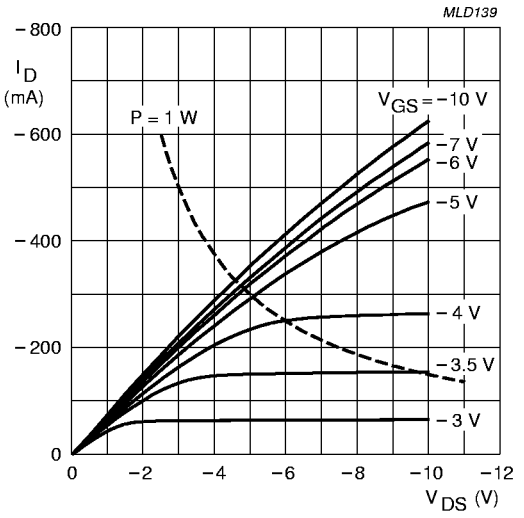
δ = 0.01.
T_{amb} = 25 °C.
(1) R_{DSon} limitation.

Fig.5 DC SOAR.



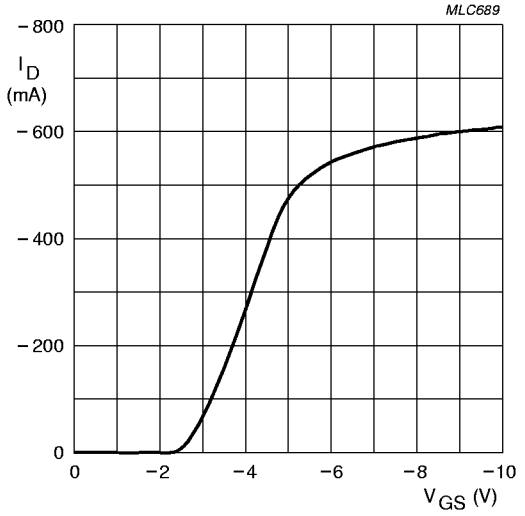
V_{GS} = 0.
T_j = 25 °C.
f = 1 MHz.

Fig.6 Capacitance as a function of drain source voltage; typical values.



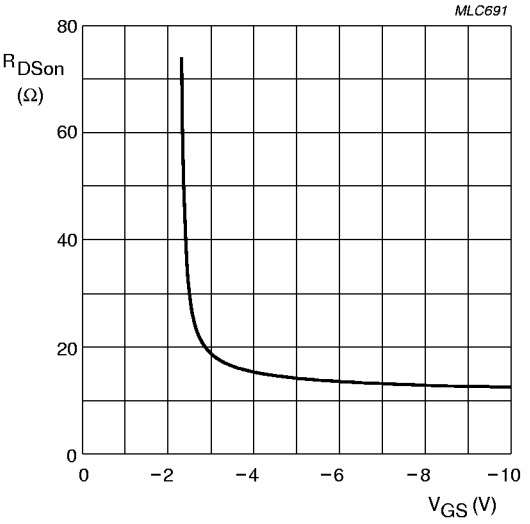
T_j = 25 °C.

Fig.7 Typical output characteristics.



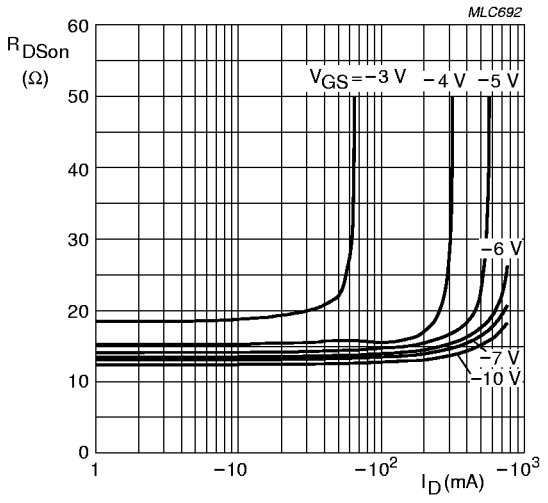
V_{DS} = −25 V.
T_j = 25 °C.

Fig.8 Typical transfer characteristics.



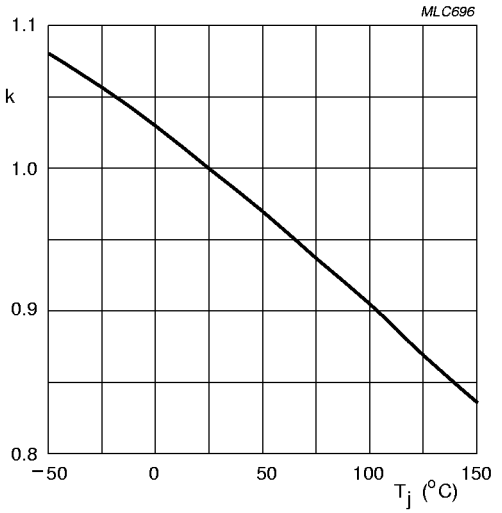
I_D = −170 mA.
T_j = 25 °C.

Fig.9 Drain-source on-state resistance as a function of gate-source voltage; typical values.



T_j = 25 °C.

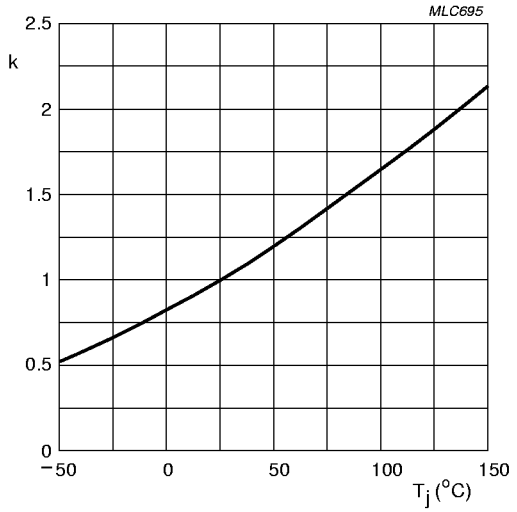
Fig.10 Drain-source on-state resistance as a function of drain current; typical values.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25°C}$$

Typical V_{GSth} at I_D = −1 mA; V_{DS} = V_{GS}.

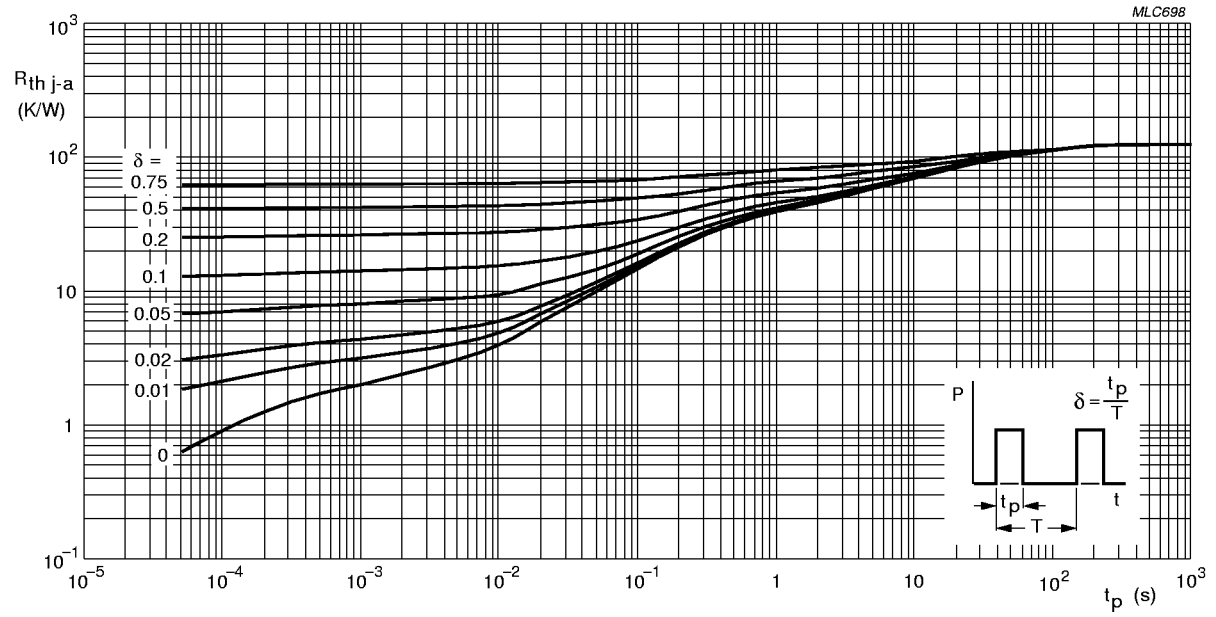
Fig.11 Temperature coefficient of gate-source threshold voltage.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25\ °C}$$

Typical R_{DSon} at I_D = −170 mA; V_{GS} = −10 V.

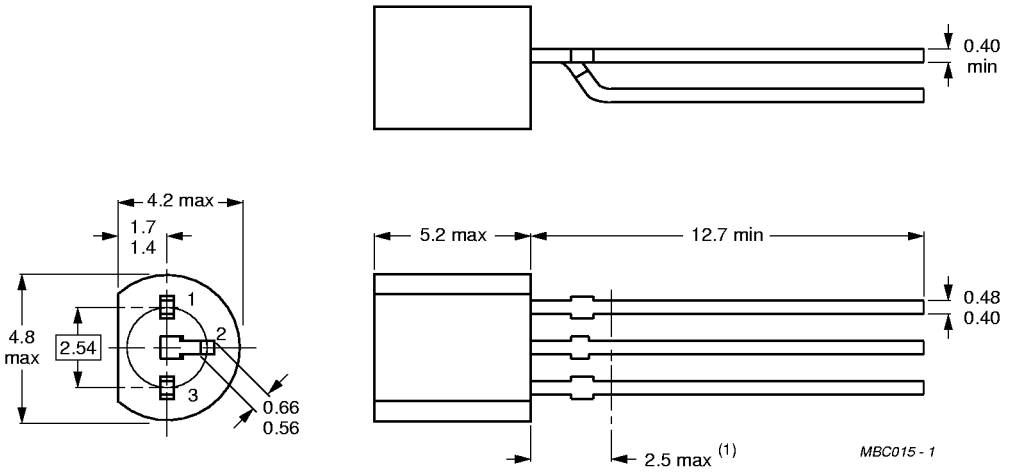
Fig.12 Temperature coefficient of drain-source on-state resistance.



T_{amb} = 25 °C.

Fig.13 Transient thermal resistance from junction to ambient as a function of pulse time; typical values.

PACKAGE OUTLINE



Dimensions in mm.

(1) Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

Fig.14 TO-92 variant.