



Integrated Device Technology, Inc.

HIGH-SPEED CMOS OCTAL D FLIP-FLOP (3-STATE)

IDT54AHCT534

FEATURES:

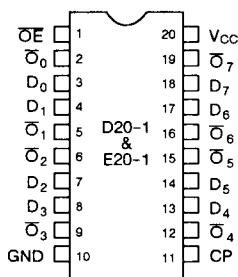
- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- 10ns typical clock to output
- $I_{OL} = 14\text{mA}$ over full military temperature range
- CMOS power levels ($5\mu\text{W}$ typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS ($5\mu\text{A}$ max.)
- Octal D flip-flop with 3-state output
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

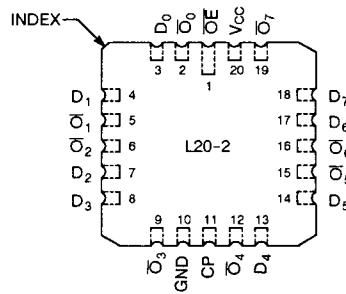
The IDT54AHCT534 are high-speed, low-power octal D-type flip-flops featuring separate D-type inputs for each flip-flop and 3-state outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable (\overline{OE}) are common to all flip-flops.

They are built using IDT's advanced CEMOS™, a dual metal CMOS technology.

PIN CONFIGURATIONS



DIP/CERPACK
TOP VIEW



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

SYMBOL	RATING	VALUE	UNIT
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T _A	Operating Temperature	-55 to +125	°C
T _{BIAS}	Temperature Under Bias	-65 to +135	°C
T _{STG}	Storage Temperature	-65 to +150	°C
P _T	Power Dissipation	0.5	W
I _{OUT}	DC Output Current	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER ⁽¹⁾	CONDITIONS	TYP.	MAX.	UNIT
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

$$T_A = -55^\circ\text{C to } +125^\circ\text{C}$$

$$V_{CC} = 5.0V \pm 10\%$$

$$V_{LC} = 0.2V$$

$$V_{HC} = V_{CC} - 0.2V$$

SYMBOL	PARAMETER	TEST CONDITIONS ⁽¹⁾		MIN.	TYP. ⁽²⁾	MAX.	UNIT
V _{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	—	—	V
V _{IL}	Input LOW Level	Guaranteed Logic Low Level		—	—	0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max., V _{IN} = V _{CC}		—	—	5	μA
I _{IL}	Input LOW Current	V _{CC} = Max., V _{IN} = GND		—	—	-5	μA
I _{OZ}	Off State (High Impedance) Output Current	V _{CC} = Max.	V _O = V _{CC}	—	—	10	μA
			V _O = GND	—	—	-10	
I _{SC}	Short Circuit Current	V _{CC} = Max. ⁽³⁾		-60	-120	—	mA
V _{OH}	Output HIGH Voltage	V _{CC} = 3V, V _{IN} = V _{LC} or V _{HC} , I _{OH} = -32μA		V _{HC}	V _{CC}	—	V
		V _{CC} = Min.	I _{OH} = -150μA	V _{HC}	V _{CC}	—	
V _{OL}	Output LOW Voltage	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -1.0mA	2.4	4.3	—	V
		V _{CC} = 3V, V _{IN} = V _{LC} or V _{HC} , I _{OL} = 300μA		—	GND	V _{LC}	
		V _{CC} = Min.	I _{OL} = 300μA	—	GND	V _{LC}	
V _{IN} = V _{IH} or V _{IL}		I _{OL} = 14mA	—	—	0.4	—	

NOTES:

- For conditions shown as max. or min. use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

 $V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	TEST CONDITIONS ⁽¹⁾	MIN.	TYP. ⁽²⁾	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ $V_{IN} \geq V_{HC}; V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$	—	0.001	1.5	mA
I_{CCT}	Power Supply Current Per TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(4)}$	—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁵⁾	$V_{CC} = \text{Max.}$ Outputs Open $\bar{OE} = \text{GND}$ One Bit Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25
I_{CC}	Total Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 1.0MHz$, 50% Duty Cycle $\bar{OE} = \text{GND}$ One Bit Toggling at $f_i = 500kHz$ 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC} (\text{AHCT})$	—	0.15	1.8
			$V_{IN} = 3.4V$ or $V_{IN} = \text{GND}$	—	0.65	3.8
		$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 1.0MHz$, 50% Duty Cycle $\bar{OE} = \text{GND}$ Eight Bits Toggling at $f_i = 250kHz$ 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC} (\text{AHCT})^{(6)}$	—	0.63	2.2
			$V_{IN} = 3.4V^{(6)}$ or $V_{IN} = \text{GND}$	—	2.88	11.2

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at $V_{CC} = 5.0V$, $+25^{\circ}\text{C}$ ambient and maximum loading.

3. Per TTL driven input ($V_{IN} = 3.4V$); all other inputs at V_{CC} or GND.

4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$$I_{CC} = I_{CCQ} + I_{CCT} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$$

I_{CCQ} = Quiescent Current

I_{CCT} = Power Supply Current for a TTL High Input ($V_{IN} = 3.4V$)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Input Frequency

N_i = Number of Inputs at f_i

All currents are in millamps and all frequencies are in megahertz.

5. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.

6. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
D ₀ - D ₇	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
OE	3-State Output Enable Input (Active LOW)
Q ₀ - Q ₇	Complementary 3-State Outputs

TRUTH TABLE

FUNCTION	INPUTS			Q _I	INTERNAL
	OE	CP	D _I		
Hi-Z	H	L	X	Z	NC
LOAD REGISTER	L L H	↗ ↗ ↗	L H H	H L Z	L H L

H = HIGH

L = LOW

X = Don't Care

Z = High Impedance

↗ = LOW-to-HIGH transition

NC = No Change

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION ⁽¹⁾	TYP.	MIN. ⁽²⁾	MAX.	UNIT
t _{PLH} t _{PHL}	Propagation Delay CP to Q _n	C _L = 50pF R _L = 500Ω	10.0	2.0	18.0	ns
t _{ZH} t _{ZL}	Output Enable Time		11.0	1.5	20.0	ns
t _{HZ} t _{LZ}	Output Disable Time		11.0	1.5	16.0	ns
t _S	Set-up Time HIGH or LOW D _n to CP		2.0	10.0	—	ns
t _H	Hold Time HIGH or LOW D _n to CP		0.5	1.5	—	ns
t _W	CP Pulse Width HIGH or LOW		7.0	16.0	—	ns

NOTES:

- See test circuit and waveforms.
- Minimum limits are guaranteed but not tested on Propagation Delays.

ORDERING INFORMATION

