BURST EDO DRAM

1 MEG x 16

FEATURES

- Burst order, interleave or linear, programmed by executing WCBR cycle after initialization
- Single power supply: +3.3V ±5%
- All inputs and outputs are LVTTL compatible with 5V input/output tolerance
- Industry-standard x16 pinout and packages
- High-performance CMOS silicon-gate process
- Refresh: $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) or $\overline{RAS}$ ONLY
- 1,024-cycle refresh (10 row-, 10 column-addresses)
- Four-cycle Extended Data-Out (EDO) burst accesses

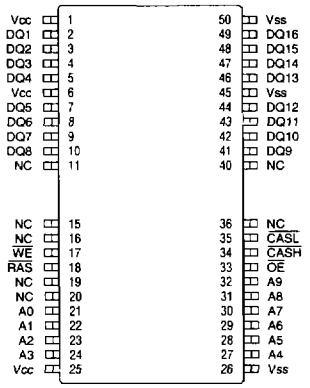
OPTIONS

	MARKING
• Timing	
52ns access; 15ns cycle	-52
60ns access; 16.6ns cycle	-60
70ns access; 20ns cycle	-70
• Packages	
Plastic TSOP (400 mil)	TG
Plastic SOJ (400 mil)	DJ
• Refresh	
Standard (1,024 cycles at 16ms)	None

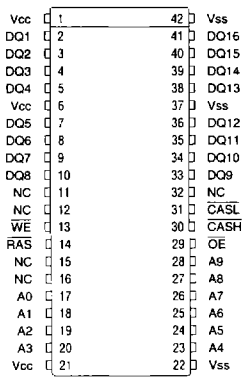
- Part Number Example: MT4LC1M16H5TG-52

PIN ASSIGNMENT (Top View)

44/50-Pin TSOP
(BB-1)



42-Pin SOJ
(BA-3)



GENERAL DESCRIPTION

The MT4LC1M16H5 is a randomly accessed solid-state memory containing 16,777,216 bits organized in a x16 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20 address bits, which are entered 10 bits (A0-A9) at $\overline{RAS}$ time and 10 bits (A0-A9) at $\overline{CAS}$ time.

The MT4LC1M16H5 is a burst access DRAM in which all READ and WORD WRITE access cycles occur in bursts of four. The bursts wrap around on a 4-byte boundry. This means that the two least significant bits of the $\overline{CAS}$ ($\overline{CASL}$ and $\overline{CASH}$) address are modified internally to produce each address of the burst sequence. The burst type, interleave or linear, is determined by executing a WCBR cycle (CBR cycle with $\overline{WE}$ LOW) with address A0 set to either HIGH or LOW. A0 LOW will program the device to execute linear bursts, A0 HIGH will program the bursts to be interleave. For future compatability it is strongly recommended that the information ($0010\ 000x_B$) where x=A0 is supplied on addresses A7-A0 during the WCBR cycle. The WCBR cycle must be followed by a $\overline{RAS}$-ONLY or CBR REFRESH cycle to exit this programming mode.

$\overline{RAS}$ HIGH and $\overline{CAS}$ HIGH ($\overline{CASL}$ and $\overline{CASH}$) terminates burst operations in the selected row, resets the burst counter, closes that row and decreases chip current to a reduced standby level. The chip is precharged for the next access during the $\overline{RAS}$ HIGH time.

READ CYCLE

A READ cycle is selected by $\overline{WE}$ input HIGH prior to the first $\overline{CAS}$ LOW transition of the burst ($\overline{CASL}$ or $\overline{CASH}$). During the READ burst cycle the $\overline{WE}$ input must remain HIGH for the burst to continue. Transition of the $\overline{WE}$ input during a burst causes the burst to terminate and places the outputs in a High-Z state. After a terminated burst, the next falling edge of $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$) will start a new burst access at the address present on the external address bus.

READ cycles always produce 16 bits of data (word). The READ timing is determined by the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$) to transition LOW and the last $\overline{CAS}$ to transition back HIGH. Both $\overline{CAS}$ signals may transistion but only one $\overline{CAS}$ is required for READ operations. If only one $\overline{CAS}$ is used for READ operations, the unused $\overline{CAS}$ must be held HIGH during the READ cycle.

WORD WRITE CYCLE

A WORD WRITE cycle is selected by $\overline{WE}$ input LOW during the first $\overline{CASL}$ and $\overline{CASH}$ LOW transition of the burst. Since $\overline{CASL}$ controls the lower byte (DQ1-DQ8) and $\overline{CASH}$ controls the upper byte (DQ9-DQ16), both $\overline{CASL}$ and $\overline{CASH}$ must transition for both bytes to be written. If only $\overline{CASL}$ or $\overline{CASH}$ transitions then only that corresponding byte will be written.

During a WORD WRITE cycle, data-in (D) is latched by the falling edge of $\overline{CAS}$ ($\overline{CASL}$ and $\overline{CASH}$). $\overline{WE}$ must be LOW prior to $\overline{CAS}$ ($\overline{CASL}$ and $\overline{CASH}$) going LOW. This places the input/output pins in the High-Z state allowing the data-in (D) to be driven on the bus. $\overline{WE}$ must remain LOW during the burst operation for the burst to complete. $\overline{WE}$ going HIGH during the burst terminates the burst operation and places the DQ pins in the High-Z state.

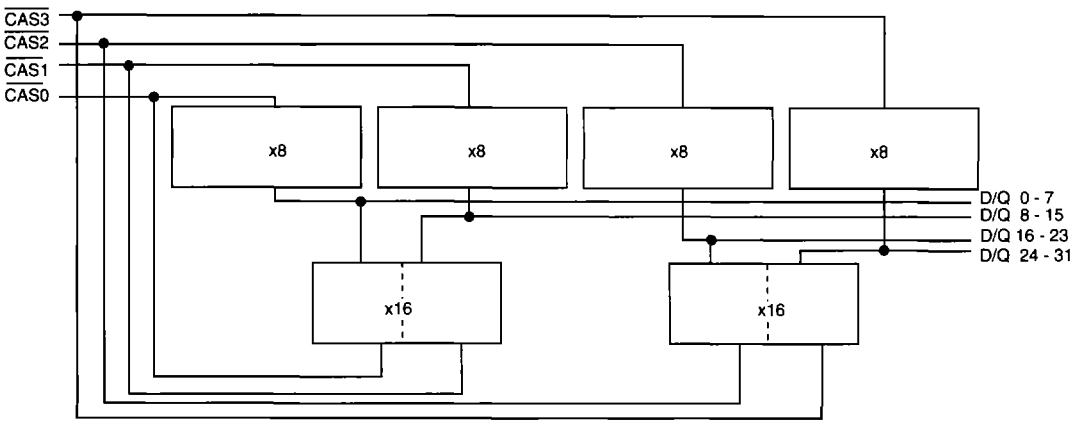
BYTE WRITE CYCLE

BYTE WRITE cycles can occur as bursts similar to word WRITE cycles. A transition on $\overline{CASH}$ or $\overline{CASL}$ increments the burst counter from which both bytes are internally addressed. During WRITEs ($\overline{WE}$ held LOW), $\overline{CASL}$ controls the lower byte (DQ1-DQ8) and $\overline{CASH}$ controls the upper byte DQ9-DQ16). However, in all practicality burst BYTE WRITE cycles do not make sense in most applications and therefore most BYTE WRITEs are single BYTE WRITE cycles. The full bus width needs to be burst accessed to keep the burst counters between devices from becoming out of step with each other. By performing a burst BYTE WRITE, only one of the $\overline{CAS}$ lines is being toggled, which causes the burst counter to be incremented for the byte not selected. This situation results in the burst counters on separate devices to become out of step with each other. Figure 1 demonstrates a 64-bit bus with two banks of Burst EDO DRAM. The first bank is composed of x8 devices and the second bank uses x16 devices. $\overline{CAS0}$ - $\overline{CAS3}$ are transitioned first together then independently. When $\overline{CAS}$ signals of all DRAMs that make up the bus width transition, the bytes are read from the DRAM array as expected and are in step between the DRAM devices. However, when some $\overline{CAS}$ signals are not transitioned 10 BYTE WRITEs, the DRAMs get out of step with each other. Depending on what organization of DRAM is being addressed, different results will occur. This comes from the fact that for x4 and x8 devices, a burst counter controls no more than one byte. However, for x16 devices, the burst counter controls a word (16 bits). This means that on a x16 device a LOW transition of either $\overline{CASL}$ and $\overline{CASH}$ will increment both the high byte and low byte burst counter.

Hence, byte WRITE cycles will almost always be a single BYTE WRITE followed by a terminate. Like a WORD WRITE cycle, the first $\overline{CAS}$ ($\overline{CASL}$ or $\overline{CASH}$) LOW transition when the $\overline{WE}$ input is LOW will start the WRITE burst cycle. Successive falling edges of $\overline{CAS}$ will WRITE to the next address locations in the burst sequence. The burst is terminated by transitioning the $\overline{WE}$ input. $\overline{CASL}$ LOW will WRITE the lower BYTE (DQ1-DQ8) while $\overline{CASH}$ is held HIGH. $\overline{CASH}$ LOW will WRITE the upper BYTE (DQ9-DQ16) while $\overline{CASL}$ is held HIGH.

MEMORY ARRAY ORGANIZATION

D0-7	D8-15	D16-23	D24-31
byte 0	byte 1	byte 2	byte 3
byte 4	byte 5	byte 6	byte 7
byte 8	byte 9	byte 10	byte 11
byte 12	byte 13	byte 14	byte 15



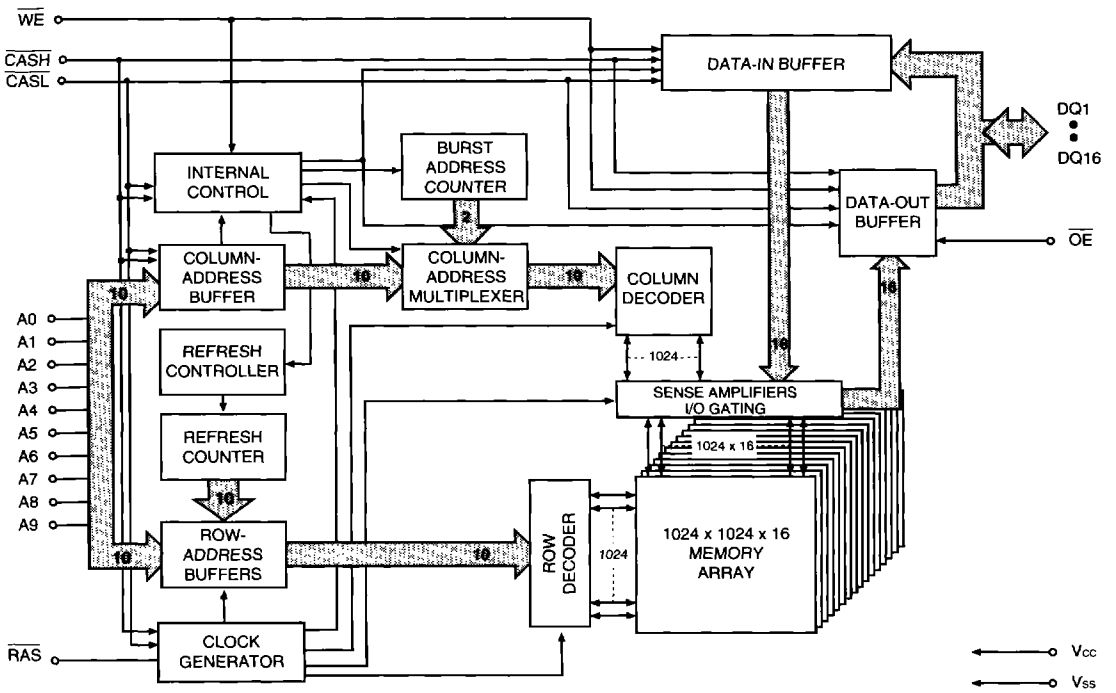
CAS WRITE SEQUENCE

	x8				x16			
Beginning	B0*	B1	B2	B3	B0	B1	B2	B3
CAS 0-3 transition	B4	B5	B6	B7	B4	B5	B6	B7
CAS 0 tansition	B8	X	X	X	B8	X	X	X
CAS 1 transition	X	B9	X	X	X	B13	X	X
CAS 2 transition	X	X	B10	X	X	X	B10	X
CAS 3 transition	X	X	X	B11	X	X	X	B15

*Shaded areas indicate that the byte was written by the CAS transition, X indicates byte not written.

Figure 1
BYTE WRITE EXAMPLES

FUNCTIONAL BLOCK DIAGRAM
Burst EDO



EDO BURST MODE TRUTH TABLE

PRESENT STATE	RESULTING STATE	$\overline{RAS}$	$\overline{CASL}$	$\overline{CASH}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES		DATA
							Row	Column	DQ
Any	Idle	L→H	H	H	X	X	X	X	High-Z
Idle	Row Open	H→L	H	H	X	X	ROW	X	High-Z
Idle	CBR REFRESH	H→L	L	L	H	X	X	X	High-Z
Row Open	$\overline{RAS}$-ONLY REFRESH	L	H	H	X	X	ROW	X	High-Z
Row Open	WORD READ burst	L	H→L	H	H	L	X	COL	Data-Out
Row Open	WORD READ burst	L	H	H→L	H	L	X	COL	Data-Out
Row Open	WORD WRITE burst	L	H→L	H→L	L	X	X	COL	Data-In
Row Open	LOWER BYTE WRITE burst	L	H→L	H	L	X	X	COL	Data-In
Row Open	UPPER BYTE WRITE burst	L	H	H→L	L	X	X	COL	Data-In
READ burst	TERMINATE READ burst	L	H/L	H/L	H→L	X	X	X	High-Z
WRITE burst	TERMINATE WRITE burst	L	H/L	H/L	L→H	X	X	X	High-Z
Idle	PROGRAM burst type	H→L	L	L	L	X	A0[1]	X	High-Z
PROGRAM	EXIT PROGRAM MODE	H→L	L	L	H	X	X	X	High-Z
PROGRAM	EXIT PROGRAM MODE	L	H	H	X	X	ROW	X	High-Z

NOTE: 1. A WCBR cycle determines the burst sequence. A0=LOW sets the burst sequence to linear, A0=HIGH set the burst sequence to interleave. A8 through A9 are "don't cares." A7-A0 should contain the sequence ($0010\ 000x_B$ where x=A0) to ensure future compatability. A refresh cycle ($\overline{RAS}$ ONLY or CBR) must follow the WCBR cycle to exit the programming mode.

INTERLEAVE BURST SEQUENCE TABLE

	ADDRESSES USED		
OPERATION	**A9 - A2**	**A1**	**A0**
First access, register external CAS address	A9 - A2	A1	A0
Second access, (first burst address)	registered A9 - A2	registered A1	registered $\overline{A0}$
Third access (second burst address)	registered A9 - A2	registered $\overline{A1}$	registered A0
Fourth access (third burst address)	registered A9 - A2	registered $\overline{A1}$	registered $\overline{A0}$

INTERLEAVE BURST ADDRESS TABLE

FIRST ADDRESS	SECOND ADDRESS	THIRD ADDRESS	FOURTH ADDRESS
X...X00	X..X01	X..X10	X..X11
X..X01	X..X00	X..X11	X..X10
X..X10	X..X11	X..X00	X..X01
X..X11	X..X10	X..X01	X..X00

LINEAR BURST ADDRESS TABLE

FIRST ADDRESS	SECOND ADDRESS	THIRD ADDRESS	FOURTH ADDRESS
X...X00	X..X01	X..X10	X..X11
X..X01	X..X10	X..X11	X..X00
X..X10	X..X11	X..X00	X..X01
X..X11	X..X00	X..X01	X..X10

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to V_{SS} ..... -1.0V to +4.6V
Voltage on Inputs, NC or I/O pins
Relative to V_{SS} ..... -1.0V to +5.5V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 600mW
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 11) (V_{CC} = +3.3V ±5%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	3.13	3.47	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.0	5.5	V	2
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	2
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 5.5V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2mA)	V_{OH}	2.4		V	21
Output Low Voltage (I_{OUT} = 2mA)	V_{OL}		0.4	V	

		MAX				
PARAMETER/CONDITION	SYM	-52	-60	-70	UNITS	NOTES
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CASL}$ = $\overline{CASH}$ = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CASL}$ = $\overline{CASH}$ = V_{CC} -0.2V)	I_{CC2}	500	500	500	µA	
OPERATING CURRENT: Closed Row Burst READ/WRITE Average power supply current; (^tPC = ^tPC [MIN]; 50% duty cycle on $\overline{RAS}$; Open Row, four Cycle Burst, Close Row)	I_{CC3}	150	140	130	mA	5, 17
OPERATING CURRENT: Open Row Burst READ/WRITE Average power supply current (Alternating four cycle burst followed by four cycles of inactivity; ^tPC = ^tPC [MIN])	I_{CC4}	110	100	90	mA	5, 17
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current (Address Cycling; $\overline{RAS}$ Cycling; $\overline{CASL}$,$\overline{CASH}$ = V_{IH}; ^tRAS = ^tRAS [MIN]; ^tRP = ^tRP [MIN])	I_{CC5}	190	180	160	mA	4, 17
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$,$\overline{CASL}$,$\overline{CASH}$, Cycling: ^tRAS = ^tRAS [MIN]; ^tRP = ^tRP [MIN])	I_{CC6}	170	160	150	mA	4, 6

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: Addresses, $\overline{WE}$, $\overline{OE}$	C_{I1}		5	pF	3
Input Capacitance: $\overline{RAS}$	C_{I2}		6	pF	3
Input Capacitance: $\overline{CASL}$, $\overline{CASH}$	C_{I3}		4	pF	3
Input/Output Capacitance: DQ	C_{IO}		7	pF	3

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 7, 8, 9, 10, 15) (V_{CC} = +3.3V ±5%)

AC CHARACTERISTICS		-52		-60		-70			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from $\overline{CAS}$	^tAA		25		28.2		35	ns	12
Column-address setup time	^tASC	1.5		1.5		1.5		ns	
Row-address setup time	^tASR	1.5		1.5		1.5		ns	
Burst terminate hold time	^tBTH	3		3		3		ns	
Output disable from burst terminate	^tBTHZ	7	13	7	13	7	13	ns	13, 16
Access time from $\overline{CAS}$	^tCAC		10		11		15	ns	
Column-address hold time	^tCAH	8.5		8.5		8.5		ns	
$\overline{CAS}$ pulse width	^tCAS	5	10,000	5	10,000	5	10,000	ns	
$\overline{CASL}$ and $\overline{CASH}$ coincident HIGH time	^tCCH	5		5		5		ns	18
$\overline{CAS}$ hold time (CBR or WCBR)	^tCHR	15		15		15		ns	6
$\overline{CAS}$ to output in Low-Z	^tCLZ	3		3		3		ns	13
Data Hold time from $\overline{CAS}$ LOW	^tCOH	3		3		3		ns	
$\overline{CAS}$ precharge time	^tCP	5		5		5		ns	
$\overline{CAS}$ precharge time (CBR or WCBR)	^tCPN	10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	^tCRP	10		10		10		ns	
$\overline{CAS}$ LOW to $\overline{RAS}$ HIGH (WRITE only)	^tCRW	15		16.6		20		ns	
Skew between $\overline{CASL}$ and $\overline{CASH}$ (WRITE only)	^tCSK		2		2		2	ns	19
$\overline{CAS}$ setup time (CBR or WCBR)	^tCSR	10		10		10		ns	6
Data-in hold time	^tDH	5		5		5		ns	
Data-in setup time	^tDS	0		0		0		ns	22
Ouput Disable	^tOD	4	10	4	10	4	15	ns	13
Ouput Enable access time	^tOEA		10		12		15	ns	
Ouput Enable hold (only near $\overline{CAS}$)	^tOEH	5		5		5		ns	
$\overline{OE}$ to output in Low-Z	^tOELZ	3		3		3		ns	13
$\overline{OE}$ HIGH pulse width	^tOEP	10		10		10		ns	
Ouput Enable setup (only near $\overline{CAS}$)	^tOES	3		3		3		ns	
Output buffer turn-off delay	^tOFF	4	10	4	10	4	15	ns	13
Burst EDO cycle time	^tPC	15		16.6		20			
Access time from $\overline{RAS}$	^tRAC		52		60		70	ns	
Row-address hold time	^tRAH	8.5		8.5		8.5		ns	
$\overline{RAS}$ pulse width	^tRAS	52	125,000	60	125,000	70	125,000	ns	
Random Read or Write cycle time	^tRC	90		110		130			
$\overline{RAS}$ to $\overline{CAS}$ delay time	$^tRCD1$	20		20		20		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	$^tRCD2$	40		45		55		ns	
Read command hold time	^tRCH	5		5		5		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 7, 8, 9, 10, 15) (V_{CC} = +3.3V ±5%)

AC CHARACTERISTICS		-52		-60		-70			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Read command setup time	^{t}RCS	3		4		5		ns	
Refresh period (1,024 cycles)	^{t}REF		16		16		16	ms	
$\overline{RAS}$ precharge time	^{t}RP	30		40		50		ns	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	^{t}RPC	5		5		5		ns	
$\overline{RAS}$ hold time	^{t}RSH	0		0		0		ns	
Transition time (rise or fall)	^{t}T	1.5	50	1.5	50	1.5	50	ns	
Burst Terminate pulse width	^{t}TP	6		6		8		ns	14
Write command hold time	^{t}WCH	5		5		5		ns	
$\overline{WE}$ command setup time	^{t}WCS	3		4		5		ns	
Ouput Disable from $\overline{WE}$ LOW	^{t}WHZ	4	10	4	10	4	15	ns	13, 16
$\overline{WE}$ hold time (CBR or WCBR)	^{t}WRH	10		10		10		ns	
$\overline{WE}$ setup time (CBR or WCBR)	^{t}WRP	10		10		10		ns	

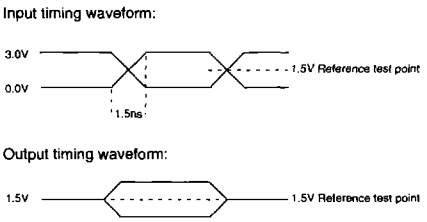


Figure 2
TIMING SPECIFICATIONS

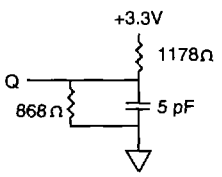


Figure 3
HIGH-Z OUTPUT LOAD

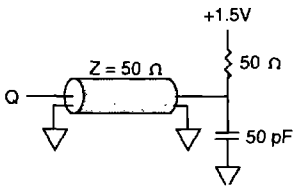


Figure 4
AC TIMING OUTPUT LOAD EQUIVALENT

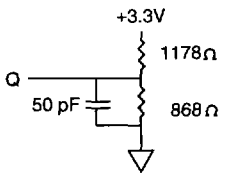
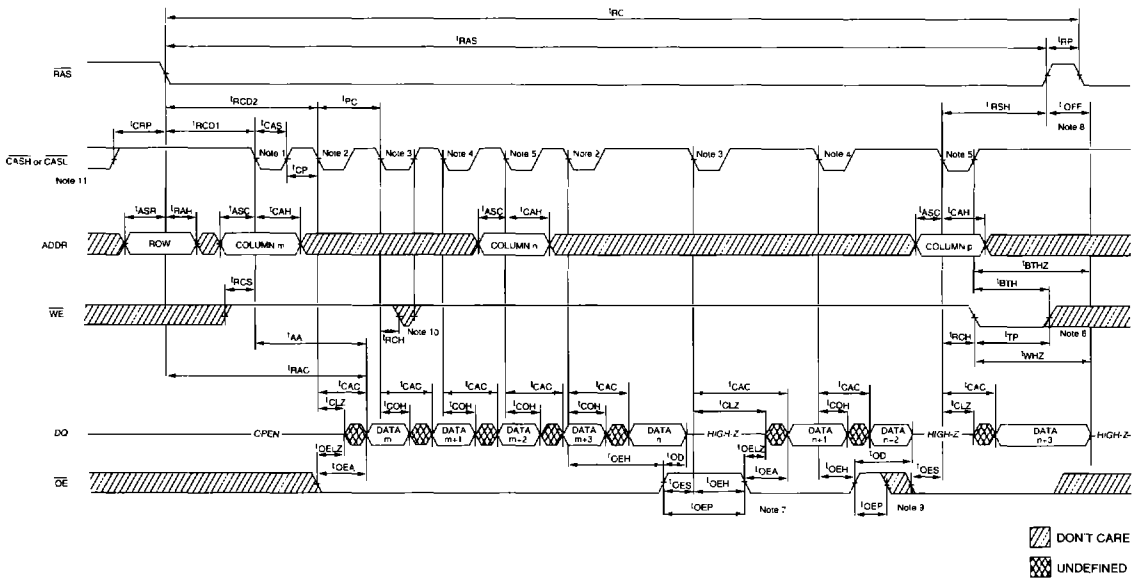


Figure 5
OUTPUT LOAD EQUIVALENT

NOTES

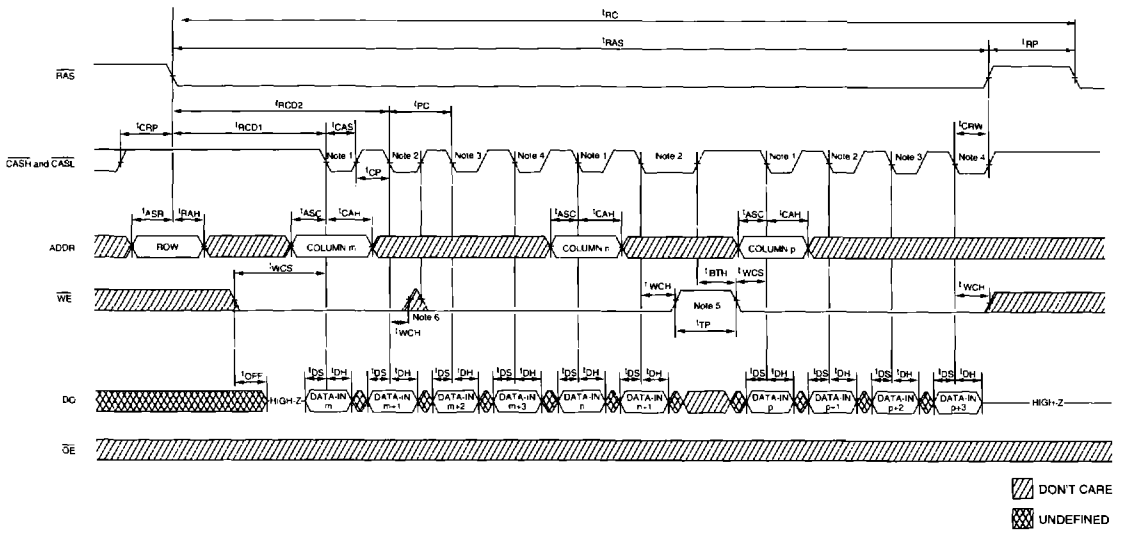
1. All voltages referenced to V_{SS}.
2. Input Power-up: $V_{IH} \leq +5.5V$ and $V_{CC} \leq +3.13V$ for $t \leq 200ms$.
3. This parameter is sampled. $V_{CC} = 3.3V \pm 5\%$; f = 1 MHz.
4. I_{CC} is dependent on cycle rates.
5. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum ^tPC and 50 percent duty cycle. The outputs are open.
6. Enables on-chip refresh and address counters.
7. Initialization consists of an initial pause of 100µs after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH). This sequence must be executed before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded. A WCBR cycle must be executed to initalize the burst type, interleave or linear followed by a $\overline{RAS}$-ONLY or CBR REFRESH cycle.
8. AC characteristics assume $^tT = 1.5ns$.
9. All output timings are referenced to 1.5V and all input timings are referenced to 1.5V, unless otherwise specified. Inputs must be driven to the appropriate voltage levels indicated by the corresponding timing diagrams when AC specifications are measured, as shown in Figure 2.
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. NC pins are assumed to be left floating and are not tested for leakage.
12. ^tAA is a calculated specification which is the sum of ^tPC and ^tCAC.
13. Output loading is specified with $C_L = 5pF$ as in Figure 3. Transition is measured ±200mV from steady state voltage. These parameters are sampled.
14. Applies only during burst termination operation.
15. AC output loading is specified with $C_L = 50pF$ as in Figure 4. Figure 5 is shown for reference. Transition is measured at the 1.5V reference level.
16. The DQs will continue to drive data out until both ^tBTHZ (MIN) and ^tWHZ (MIN) have been satisfied and will reach the High-Z state once both ^tBTHZ (MAX) and ^tWHZ (MAX) have been satisfied.
17. Address transitions once per burst access.
18. The $\overline{CASL}$ and $\overline{CASH}$ HIGH pulse widths must be concurrently HIGH for at least this limit.
19. The skew between $\overline{CASL}$ and $\overline{CASH}$ is only required for WRITE cycles and is required only between the $\overline{CASL}$ and $\overline{CASH}$ for a specific device.
20. ^tCPC is specified for back to back cycles where either $\overline{CASL}$ or $\overline{CASH}$ starts the first cycle and the other $\overline{CAS}$ starts the following cycle.
21. The outputs are designed to drive -5mA (I_{OH}) and 4.2mA (I_{OL}) when the 5V-tolerant I/Os are connected to a 5V bus rather than a 3.3V bus.
22. Valid data-in is referenced from when a valid logic level (V_{IH}, V_{IL}) has been achieved.

BURST EDO
READ CYCLE



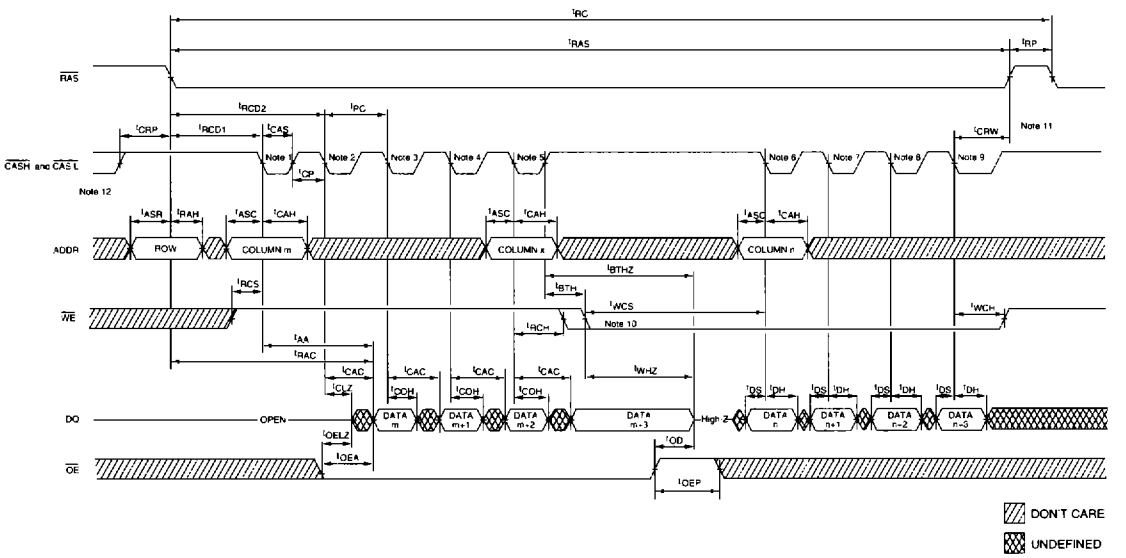
NOTE:
1. Latch column address; start READ cycle.
2. Output data 1; increment burst counter.
3. Output data 2; increment burst counter.
4. Output data 3; increment burst counter.
5. Output data 4; latch column address; start READ cycle.
6. $\overline{WE}$ transitioning LOW will terminate the burst and reset the burst counter provided ^{t}TP and ^{t}BTH are satisfied. The DQs will continue to drive data out until both ^{t}BTHZ (MIN) and ^{t}WHZ (MIN) have been satisfied and will reach the High-Z state once both ^{t}BTHZ (MAX) and ^{t}WHZ (MAX) have been satisfied.
7. ^{t}OES and ^{t}OEH are only required when $\overline{OE}$ transitions around the falling edge of $\overline{CASL}$ and $\overline{CASH}$.
8. The combination of $\overline{RAS}$ and $\overline{CAS}$ HIGH close the row and place the DQs in the High-Z state. ^{t}OFF is measured from the last signal ($\overline{RAS}$ or $\overline{CAS}$) that transitions HIGH.
9. When $\overline{OE}$ transitions HIGH, the DQ pins are placed in the High-Z state and will remain in the High-Z state until another $\overline{CAS}$ LOW transition occurs, regardless of the state of $\overline{OE}$.
10. $\overline{WE}$ transitioning LOW and returning HIGH prior to $\overline{CAS}$ going HIGH will not terminate the burst.
11. $\overline{CASL}$ and $\overline{CASH}$ are shown as if they are tied together and create a single $\overline{CAS}$. If not connected, either or both $\overline{CASL}$ and $\overline{CASH}$ may toggle. If only one $\overline{CAS}$ toggles, the other $\overline{CAS}$ must be held HIGH.

BURST EDO
WORD WRITE CYCLE



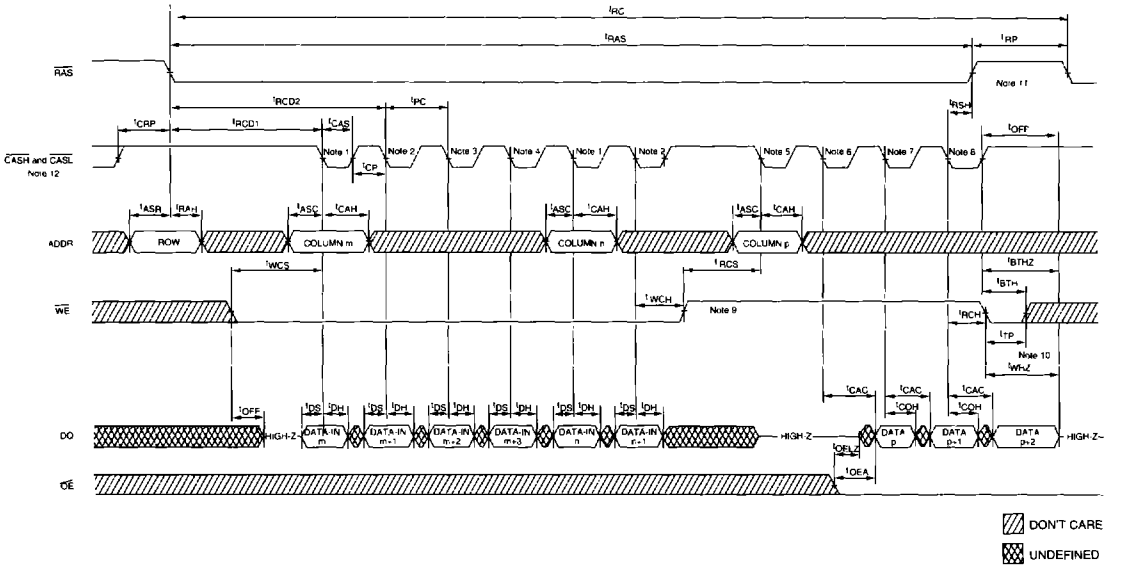
NOTE:
1. Latch column address; start burst WRITE cycle; write data 1.
2. Increment burst counter; write data 2.
3. Increment burst counter; write data 3.
4. Increment burst counter; write data 4.
5. $\overline{WE}$ transitioning HIGH will terminate the burst and reset the burst counter provided ^{t}TP and ^{t}BTH are satisfied.
6. $\overline{WE}$ transitioning HIGH and returning LOW prior to $\overline{CAS}$ going HIGH will not terminate the burst.
7. $\overline{CASL}$ and $\overline{CASH}$ are shown as if they are tied together and create a single $\overline{CAS}$. If not connected, both $\overline{CASL}$ and $\overline{CASH}$ must toggle. If only one $\overline{CAS}$ toggles, the other $\overline{CAS}$ must be held HIGH.

BURST EDO
READ/WRITE (WORD) CYCLE



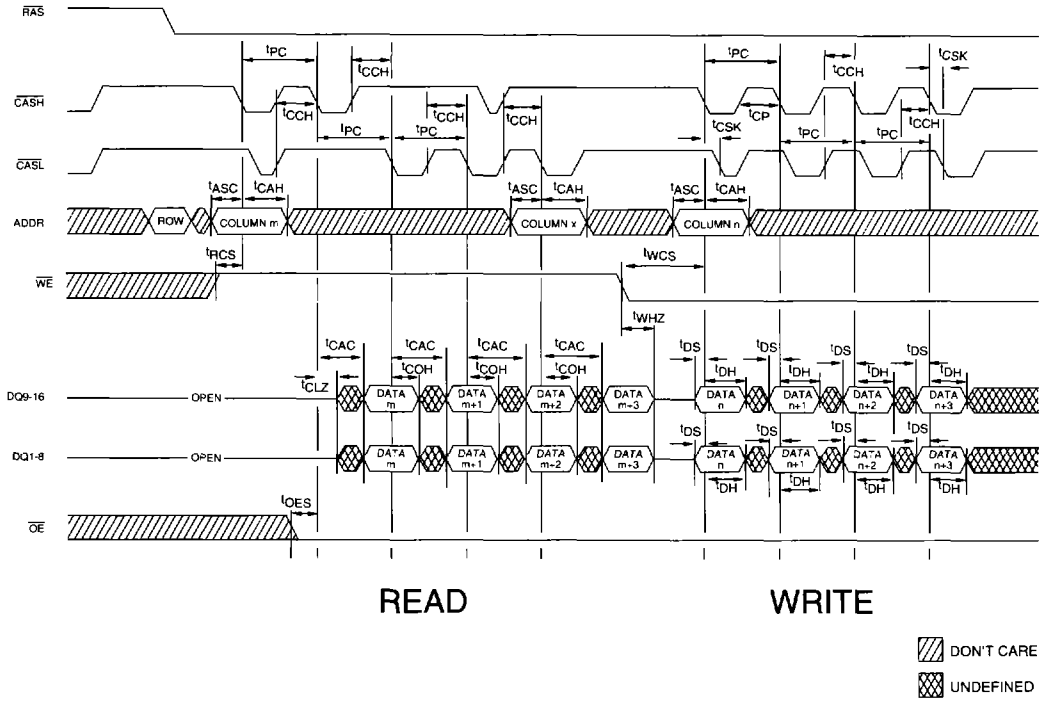
NOTE:
1. Latch column address; start burst READ cycle.
2. Output data 1; increment burst counter.
3. Output data 2; increment burst counter.
4. Output data 3; increment burst counter.
5. Output data 4; latch column address; start burst READ cycle.
6. Latch column address; start burst WRITE cycle; write data 1.
7. Increment burst counter; write data 2.
8. Increment burst counter; write data 3.
9. Increment burst counter; write data 4.
10. $\overline{WE}$ transitioning LOW will terminate the burst and reset the burst counter provided ^{t}TP and ^{t}BTH are satisfied. ^{t}TP is met by the READ burst being terminated by a WRITE burst. The DQs will continue to drive data out until both $^{t}BTHZ$ (MIN) and ^{t}WHZ (MIN) have been satisfied and will reach the High-Z state once both $^{t}BTHZ$ (MAX) and ^{t}WHZ (MAX) have been satisfied.
11. The combination of $\overline{RAS}$ and $\overline{CAS}$ HIGH close the row and place the DQ pins in the High-Z state.
12. $\overline{CASL}$ and $\overline{CASH}$ are shown as if they are tied together and create a single $\overline{CAS}$. If not connected, either or both $\overline{CASL}$ and $\overline{CASH}$ may toggle during READs but they must both toggle during WRITEs to perform a WORD WRITE. If only one $\overline{CAS}$ toggles, the other $\overline{CAS}$ must be held HIGH.

BURST EDO
WORD-WRITE/READ CYCLE



NOTE:
1. Latch column address; start burst WRITE cycle; write data 1.
2. Increment burst counter; write data 2.
3. Increment burst counter; write data 3.
4. Increment burst counter; write data 4.
5. Latch column address; start burst READ cycle.
6. Output data 1; increment column address.
7. Output data 2; increment column address.
8. Output data 3; increment column address.
9. $\overline{WE}$ transitioning HIGH will terminate the burst and reset the burst counter. The ^{t}BTH time is not required as it is satisfied by ^{t}RCS; ^{t}TP is met by the WRITE burst being terminated by a READ burst.
10. $\overline{WE}$ transitioning LOW will terminate the burst and reset the burst counter provided ^{t}TP and ^{t}BTH are satisfied. The DQs will continue to drive data out until both $^{t}BTHZ$ (MIN) and ^{t}WHZ (MIN) have been satisfied and will reach the High-Z state once both $^{t}BTHZ$ (MAX) and ^{t}WHZ (MAX) have been satisfied.
11. The combination of $\overline{RAS}$ and $\overline{CAS}$ HIGH close the row and place the DQ pins in the High-Z state. ^{t}OFF is measured from the last signal ($\overline{RAS}$ or $\overline{CAS}$) that transitions HIGH.
12. $\overline{CASL}$ and $\overline{CASH}$ are shown as if they are tied together and create a single $\overline{CAS}$. If not connected, either or both $\overline{CASL}$ and $\overline{CASH}$ may toggle during READs but they must both toggle during WRITEs to perform a WORD WRITE. If only one $\overline{CAS}$ toggles, the other $\overline{CAS}$ must be held HIGH.

BURST EDO
READ/WORD-WRITE CYCLE



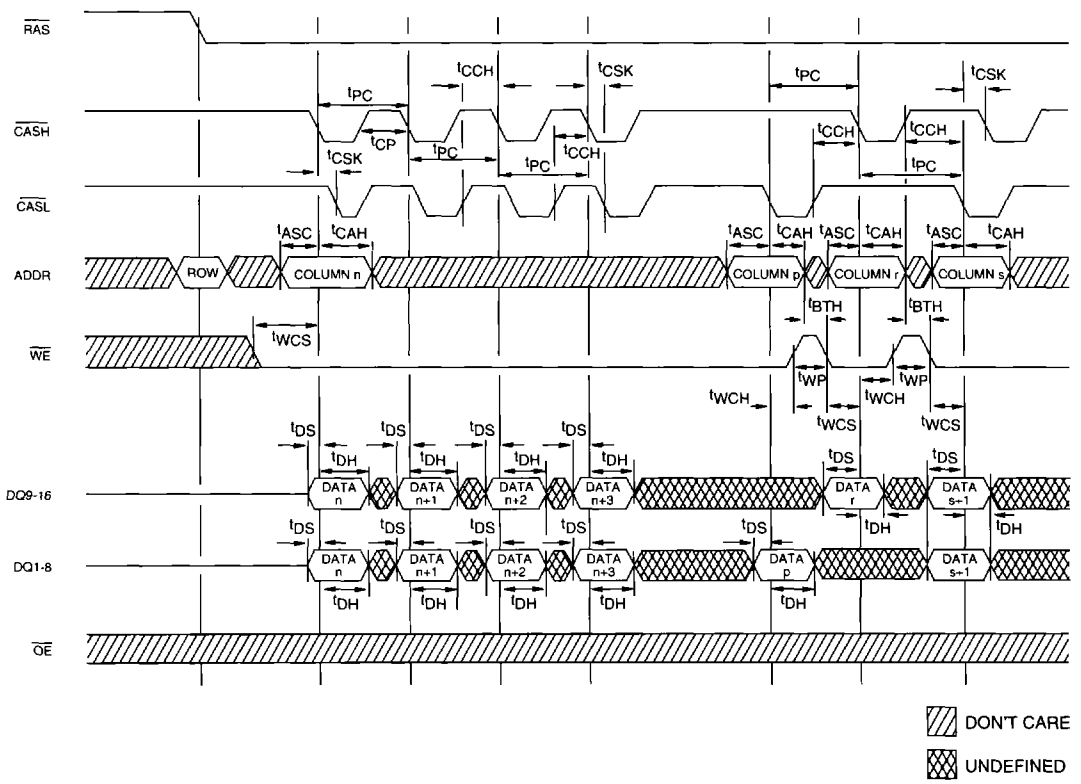
READ WRITE

DON'T CARE

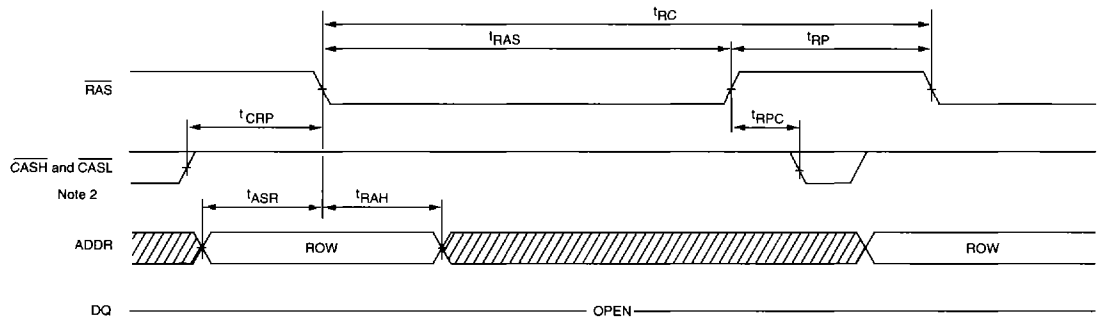
UNDEFINED

NOTE: 1. $\overline{\text{CASL}}$ and $\overline{\text{CASH}}$ are shown as if they are tied together and create a single $\overline{\text{CAS}}$. If not connected, either or both $\overline{\text{CASL}}$ and $\overline{\text{CASH}}$ may toggle during READs but they must both toggle during WRITEs to perform a WORD WRITE. If only one $\overline{\text{CAS}}$ toggles, the other $\overline{\text{CAS}}$ must be held HIGH.

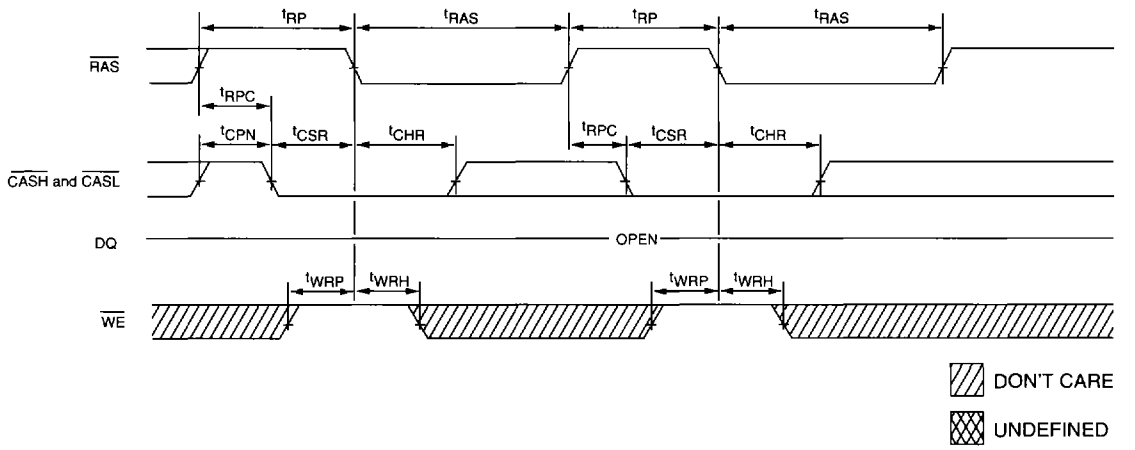
BURST EDO
WORD-WRITE/BYTE-WRITE CYCLE



RAS-ONLY REFRESH CYCLE



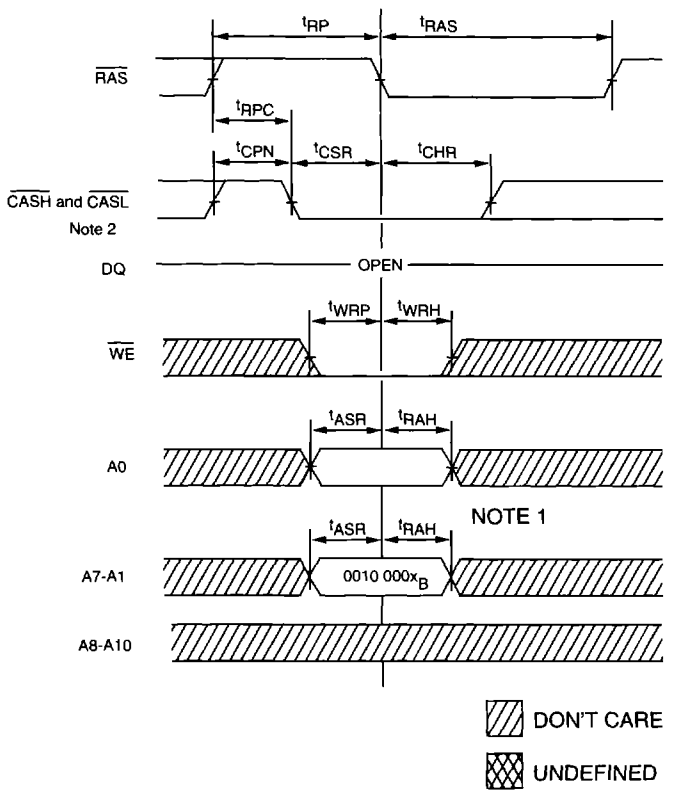
CBR REFRESH CYCLE



NOTE: 1. CBR REFRESH is recommended for all new designs to insure compatibility with future generation DRAMs. Micron and JEDEC recommend CBR REFRESH as the preferred method of refresh for the 64 Meg DRAM generation and beyond.

2. CASL and CASH are shown as if they are tied together and create a single CAS. If not connected, either or both CASL and CASH may toggle. If only one CAS toggles, the other CAS must be held HIGH.

WCBR PROGRAM CYCLE



NOTE:
1. A0 LOW sets the burst sequence to linear bursts. A0 HIGH sets the burst sequence to interleave bursts. Addresses A8 through A10 are "don't cares." Addresses A7-A10 should contain the state of (0010 $000x_B$ where x=A0) to ensure future compatability. The burst sequence will remain set until the device power is interrupted or another WCBR cycle is executed.
2. A $\overline{RAS}$-ONLY or CBR REFRESH cycle must be executed after the WCBR cycle to exit the programming mode.
3. $\overline{CASL}$ and $\overline{CASH}$ are shown as if they are tied together and create a single $\overline{CAS}$. If not connected, either or both $\overline{CASL}$ and $\overline{CASH}$ may toggle. If only one $\overline{CAS}$ toggles, the other $\overline{CAS}$ must be held HIGH.