Integrated Device Technology, Inc.

CMOS PARALLEL FLAGGED FIFO WITH $\overline{OE}$ 1K x 9, 2K x 9, 4K x 9

IDT 72021
IDT 72031
IDT 72041

FEATURES:

- First-In/First-Out dual-port memory
- Bit organization
  - IDT72021 – 1K x 9
  - IDT72031 – 2K x 9
  - IDT72041 – 4K x 9
- Ultra high speed
  - IDT72021 – 25ns access time, 35ns cycle time
  - IDT72031 – 35ns access time, 45ns cycle time
  - IDT72041 – 35ns access time, 45ns cycle time
- Low power CMOS
- Easily expandable in word depth and/or width
- Asynchronous and simultaneous read and write
- Functionally equivalent to IDT7202/03/04 with Output Enable ($\overline{OE}$) and Almost Empty/Almost Full Flag ($\overline{AEF}$)
- Four status flags: Full, Empty, Half-Full (single device mode), and Almost-Empty/Almost-Full (7/8 empty or 7/8 full in single device mode)
- Output Enable controls the data output port
- Auto-retransmit capability
- Available in 32-pin DIP and surface mount 32-pin LCC and PLCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

IDT72021/031/041s are high-speed, low-power, dual-port memory devices commonly known as FIFOs (First-In/First-Out). Data can be written into and read from the memory at independent rates. The order of information stored and extracted does not change, but the rate of data entering the FIFO might be different than the rate leaving the FIFO. Unlike a static RAM, no address information is required because the read and write pointers advance sequentially. The IDT72021/031/041s can perform asynchronous and simultaneous read and write operations. There are four status flags ($\overline{HF}$, $\overline{FF}$, $\overline{EF}$, $\overline{AEF}$) to monitor data overflow and underflow. Output Enable ($\overline{OE}$) is provided to control the flow of data through the output port. Additional key features are Write ($\overline{W}$), Read ($\overline{R}$), Retransmit ($\overline{RT}$), First Load ($\overline{FL}$), Expansion In ($\overline{XI}$) and Expansion Out ($\overline{XO}$). The IDT72021/031/041s are designed for those applications requiring data control flags and Output Enable ($\overline{OE}$) in multiprocessing and rate buffer applications.

The IDT72021/031/041s are fabricated using IDT's high-performance CEMOS™ technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, for high reliability systems.

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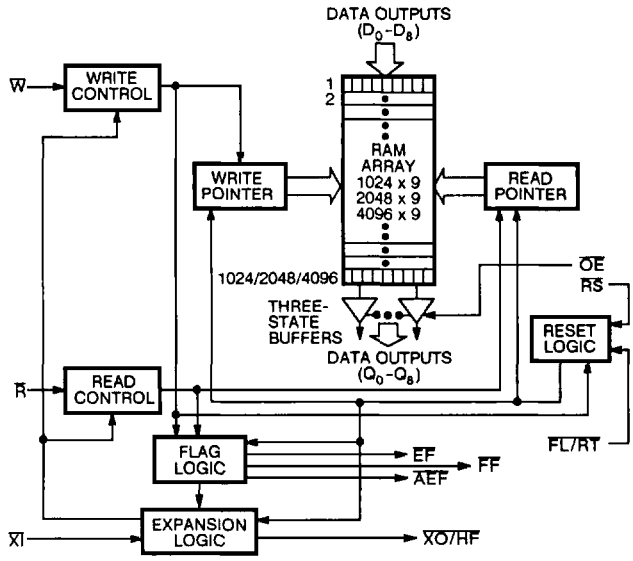
FUNCTIONAL BLOCK DIAGRAM



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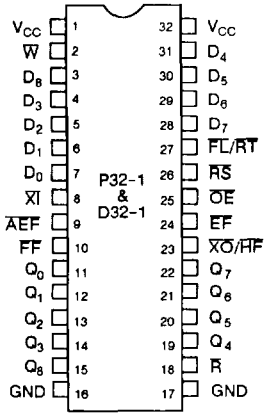
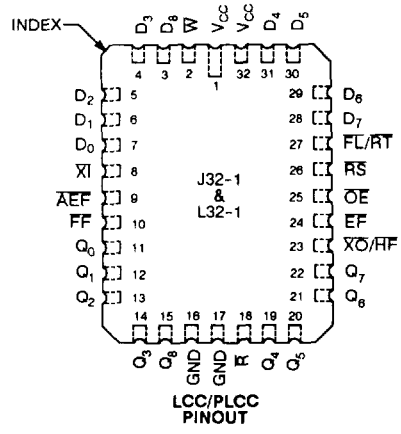
PIN CONFIGURATIONS



DIP
TOP VIEW



LCC/PLCC
PINOUT

PIN DESCRIPTIONS

SYMBOL	NAME	I/O	DESCRIPTION
D0-D8	Inputs	I	Data inputs for 9-bit wide data.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal READ and WRITE pointers are set to the first location of the RAM array, $\overline{HF}$ and $\overline{FF}$ go high, and $\overline{AEF}$ and $\overline{EF}$ go low. A reset is required before an initial WRITE after power-up. $\overline{R}$ and $\overline{W}$ must be high during $\overline{RS}$ cycle.
$\overline{W}$	Write	I	When WRITE is low, data can be written into the RAM array sequentially, independent of READ. In order for WRITE to be active, $\overline{FF}$ must be high. When the FIFO is full ($\overline{FF}$-low), the internal WRITE operation is blocked.
$\overline{R}$	Read	I	When READ is low, data can be read from the RAM array sequentially, independent of WRITE. In order for READ to be active, $\overline{EF}$ must be high. When the FIFO is empty ($\overline{EF}$-low), the internal READ operation is blocked. Q0-Q8 are in a high impedance condition.
$\overline{FL}/\overline{RT}$	First Load/ Retransmit	I	This is a dual purpose input. In the single device configuration ($\overline{XI}$ grounded), activating retransmit ($\overline{FL}/\overline{RT}$-low) will set the internal READ pointer to the first location. There is no effect on the WRITE pointer. $\overline{R}$ and $\overline{W}$ must be high before setting $\overline{FL}/\overline{RT}$ low. Retransmit is not compatible with depth expansion. In the depth expansion configuration, $\overline{FL}/\overline{RT}$-low indicates the first activated device.
$\overline{XI}$	Expansion In	I	In the single device configuration, $\overline{XI}$ is grounded. In depth expansion or daisy chain expansion, $\overline{XI}$ is connected to $\overline{XO}$ (expansion out) of the previous device.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is set low, the parallel output buffers receive data from the RAM array. When $\overline{OE}$ is set high, parallel three-state buffers inhibit data flow.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ goes low, the device is full and further WRITE operations are inhibited. When $\overline{FF}$ is high, the device is not full.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ goes low, the device is empty and further READ operations are inhibited. When $\overline{EF}$ is high, the device is not empty.
$\overline{AEF}$	Almost-Empty/ Almost-Full Flag	O	When $\overline{AEF}$ is low, the device is empty to 1/8 full or 7/8 to completely full. When $\overline{AEF}$ is high, the device is greater than 1/8 full, but less than 7/8 full.
$\overline{XO}/\overline{HF}$	Expansion Out/ Half-Full Flag	O	This is dual purpose output. In the single device configuration ($\overline{XI}$ grounded), the device is more than half full when $\overline{HF}$ is low. In the depth expansion configuration ($\overline{XO}$ connected to $\overline{XI}$ of the next device), a pulse is sent from $\overline{XO}$ to $\overline{XI}$ when the last location in the RAM array is filled.
Q0 - Q8	Outputs	O	Data outputs for 9-bit wide data.

STATUS FLAGS

NUMBER OF WORDS IN FIFO			$\overline{FF}$	$\overline{AEF}$	$\overline{HF}$	$\overline{EF}$
1K	2K	4K				
0	0	0	H	L	H	L
1-127	1-255	1-511	H	L	H	H
128-512	256-1024	512-2048	H	H	H	H
513-896	1025-1792	2049-3584	H	H	L	H
897-1023	1793-2047	3585-4095	H	L	L	H
1024	2048	4096	L	L	L	H

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	–	–	V
V_{IH}	Input High Voltage Military	2.2	–	–	V
V_{IL} (1)	Input Low Voltage Commercial & Military	–	–	0.8	V

NOTE:

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS – IDT72021

(Commercial: V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	IDT72021 COMMERCIAL t_A = 25, 35ns			IDT72021 MILITARY t_A = 30, 40ns			IDT72021 COMMERCIAL t_A = 50, 65, 80, 120ns			IDT72021 MILITARY t_A = 50, 65, 80, 120ns			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
I_{LI} (1)	Input Leakage Current (Any Input)	-1	–	1	-10	–	10	-1	–	1	-10	–	10	µA
I_{LO} (2)	Output Leakage Current	-10	–	10	-10	–	10	-10	–	10	-10	–	10	µA
V_{OH}	Output Logic "1" Voltage I_{OH} = -2mA	2.4	–	–	2.4	–	–	2.4	–	–	2.4	–	–	V
V_{OL}	Output Logic "0" Voltage I_{OL} = 8mA	–	–	0.4	–	–	0.4	–	–	0.4	–	–	0.4	V
I_{CC1} (3)	Active Power Supply Current	–	–	120(5)	–	–	140(5)	–	50	80	–	70	100	mA
I_{CC2} (3)	Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = V_{IH})	–	–	15	–	–	20	–	5	8	–	8	15	mA
I_{CC3} (L) (3)	Power Down Current (All Input = V_{CC} -0.2V)	–	–	500	–	–	900	–	–	500	–	–	900	µA
I_{CC3} (S) (3)	Power Down Current (All Input = V_{CC} -0.2V)	–	–	5	–	–	9	–	–	5	–	–	9	mA

DC ELECTRICAL CHARACTERISTICS – IDT72031/041

SYMBOL	PARAMETER	IDT72031 IDT72041 COMMERCIAL t_A = 35ns			IDT72031 IDT72041 MILITARY t_A = 40ns			IDT72031 IDT72041 COMMERCIAL t_A = 50, 65, 80, 120ns			IDT72031 IDT72041 MILITARY t_A = 50, 65, 80, 120ns			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
I_{LI} (1)	Input Leakage Current (Any Input)	-1	–	1	-10	–	10	-1	–	1	-10	–	10	µA
I_{LO} (2)	Output Leakage Current	-10	–	10	-10	–	10	-10	–	10	-10	–	10	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = -2mA	2.4	–	–	2.4	–	–	2.4	–	–	2.4	–	–	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 8mA	–	–	0.4	–	–	0.4	–	–	0.4	–	–	0.4	V
I_{CC1} (3)	Active Power Supply Current	–	90	140(6)	–	105	160(6)	–	75	120	–	100	150	mA
I_{CC2} (3)	Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RST}$ = $\overline{FL}/\overline{RT}$ = V_{IH})	–	8	12	–	12	25	–	8	12	–	12	25	mA
I_{CC3} (L) (3, 4)	Power Down Current (All Input = V_{CC} -0.2V)	–	–	2	–	–	4	–	–	2	–	–	4	mA
I_{CC3} (S) (3, 4)	Power Down Current (All Input = V_{CC} -0.2V)	–	–	8	–	–	12	–	–	8	–	–	12	mA

NOTES:

1. Measurements with $0.4 \le V_{IN} \le V_{CC}$.
2. $\overline{R} \ge V_{IH}$, $0.4 \le V_{OUT} \le V_{CC}$.
3. I_{CC} measurements are made with $\overline{OE}$ = HIGH.
4. (L) - Low Power, (S) - Standard Power
5. Tested at f = 20 MHz.
6. Tested at f = 15.3 MHz.

AC ELECTRICAL CHARACTERISTICS – IDT72021[1]

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	COM'L.		MIL.		COM'L.		MIL.		MILITARY AND COMMERCIAL								UNIT
		72021x25		72021x30		72021x35		72021x40		72021x50		72021x65		72021x80		72021x120		
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
f_S	Shift Frequency	–	28.5	–	25	–	22.2	–	20	–	15	–	12.5	–	10	–	7	MHz
t_{RC}	$\overline{R}$ Cycle Time	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_A	Access Time	–	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	ns
t_{RR}	$\overline{R}$ Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{RPW}	$\overline{R}$ Pulse Width[2]	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RLZ}	$\overline{R}$ Pulse Low to Data Bus at Low Z[3]	5	–	5	–	5	–	5	–	10	–	10	–	10	–	10	–	ns
t_{WLZ}	$\overline{W}$ Pulse High to Data Bus at Low Z[3, 4]	5	–	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{DV}	Data Valid from $\overline{R}$ Pulse High	5	–	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{RHZ}	$\overline{R}$ Pulse High to Data Bus at High Z[3]	–	18	–	20	–	20	–	25	–	30	–	30	–	30	–	35	ns
t_{WC}	$\overline{W}$ Cycle Time	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{WPW}	$\overline{W}$ Pulse Width[2]	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{WR}	$\overline{W}$ Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{DS}	Data Set-up Time	15	–	18	–	18	–	20	–	30	–	30	–	40	–	40	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	5	–	10	–	10	–	10	–	ns
t_{RSC}	$\overline{RS}$ Cycle Time	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{RS}	$\overline{RS}$ Pulse Width[2]	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RSS}	$\overline{RS}$ Set-up Time	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RSR}	$\overline{RS}$ Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{RTC}	$\overline{RT}$ Cycle Time	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{RT}	$\overline{RT}$ Pulse Width[2]	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RTR}	$\overline{RT}$ Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{RSF1}	$\overline{RS}$ to $\overline{EF}$ and $\overline{AEF}$ Low	–	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{RSF2}	$\overline{RS}$ to $\overline{HF}$ and $\overline{FF}$ High	–	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{REF}	$\overline{R}$ Low to $\overline{EF}$ Low	–	25	–	30	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{RFF}	$\overline{R}$ High to $\overline{FF}$ High	–	25	–	30	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{RPE}	$\overline{R}$ Pulse Width After $\overline{EF}$ High	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{WEF}	$\overline{W}$ High to $\overline{EF}$ High	–	25	–	30	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{WFF}	$\overline{W}$ Low to $\overline{FF}$ Low	–	25	–	30	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{WHF}	$\overline{W}$ Low to $\overline{HF}$ Low	–	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{RHF}	$\overline{R}$ High to $\overline{HF}$ High	–	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{WPF}	$\overline{W}$ Pulse Width after $\overline{FF}$ High	25	–	30	–	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RF}	$\overline{R}$ High to Transitioning $\overline{AEF}$	–	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{WF}	$\overline{W}$ Low to Transitioning $\overline{AEF}$	–	35	–	40	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{OEHZ}	$\overline{OE}$ High to High-Z (Disable)[3]	0	12	0	15	0	17	0	20	0	25	0	30	0	30	0	30	ns
t_{OELZ}	$\overline{OE}$ Low to Low-Z (Enable)[3]	0	12	0	15	0	17	0	20	0	25	0	30	0	30	0	30	ns
t_{AOE}	$\overline{OE}$ Low to Data Valid (Q0-8)	–	15	–	18	–	20	–	25	–	30	–	40	–	40	–	40	ns

NOTES:

1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read data flow-through mode.

AC ELECTRICAL CHARACTERISTICS – IDT72031/041[1]

(Commercial: V_{CC} = 5V ±10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ±10%, T_A = -55°C to +125°C)

SYMBOL	PARAMETER	72031x35 72041x35 MIN.	72031x35 72041x35 MAX.	72031x40 72041x40 MIN.	72031x40 72041x40 MAX.	72031x50 72041x50 MIN.	72031x50 72041x50 MAX.	72031x65 72041x65 MIN.	72031x65 72041x65 MAX.	72031x80 72041x80 MIN.	72031x80 72041x80 MAX.	72031x120 72041x120 MIN.	72031x120 72041x120 MAX.	UNIT
f_s	Shift Frequency	–	22.2	–	20	–	15	–	12.5	–	10	–	7	MHz
t_{RC}	$\overline{R}$ Cycle Time	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_A	Access Time	–	35	–	40	–	50	–	65	–	80	–	120	ns
t_{RR}	$\overline{R}$ Recovery Time	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{RPW}	$\overline{R}$ Pulse Width[2]	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RLZ}	$\overline{R}$ Pulse Low to Data Bus at Low Z[3]	5	–	5	–	10	–	10	–	10	–	10	–	ns
t_{WLZ}	$\overline{W}$ Pulse High to Data Bus at Low Z[3, 4]	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{DV}	Data Valid from $\overline{R}$ Pulse High	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{RHZ}	$\overline{R}$ Pulse High to Data Bus at High Z[3]		20	–	25		30		30		30	–	35	ns
t_{WC}	$\overline{W}$ Cycle Time	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{WPW}	$\overline{W}$ Pulse Width[2]	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{WR}	$\overline{W}$ Recovery Time	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{DS}	Data Set-up Time	18	–	20	–	30	–	30	–	40	–	40	–	ns
t_{DH}	Data Hold Time	0	–	0	–	5	–	10	–	10	–	10	–	ns
t_{RSC}	$\overline{RS}$ Cycle Time	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{RS}	$\overline{RS}$ Pulse Width[2]	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RSS}	$\overline{RS}$ Set-up Time	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RSR}	$\overline{RS}$ Recovery Time	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{RTC}	$\overline{RT}$ Cycle Time	45	–	50	–	65	–	80	–	100	–	140	–	ns
t_{RT}	$\overline{RT}$ Pulse Width[2]	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RTR}	$\overline{RT}$ Recovery Time	10	–	10	–	15	–	15	–	20	–	20	–	ns
t_{RSF1}	$\overline{RS}$ to $\overline{EF}$ and $\overline{AEF}$ Low	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{RSF2}	$\overline{RS}$ to $\overline{HF}$ and $\overline{FF}$ High	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{REF}	$\overline{R}$ Low to $\overline{EF}$ Low	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{RFF}	$\overline{R}$ High to $\overline{FF}$ High	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{RPE}	$\overline{R}$ Pulse Width after $\overline{EF}$ High	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{WEF}	$\overline{W}$ High to $\overline{EF}$ High	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{WFF}	$\overline{W}$ Low to $\overline{FF}$ Low	–	30	–	35	–	45	–	60	–	60	–	60	ns
t_{WHF}	$\overline{W}$ Low to $\overline{HF}$ Low	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{RHF}	$\overline{R}$ High to $\overline{HF}$ High	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{WPF}	$\overline{W}$ Pulse Width after $\overline{FF}$ High	35	–	40	–	50	–	65	–	80	–	120	–	ns
t_{RF}	$\overline{R}$ High to Transitioning $\overline{AEF}$	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{WF}	$\overline{W}$ Low to Transitioning $\overline{AEF}$	–	45	–	50	–	65	–	80	–	100	–	140	ns
t_{OEHZ}	$\overline{OE}$ High to High-Z (Disable)[3]	0	17	0	20	0	25	0	30	0	30	0	30	ns
t_{OELZ}	$\overline{OE}$ Low to Low-Z (Enable)[3]	0	17	0	20	0	25	0	30	0	30	0	30	ns
t_{AOE}	$\overline{OE}$ Low to Data Valid (Q0–8)	–	20	–	25	–	30	–	40	–	40	–	40	ns

NOTES:

1. Timings referenced as in AC Test Conditions.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design, not currently tested.
4. Only applies to read dataflow-through mode.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

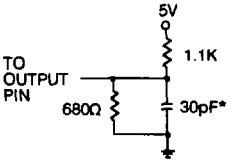


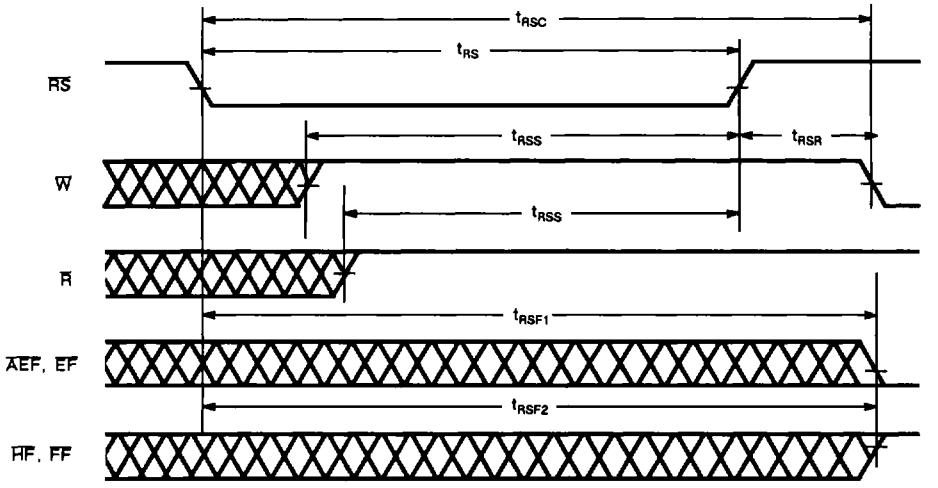
Figure 1. Output Load

*Includes scope and jig capacitances.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	10	pF

NOTE:
1. These parameters are sampled and not 100% tested.



NOTES:
1. $\overline{EF}$, $\overline{FF}$, $\overline{HF}$, and $\overline{AEF}$ may change status during Reset, but flags will be valid at t_{RSC}.
2. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of $\overline{RS}$.

Figure 2. Reset

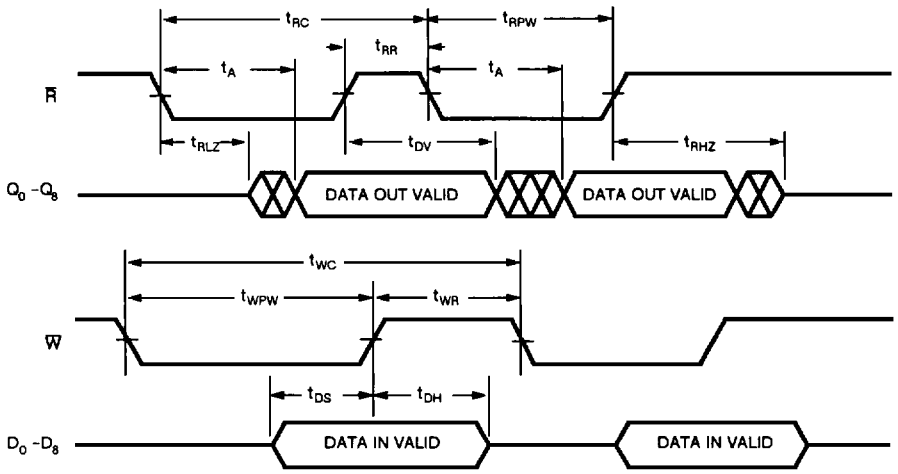


Figure 3. Asynchronous Write and Read Operation

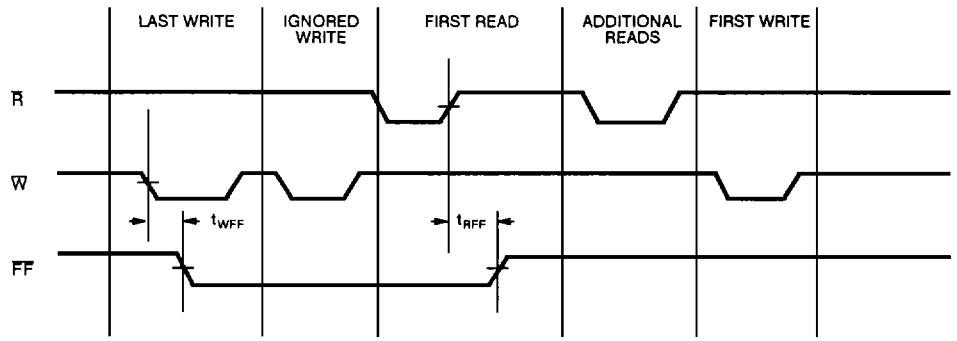


Figure 4. Full Flag From Last Write to First Read

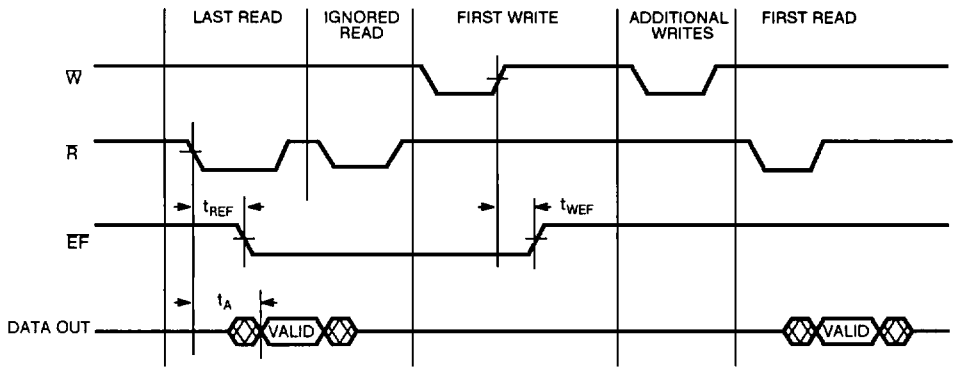
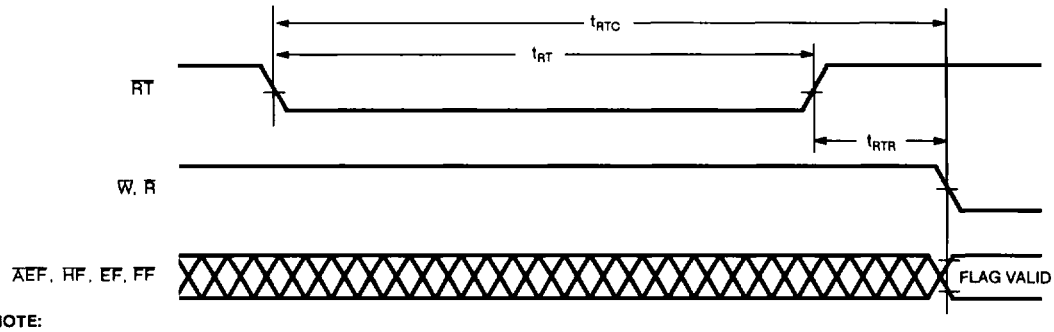


Figure 5. Empty Flag From Last Read to First Write



NOTE:
1. $\overline{EF}$, $\overline{FF}$, $\overline{HF}$, and $\overline{AEF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

Figure 6. Retransmit

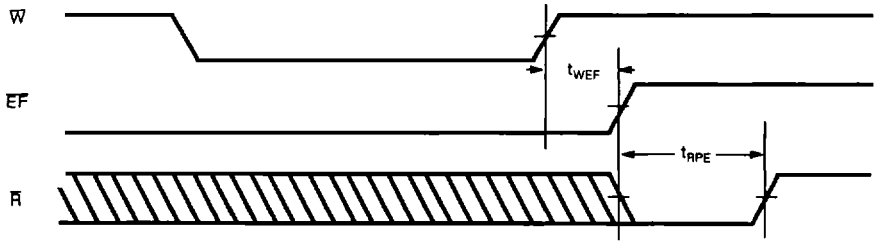


Figure 7. Empty Flag Timing

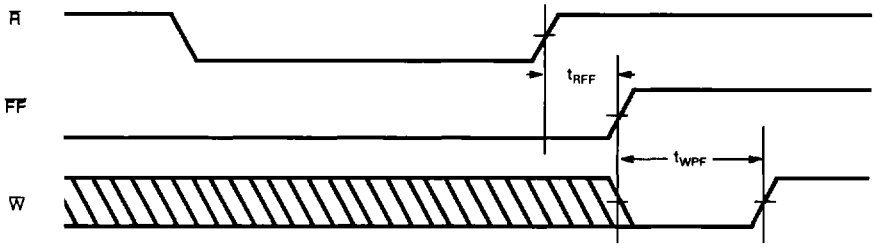


Figure 8. Full Flag Timing

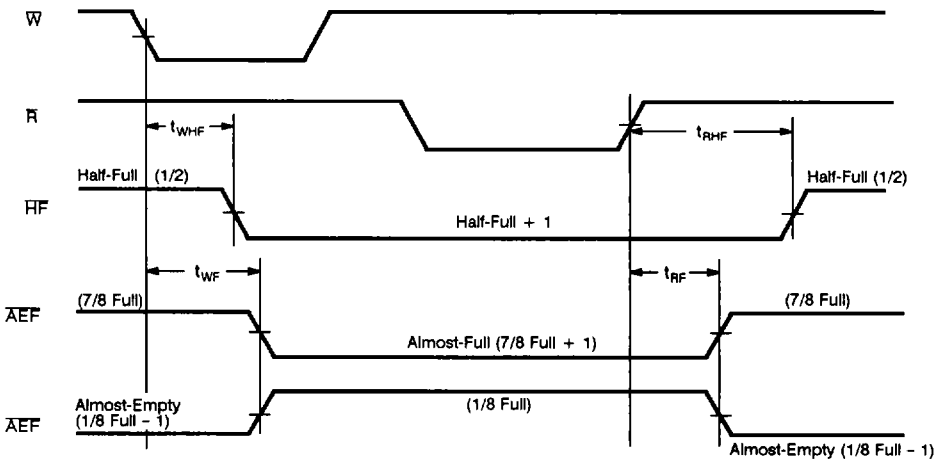


Figure 9. Almost-Empty/Almost-Full Flag and Half-Full Timings

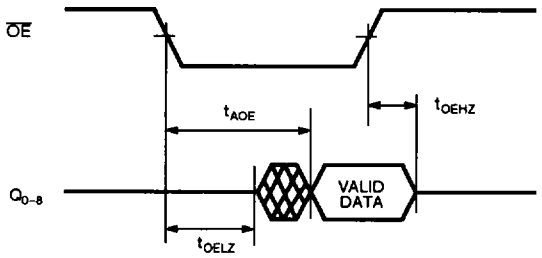


Figure 10. Output Enable Timings

OPERATING CONFIGURATIONS

SINGLE DEVICE CONFIGURATIION

The IDT72021/031/041 is in the Single Device Configuration when the Expansion in ($\overline{XI}$) control input is grounded (see Figure 11). In this mode, the Half-Full Flag ($\overline{HF}$), which is an active low output, is shared with Expansion Out ($\overline{XO}$).

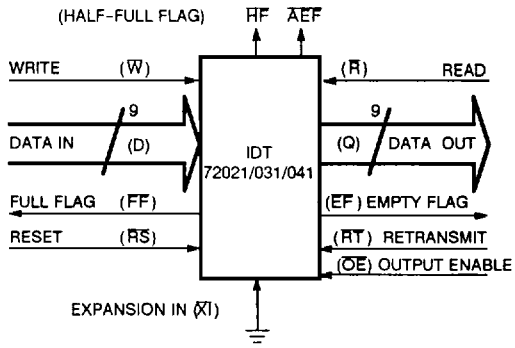
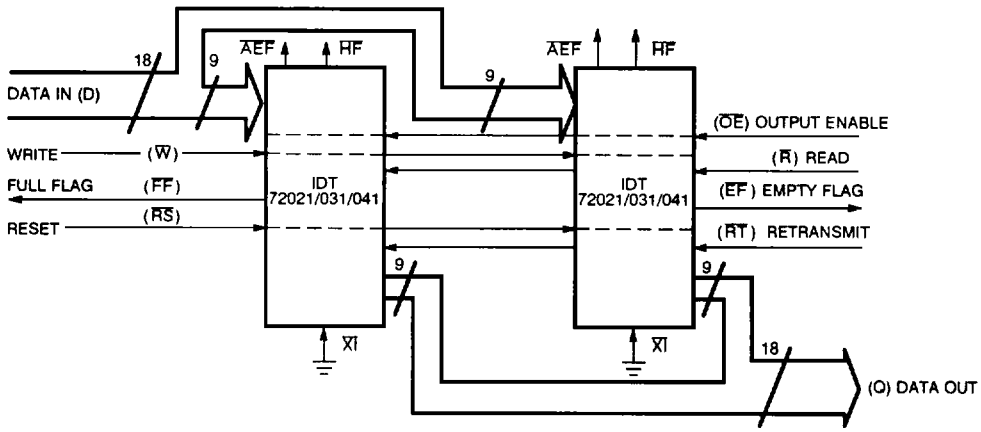


Figure 11. Block Diagram of Single 1K/2K/4K x 9 FIFO

WIDTH EXPANSION CONFIGURATION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{FF}$, $\overline{HF}$, and $\overline{AEF}$) can be detected from any one device. Figure 12 demonstrates an 18-bit word width by using two IDT72021/031/041 devices. Any word width can be attained by adding additional IDT72021/031/041s.



NOTE:
Flag detection is accomplished by monitoring the $\overline{FF}$, $\overline{EF}$, $\overline{HF}$ and $\overline{AEF}$ signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Figure 12. Block Diagram of 1K/2K/4K x 18 FIFO Memory Used in Width Expansion Configuration

DEPTH EXPANSION (DAISY CHAIN) MODE

The IDT72021/031/041 can easily be adapted to applications when the requirements are for greater than 1K/2K/4K words. Figure 13 demonstrates Depth Expansion using three IDT72021/031/041s. Any depth can be attained by adding additional devices. The IDT72021/031/041 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device. See Figure 13.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the ORing of all $\overline{EF}$s and ORing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). See Figure 13.
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion Mode.

For additional information, refer to Tech Note 9: "Cascading FIFOs or FIFO Modules".

COMPOUND EXPANSION MODE

The two expansion techniques described above can be applied together in a straightforward manner to achieve large FIFO arrays (see Figure 14).

BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT72021/031/041s as shown in Figure 15. Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH MODES

Two types of flow-through modes are permitted: a read flow-through and write flow-through mode. For the read flow-through mode (Figure 16), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in ($t_{WEF} + t_A$) ns after the rising edge of $\overline{W}$, called the first write edge. It remains on the bus until the $\overline{R}$ line is raised from low-to-high, after which the bus would go into a three-state mode after t_{RHZ} ns. The $\overline{EF}$ line would have a pulse showing temporary deassertion and then would be asserted. In the interval of time that $\overline{R}$ was low, more words can be written to the FIFO (the subsequent writes after the first write edge will deassert the empty flag); however, the same word (written on the first write edge), presented to the output bus as the read pointer, would not be incremented when $\overline{R}$ is low. On toggling $\overline{R}$, the other words that were written to the FIFO will appear on the output bus as in the read cycle timings.

In the write flow-through mode (Figure 17), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The $\overline{R}$ line causes the $\overline{FF}$ to be deasserted, but the $\overline{W}$ line being low causes it to be asserted again in anticipation of a new data word. On the rising edge of $\overline{W}$, the new word is loaded in the FIFO. The $\overline{W}$ line must be toggled when $\overline{FF}$ is not asserted to write new data in the FIFO and to increment the write pointer.

For additional information, refer to Tech Note 8: "Operating FIFOs on Full and Empty Boundary Conditions" and Tech Note 6: "Designing with FIFOs".

6

TRUTH TABLES

TABLE I – RESET AND RETRANSMIT

SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS			
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$	$\overline{AEF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1	0
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X	X
Read/Write	1	1	0	Increment (1)	Increment (1)	X	X	X	X

NOTE:
1. Pointer will increment if flag is high.

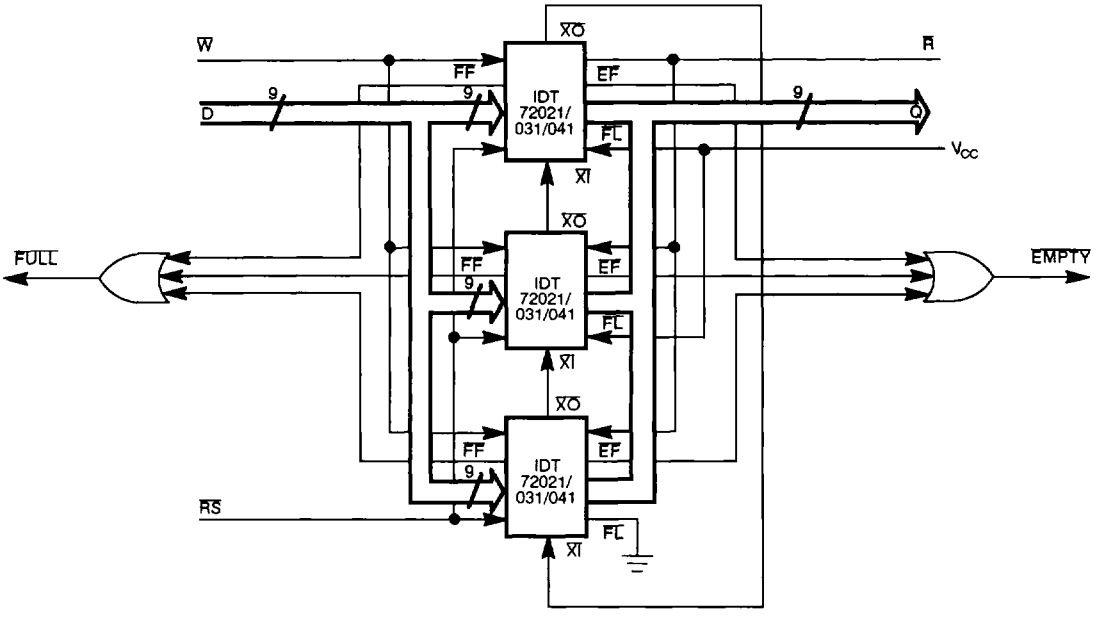
TABLE II – RESET AND FIRST LOAD TRUTH TABLE

DEPTH EXPANSION/COMPOUND EXPANSION MODE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

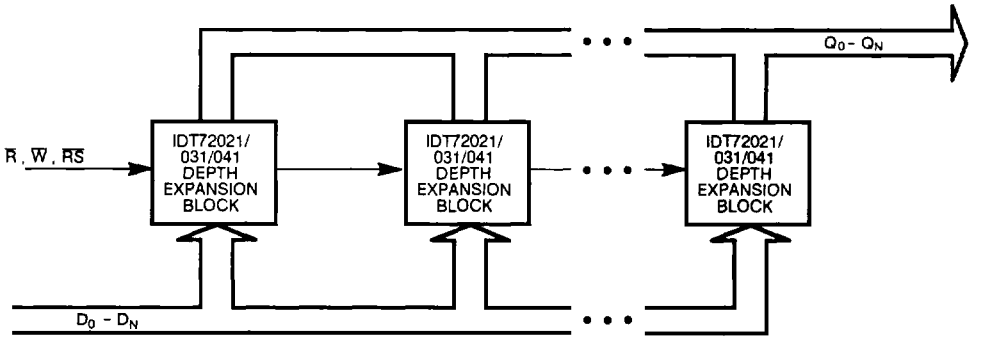
NOTE:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 13.

$\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Output, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input, $\overline{HF}$ = Half-Full Flag Output; $\overline{AEF}$ = Almost Empty/Almost Full Flag.



NOTE:
1. IDT only guarantees depth expansion with identical IDT part numbers and speed.

Figure 13. Block Diagram of 3K/6K/12K x 9 FIFO Memory (Depth Expansion)



NOTES:
1. For depth expansion block see section on Depth Expansion and Figure 13.
2. For Flag detection see section on Width Expansion and Figure 12.

Figure 14. Compound FIFO Expansion

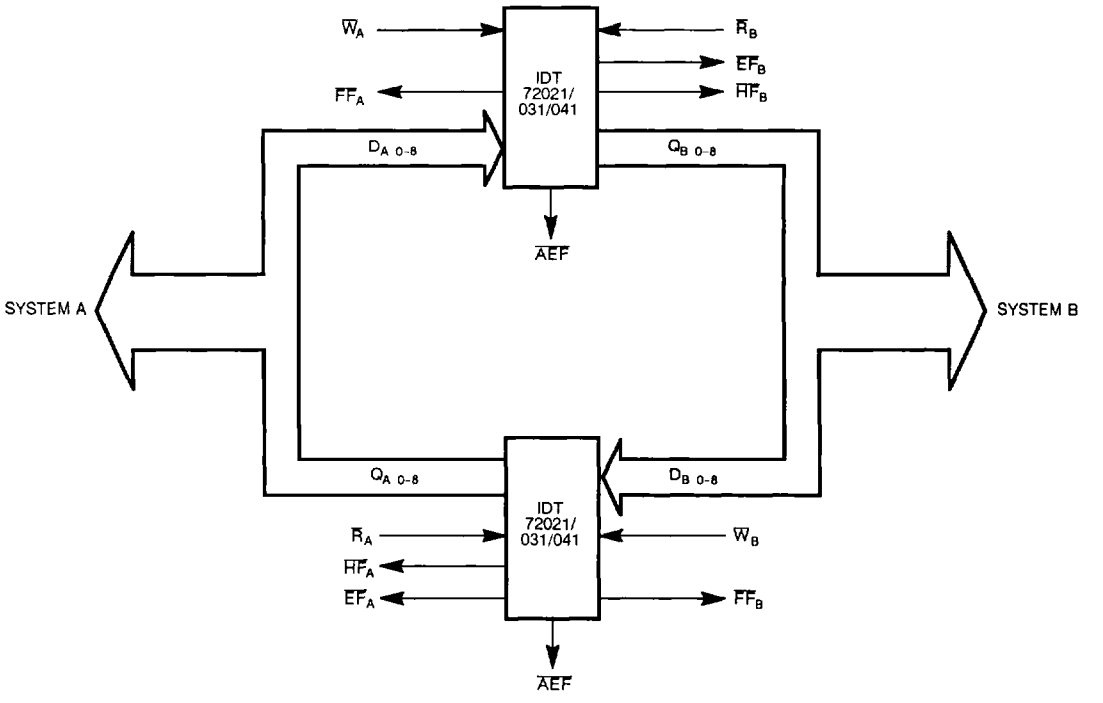


Figure 15. Bidirectional FIFO Mode

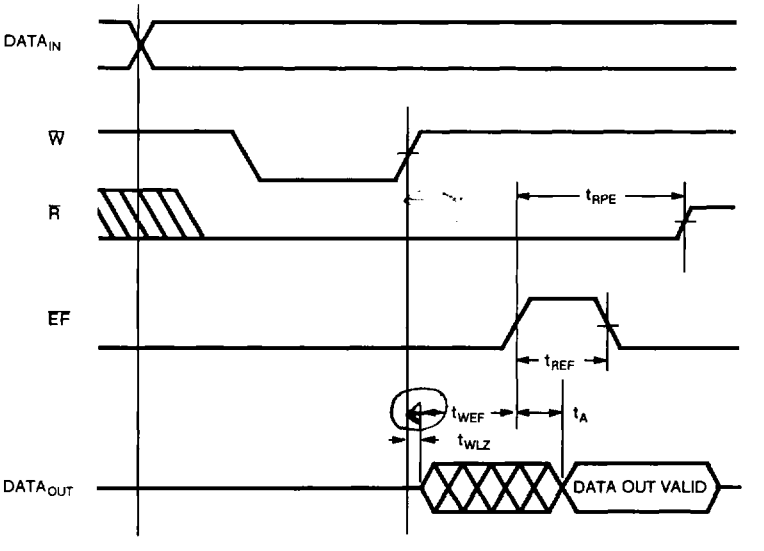


Figure 16. Read Data Flow-Through Mode

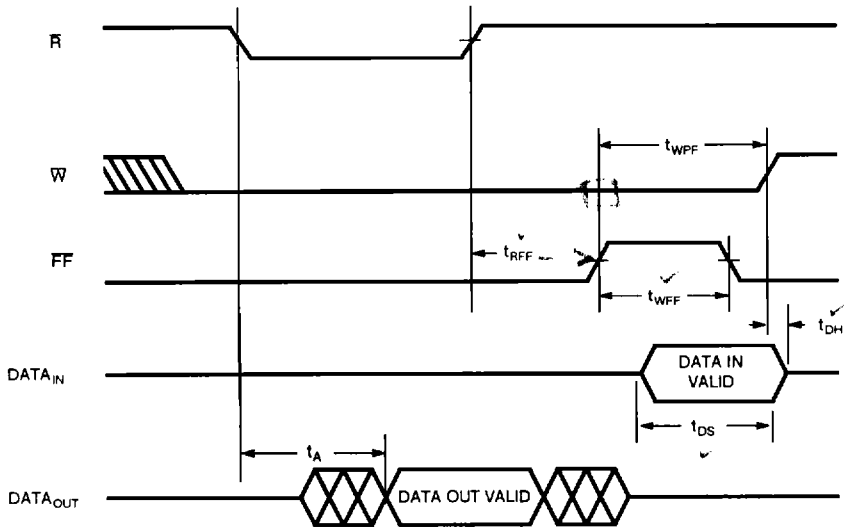


Figure 17. Write Data Flow-Through Mode

ORDERING INFORMATION