INTERSIL

2147
4096 Bit (4096 x 1) HMOS Static RAM

FEATURES

- **High speed-55ns maximum access time (2147-3)**
- **Low power — 880mW maximum active power**
- **Automatic low-power standby-20mA max (2147L)**
- **Completely static-no clock required**
- **Single +5V supply**
- **TTL compatible inputs and outputs**
- **Three-state outputs**
- **HMOS process technology**
- **Industry standard 2147 pin compatible**

GENERAL DESCRIPTION

The Intersil 2147 is a low power 4096-bit static RAM organized 4096 words by 1 bit. It is an advanced version of the industry standard 2147, fabricated with Intersil's HMOS single-layer poly selective-oxidation process. Innovative design techniques result in minimum cell area and optimum circuit performance.

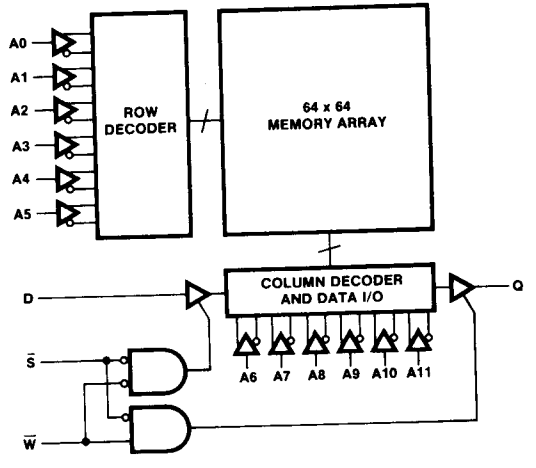
Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

An automatic low-power standby mode is controlled by chip select ($\overline{S}$); less than one cycle time after $\overline{S}$ goes high, power dissipation drops from a maximum of 160mA to 20mA (2147).

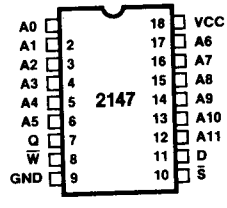
The basic device operates over the 5V ±10% range with a worst-case access time of 70ns; a "−3" device offers a worst-case access time 55ns.

The Intersil 2147 is supplied in an 18-pin package with industry standard pin configuration.

BLOCK DIAGRAM

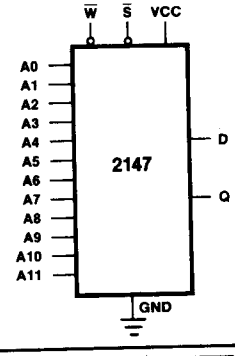


PIN CONFIGURATION



(outline drawing JN)

LOGIC SYMBOL



PIN NAMES

A0-A11	ADDRESS INPUTS
D	DATA INPUT
$\overline{Q}$	DATA OUTPUT
$\overline{S}$	CHIP SELECT
W	WRITE ENABLE

ORDERING INFORMATION

PART NO.	ACCESS TIME	ACTIVE CURRENT	STANDBY CURRENT	PACKAGE	TEMP. RANGE
D2147-3	55ns	180mA	30mA	18-pin CERDIP	0°C to +70°C
D2147L	70ns	140mA	10mA	18-pin CERDIP	0°C to +70°C
D2147	70ns	160mA	20mA	18-pin CERDIP	0°C to +70°C

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ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
V_{IN}	Voltage on any Pin Relative to GND	−1.5	+7	V	2
I_{OS}	D.C. Output Current		20	mA	
t_{STORE}	Storage Temperature	−65	+150	°C	
t_{BIAS}	Ambient Temperature Under Bias	−10	+85	°C	
P_D	Power Dissipation		1	W	

NOTES:
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions exceeding those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.
2. This device contains internal circuitry to protect against damage due to static charge. Conventional precautions should be observed, however, during storage, handling, and use to avoid exposure to excessive voltages.

ELECTRICAL CHARACTERISTICS V_{CC} = 5V ±10%, T_A = 0°C to +70°C, unless otherwise noted

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	TEST CONDITONS
V_{IH}	Input HIGH Voltage	2.0	6.0	V	
V_{IL}	Input LOW Voltage	−1.0	0.8	V	
V_{OH}	Output HIGH Voltage	2.4		V	IOH = −4.0mA
V_{OL}	Output LOW Voltage		0.4	V	IOL = 8mA
I_{IL}	Input Leakage Current		10	μA	V_{CC} = 5.5V, GND ≤ VIN ≤ VCC
I_{OLK}	Output Leakage Current		50	μA	V_{CC} = 5.5V, $\overline{S}$ = VIH, GND ≤ VO ≤ 4.5V
I_{OS}	Output Short Circuit Current	−200	200	mA	V_{OUT} = GND to V_{CC}

SYMBOL	DESCRIPTION	MAXIMUM VALUES 2147-3	2147L	2147	UNITS	NOTES
ICCOP1	Operating Supply Current	170	135	150	mA	1, 2
ICCOP2	Operating Supply Current	180	140	160	mA	1, 3
ICCSB	Standby Supply Current	30	10	20	mA	4
ICCPON	Peak Power-On Supply Current	70	30	50	mA	5

NOTES:
1. V_{CC} = 5.5V, S = V_{IL}, IO = 0mA
2. T_A = 25°C
3. T_A = 0°C
4. V_{CC} = 4.5 to 5.5V, S = V_{IH}
5. V_{CC} = GND to 4.5, $\overline{S}$ = lower of V_{CC} or V_{IH} min. A pullup resistor on $\overline{S}$ is required during power-on in order to keep the device deselected; otherwise I_{CCPON} approaches I_{CCOP}. V_{CC} slew ≥ 1V/μs.

TIMING CHARACTERISTICS V_{CC} = 5V ±10%, T_A = 0°C to +70°C, unless otherwise noted[1,4]

SYMBOL	DESCRIPTION	JEDEC SYMBOL	2147 MIN	2147 MAX	2147-3 MIN	2147-3 MAX	UNITS	TEST NOTES
	READ CYCLE							
t_{rc}	Read Cycle Time		70		55			
t_{aa}	Address Access Time	TAVQV		70		55		
t_{acs1}	Chip Select Access Time	TSLQV		70		55		2
t_{acs2}	Chip Select Access Time	TSLQV		80		65		3
t_{oh}	Output Hold from Address Change	TAXQX	5		5			
t_{lz}	Chip Selection to Output Enabled	TSLQX	10		10			
t_{hz}	Chip Deselection to Output Disabled	TSHQZ	0	40	0	40		
t_{pu}	Chip Selection to Power Up Time		0		0			
t_{pd}	Chip Deselection to Power Down Time			30		30		
	WRITE CYCLE							
t_{wc}	Write Cycle Time		70		55		ns	
t_{cw}	Chip Selection to End of Write	TSLWH	55		45			
t_{aw}	Address Valid to End of Write	TAVWH	55		45			
t_{as}	Address Setup Time	TAVWL	0		0			
t_{wp}	Write Pulse Width	TWLWH	40		35			
t_{wr}	Write Recovery Time	TWHAX	15		10			
t_{dw}	Data Valid to End of Write	TDVWH	30		25			
t_{dh}	Data Hold Time	TWHDX	10		10			
t_{wz}	Write Enabled to Output Disabled	TWLQZ	0	35	0	30		
t_{ow}	Output Active from End of Write	TWHQX	0		0			

NOTES:
1. t_r = t_f = 10ns. Input and output timing reference level = 1.5V.
2. Device deselected for 55ns or more prior to selection.
3. Device deselected for a finite time less than 55ns prior to selection.
4. Operating temperature range is guaranteed with transverse flow exceeding 400 linear feet per minute.

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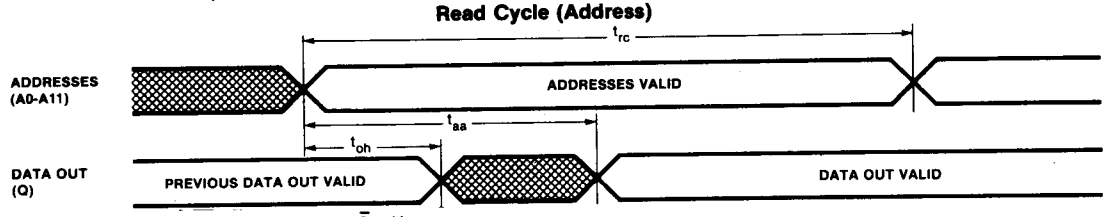
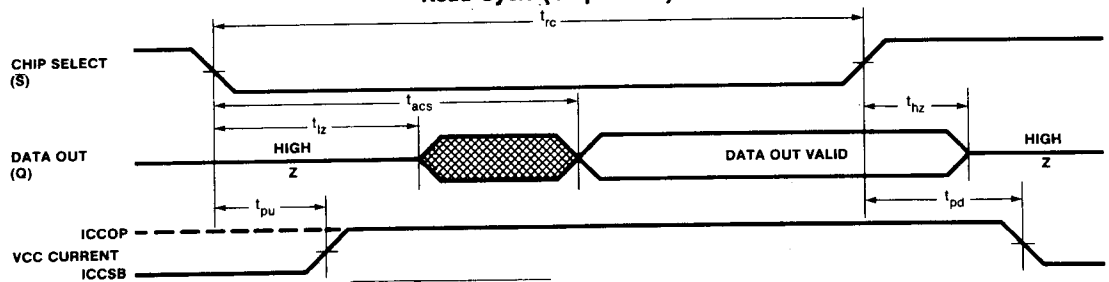
TIMING DIAGRAMS (For TEST CIRCUIT, see M2147)

Read Cycle (Address)



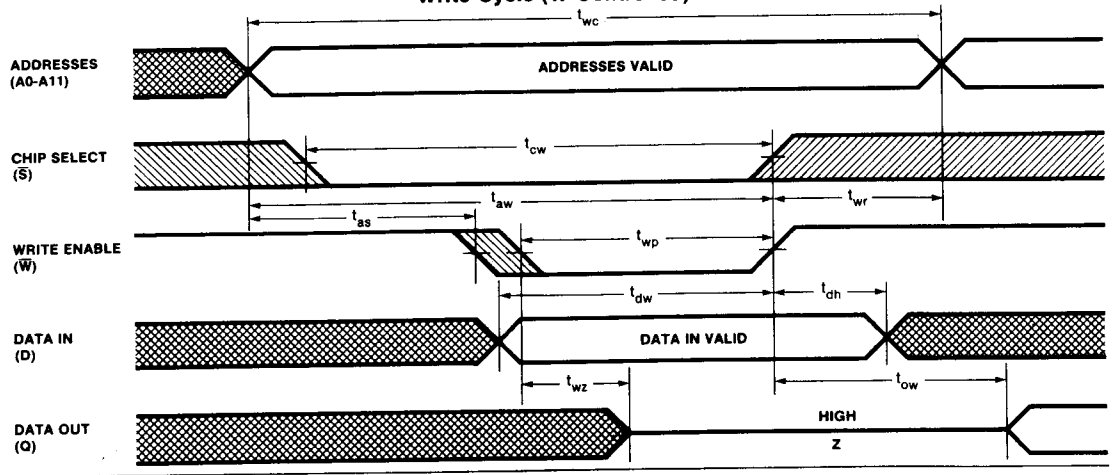
Notes: 1. Device is continuously selected, $\overline{S} = V_{IL}$.
2. Write Enable is high for read cycle, $\overline{W} = V_{IN}$.

Read Cycle (Chip Select)



Note: Address is valid prior to or coincident with $\overline{S}$ transition low.

Write Cycle (W Controlled)



Write Cycle ($\overline{S}$) Controlled