High Speed CMOS 9-bit FIFO Buffer Memories

512x9: QS8201
1Kx9: QS8202
PRELIMINARY

FEATURES/BENEFITS

- 15 ns flag and data access times
- Fully Asynchronous Read and Write
- Zero fall-through time
- Expandable in depth with no speed loss
- TTL input and output level compatible
- Military product compliant to MIL-STD-883, Class B
- 40 MHz cycle time
- Retransmit capability
- Dual Port RAM-based cell using 6T technology
- Available in 300 mil/600 mil PDIP, SOIC, SOJ, 300 mil/600 mil CERDIPs, PLCC, LCC
- Low Power with Industry standard pinouts

DESCRIPTION

The QS8201 and QS8202 are 512x9 and 1Kx9 FIFOs respectively. These FIFOs use a dual-port RAM based architecture and having independent read and write pointers. This allows high speed and zero fall-through time. The read and write pointers are incremented on the rising edges of the Read and Write lines. The flag circuitry is based on a reliable sequential design giving precise half-full, full, and empty conditions. These flags also prevent the FIFO from being written into when full or being read from when empty. These FIFOs are easily cascadable to any depth and expandable to any width. There is no speed penalty for expansion. Retransmit capability is provided. Retransmits resets the read pointer to zero, and is useful for data communications and digital filtering applications.

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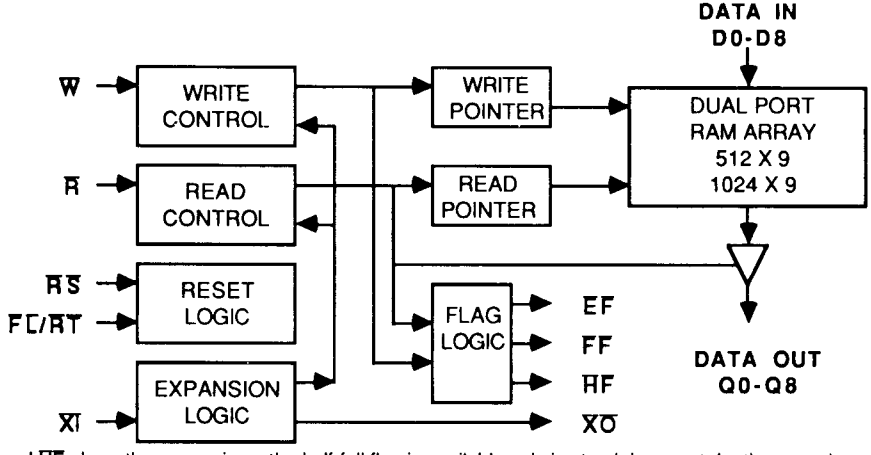
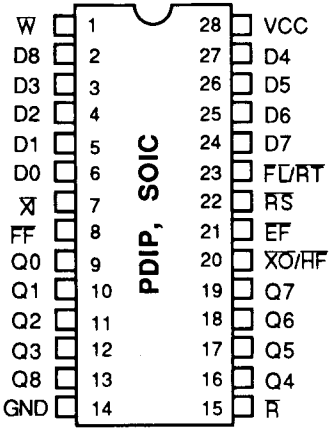
FUNCTIONAL BLOCK DIAGRAM

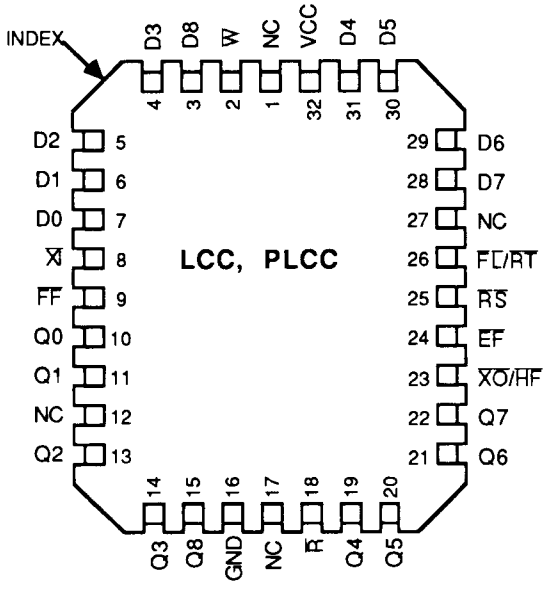


Note: $\overline{XO}$ and $\overline{HF}$ share the same pin so the half-full flag is available only in standalone, not depth expansion mode .

PINOUTS



ALL PINS TOP VIEW



PIN DESCRIPTIONS

Name	I/O	Description
Di	I	Data Inputs
Qi	O	Data Outputs
$\overline{R}$	I	Read Clock
$\overline{W}$	I	Write Clock
$\overline{EF}$	O	Empty Flag
$\overline{FF}$	O	Full Flag

Name	I/O	Description
$\overline{RS}$	I	Reset
$\overline{FL}$/$\overline{RT}$	I	First Load/Retransmit
$\overline{XI}$	I	Expansion Clock In
$\overline{XO}$/HF	I	Expansion Clock Out/ Half Full Flag

FUNCTION TABLES

RESET AND RETRANSMIT FUNCTION TABLE

Stand Alone Device or Width Expansion

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	FC/$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	EF	FF	HF
Reset	L	X	L	Location Zero	Location Zero	L	H	H
Retransmit	H	L	L	Location Zero	Unchanged	(3)	(3)	(3)
Read/Write	H	H	L	Increment (1)	Increment (2)	(4)	(4)	(4)

Notes:
(1) The Read Pointer will increment if the FIFO is not empty.
(2) The Write flag will increment if the FIFO is not full.
(3) The flags will change after the retransmit operation and will correspond to the read pointer being at location zero.
(4) The flags will reflect the relative locations of the read and write pointers.

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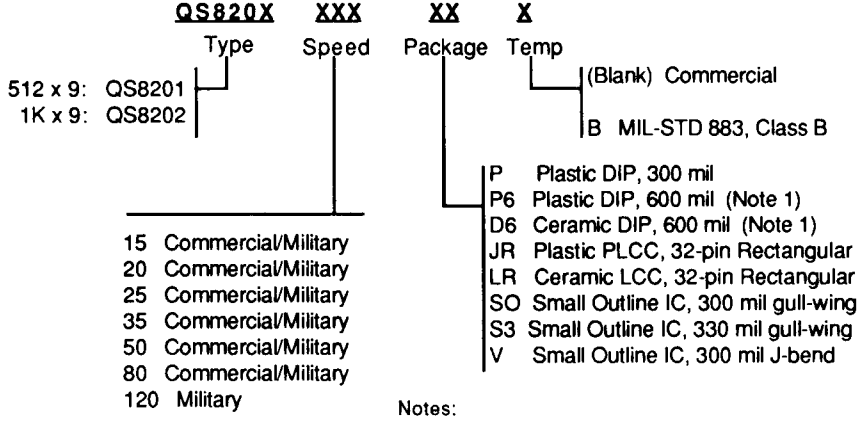
RESET AND FIRST LOAD FUNCTION TABLE

MODE	INPUTS			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	FC/$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	EF	FF	HF
Reset 1st Device	L	L	(1)	Location Zero	Location Zero	L	H	H
Reset Other Devices	H	H	(1)	Location Zero	Location Zero	(3)	(3)	(3)
Read/Write	H	(2)	(1)	Increment (1)	Increment (2)	(4)	(4)	(4)

Notes
(1) The Expansion In ($\overline{XI}$) is connected to the Expansion Out ($\overline{XO}$) of the previous device.
(2) The device with FC tied low will receive the first N writes and first N reads, where N is the FIFO size. On the Nth write, the $\overline{XO}$ pulse is sent to the next device to indicate that it will receive the (N+1)th write. Similarly on the Nth read another $\overline{XO}$ pulse is sent to the next device to indicate that it will output the (N+1) th read.
(3) The read and write pointers will be activated according to whether the FIFO received a n $\overline{XO}$ pulse, or whether they were the first device in the daisy chain. The flags will reflect the empty or full conditions for the individual FIFOs. To create the composite Full and Empty flags, an OR-ing of the individual flags is required.

ORDERING INFORMATION



Notes:
1. 600 mil DIP only available for -80 and -120 speed grades

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground.....-0.5V to +6.0V.
DC Output Voltage V_O .....-0.5V to V_{CC} + 0.5V.
DC Input Voltage V_I ..... -0.5V to V_{CC} + 0.5V.
AC Input Voltage (for pulse width≤20 ns).....-3.0 V.
DC Input Diode Current with V_I<0..... -20 mA.
DC Input Diode Current with $V_I > V_{CC}$..... 20 mA.
DC Output Diode Current with V_O <0..... -50 mA.
DC Output Diode Current with $V_O > V_{CC}$ ..... 50 mA.
DC Output Current Max. sink current/pin..... 70 mA.
DC Output Current Max. source current/pin..... 30 mA.
Total DC Ground Current..... (NxIOL +MxΔI CC) mA.
Total DC VCC Power Supply Current..... (NxIOH + MxΔI CC) mA.
N=Number of Outputs, M=Number of inputs
Maximum Power Dissipation.....0.5 watts.
TSTG Storage Temperature..... -65° to +165°C.

CAPACITANCE

Ta = 25 °C, f = 1 mHz

Name	Description	Conditions	Typ	Max	Unit
Cin	Input Capacitance	Vin = 0 V	5	8	pF
Cout	Output Capacitance	Vout = 0 V	5	8	pF

Note: Capacitance is guaranteed but not tested

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Commercial T_A=0°C to 70°C, V_{CC}=5.0V±10% Military T_A=-55°C to 125°C, V_{CC}=5.0V±10%

Symbol	Parameter	Test Conditions	Commercial		Military		Unit
			Min	Max	Min	Max	
Vih	Input HIGH Voltage	Logic High for All Inputs	2.0	6.0	2.2	6.0	Volts
Vil	Input LOW Voltage (1)	Logic Low for All Inputs		0.8		0.8	
Voh	Output HIGH Voltage	Ioh = -2 mA, Vcc = MIN	2.4		2.4		
Vol	Output LOW Voltage	Iol = 8 mA, Vcc = MIN		0.4		0.4	
|Iii|	Input Leakage	Vcc = MAX, Vin = GND to Vcc		5		10	µA
|Ilo|	Output Leakage	Vcc = MAX, Vout = GND to Vcc		10		10	

Notes: 1. Transient inputs with Vil not more negative than -1.5 volts are permitted for pulse widths ≤ 10 ns

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POWER SUPPLY CHARACTERISTICS

Commercial T_A=0°C to 70°C, V_{CC}=5.0V±10% Military T_A=-55°C to 125°C, V_{CC}=5.0V±10%
Vlc = 0.2 Volts, Vhc = Vcc - 0.2 Volts

Symbol	Parameter	≤35		≥50		Unit
		C	M	C	M	
Icc1	Operating OperatingCurrent Vcc = MAX, Outputs open	100	120	100	120	mA
Icc2	Standby Current $\overline{R} = \overline{W} = \overline{RS} = \overline{FL/RT}$ = Vih	15	20	8	15	
Isb	Power Down Current All Inputs at Vhc or Vlc $\overline{R} = \overline{W} = \overline{RS} = \overline{FL/RT}$ = Vhc	5	9	5	9	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

For 15 ns Commercial, 20, 25, 35, 50 ns Commercial/ Military, 120 ns Military
COMMERCIAL V_{CC}=5V±10%, T_A=0°C to +70°C, MILITARY V_{CC}=5V±10%, T_A=-55°C to +125°C

Symbol	Parameter (1)	Note	-15	-20	-25	-35	-50	-80	-120	Unit	Type
READ CYCLE											
f RF	Read Frequency, mHz	2	40	33	28	22	15	10	7	mHz	Min
t RC	Read Cycle Time		25	30	35	45	65	100	140	ns	
t A	Read Access Time		15	20	25	35	50	80	120		Max
t RR	Read Recovery Time		10	10	10	10	15	20	20		Min
t RPW	Read Pulse Width	1	15	20	25	35	50	80	120		
t RLZ	$\overline{R}$ Data Bus Low Z	2	3	3	3	3	3	3	3		
t WLZ	$\overline{W}$ Data Bus LowZ	2,3	3	3	3	3	3	3	3		
t DV	$\overline{R}$ high to Data Hold Time		5	5	5	5	5	5	5		
t RHZ	$\overline{R}$ to Data High Z		14	18	18	20	30	35	35		Max
WRITE CYCLE											
f WF	Write Frequency, mHz	2	40	33	28	22	15	10	7	mHz	Min
t WC	Write Cycle Time		25	30	35	45	65	100	140	ns	
t WPW	Write Pulse Width	1	15	20	25	35	50	80	120		
t WR	Write Recovery Time		10	10	10	10	15	20	20		
t DS	Write Data Setup Time		9	12	15	18	30	40	40		
t DH	Write Data Hold Time		0	0	0	0	0	0	0		
RESET AND RETRANSMIT CYCLES											
t RSC	Reset Cycle Time		25	30	35	45	65	100	140	ns	Min
t RS	Reset Pulse Width	1	15	20	25	35	50	80	120		
t RSS	Reset Setup Time		15	20	25	35	50	80	120		
t RSR	Reset Recovery Time		10	10	10	10	15	20	20		
t RTC	Retransmit Cycle Time		25	30	35	45	65	100	140		
t RT	Retransmit Pulse Width	1	15	20	25	35	50	80	120		
t RTS	Retransmit Setup Time	2	15	20	25	35	50	80	120		
t RTR	Retransmit Recovery		10	10	10	10	15	20	20		

Notes: These timings are measured as defined in AC Test Conditions

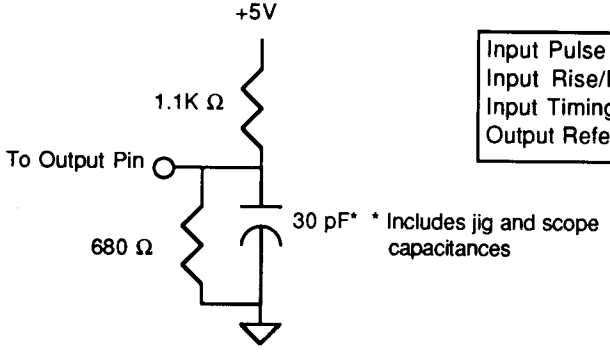
1. Pulse widths less than the specified minimum value may upset the internal pointers and are not allowed.
2. These values are guaranteed by design and not tested
3. This applies to the read data flow-through mode only.

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

For 15 ns Commercial, 20, 25, 35, 50 ns Commercial/ Military, 120 ns Military
COMMERCIAL V_{CC}=5V±10%, T_A=0°C to +70°C, MILITARY V_{CC}=5V±10%, T_A=-55°C to +125°C

Symbol	Parameter (1)	Note	-15	-20	-25	-35	-50	-80	-120	Unit	Type
FLAG TIMING											
t REF	Read Low to EF Low		15	20	25	30	45	60	60	ns	Max
t RFF	Read High to FF High		15	20	25	30	45	60	60		
t RHF	Read High to HF High		15	20	25	35	45	60	60		
t RPE	Read Pulse after EF High		15	20	25	35	50	80	120		
t WEF	Write High to EF High		15	20	25	30	45	60	60		
t WFF	Write Low to FF Low		15	20	25	30	45	60	60		
t WHF	Write Low to HF Low		15	20	25	35	45	60	60		
t WPF	Write Pulse after EF Hi		15	20	25	35	50	80	120		
t EFL	Reset to EF Low		15	20	25	35	45	60	60		
t FFH	Reset to FF High		15	20	25	35	45	60	60		
t HFH	Reset to HF High		15	20	25	35	45	60	60		
EXPANSION TIMING											
t XOL	Read/Write to XO Low		15	20	25	35	50	80	120	ns	Max
t XOH	Read/Write to XO High		15	20	25	35	50	80	120		
t XI	XI Pulse Width		15	20	25	35	50	80	120		
t XIR	XI Recovery Time		10	10	10	10	10	10	10		Min
t XIS	XI Setup Time		10	15	15	15	15	15	15		

AC TEST CONDITIONS



Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3 ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V

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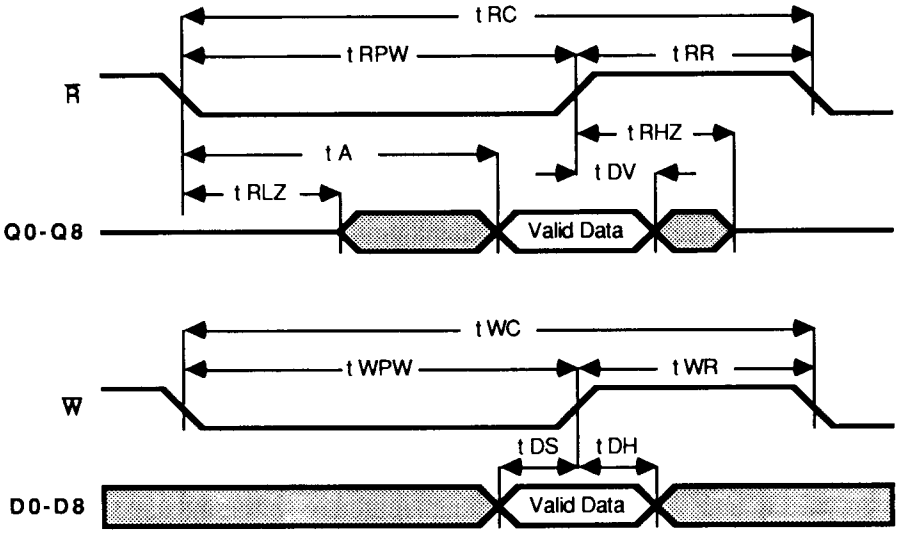
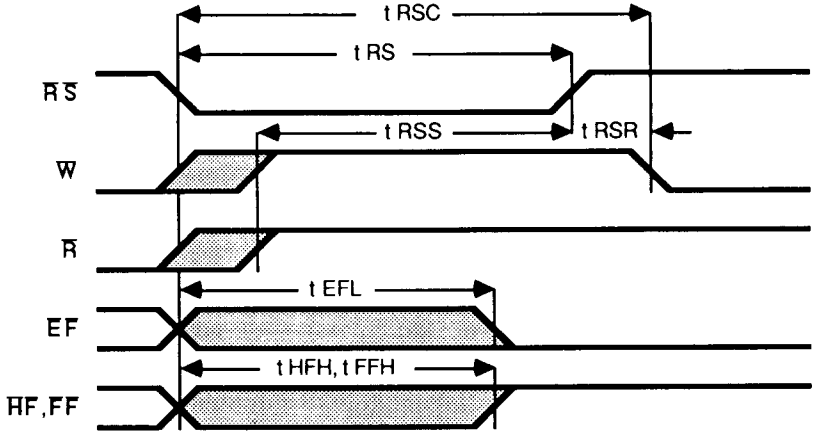
TIMING DIAGRAMS

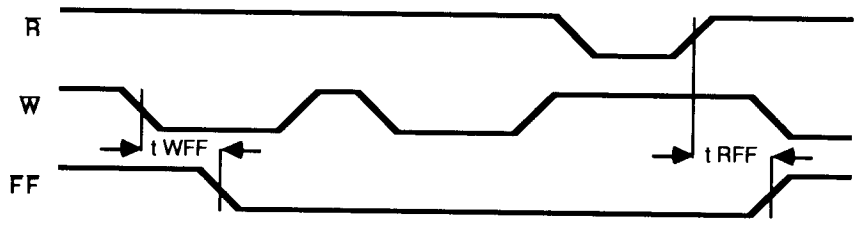


Asynchronous Read and Write Operations

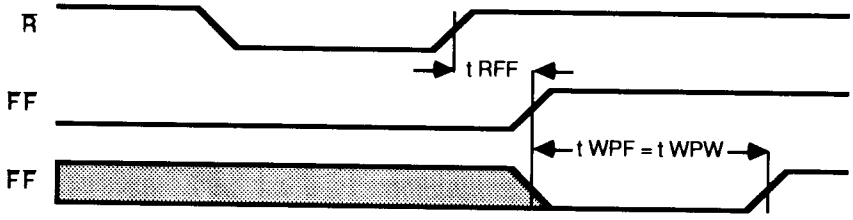


Notes: Read and Write have to be at a HIGH level around the rising edge of Reset. The flags may change during reset but are valid at t RSC.

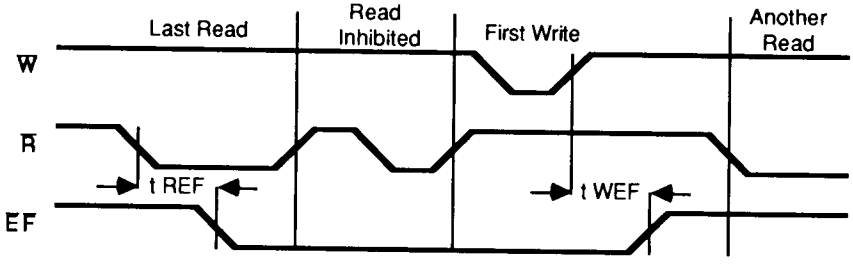
Reset Timing



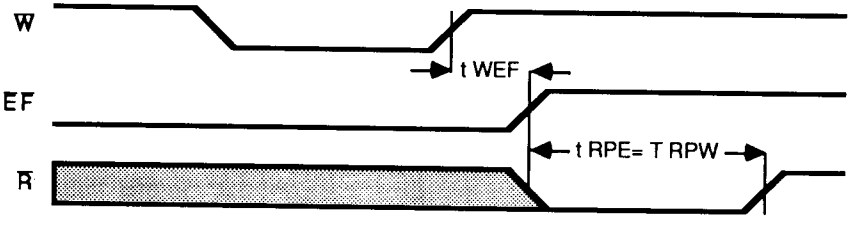
Full Flag Behavior from Last Write to First Read



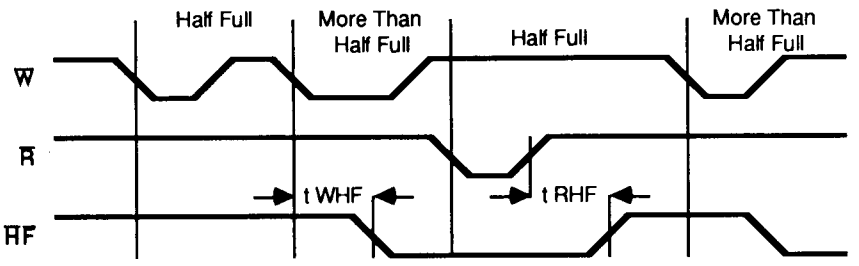
Full Flag and Required Write Pulse at Full Condition



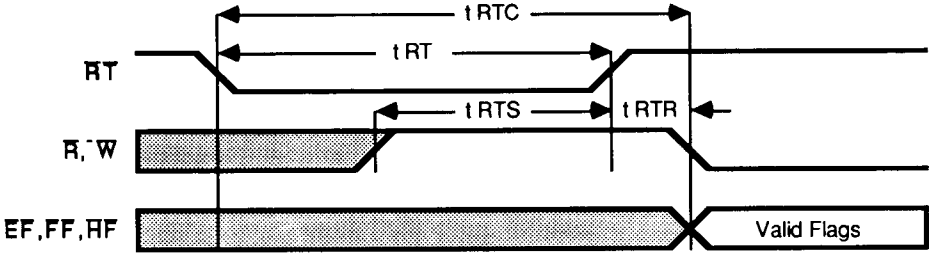
Empty Flag Behavior from Last Read to First Write



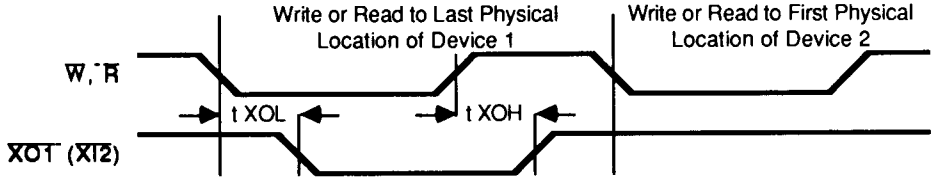
Empty Flag and Required Pulse Width at Empty Condition



Half Full Flag Timing

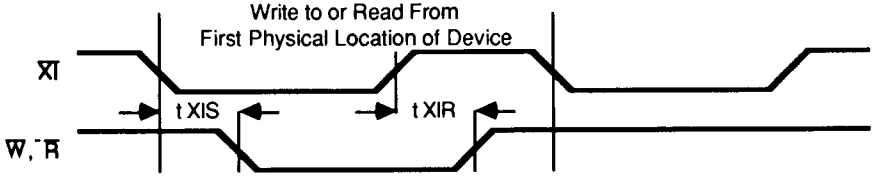


Retransmit Function Timing

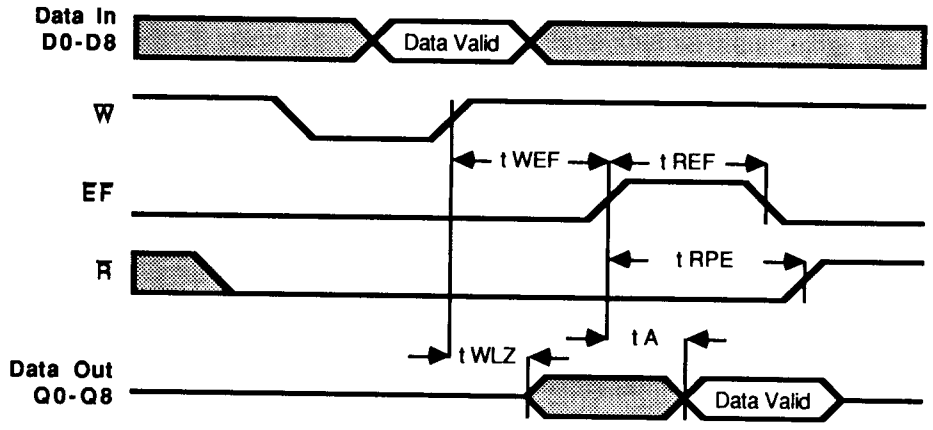


Note: the Expansion Out of Device 1 is connected to the Expansion In of device 2.

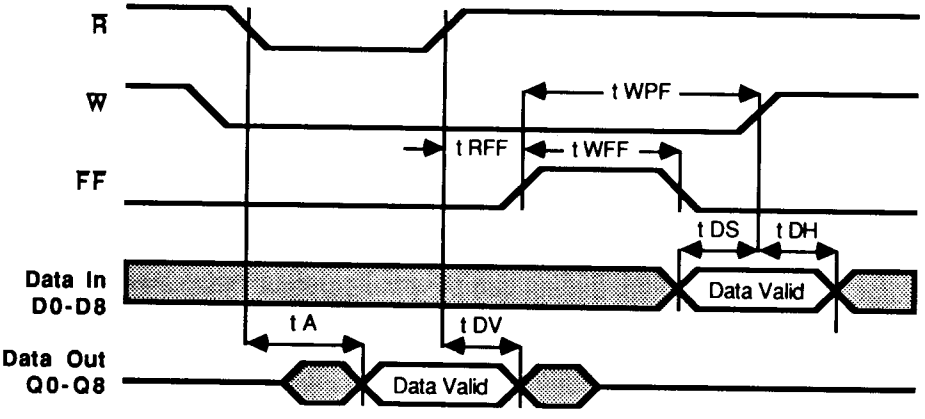
Expansion Out Timing



Expansion In Timing



Read Data Flow-Through Mode



Write Data Flow-Through Mode

OPERATIONAL DESCRIPTION AND APPLICATION INFORMATION

The QS8201 and QS8202 are 512x9 and 1Kx9 FIFOs respectively. These FIFOs use a dual-port RAM based architecture and having independent read and write pointers. This allows high speed and zero fall-through time. The Write line causes data to be written into the FIFO. The Read line causes data to be read from the FIFO. The Read line also activates the three-state outputs to present the read data. The read and write pointers are incremented on the rising edges of the Read and Write lines. The flag circuitry is based on a reliable sequential design giving precise half full, full, and empty conditions. These flags also prevent the FIFO from being written into when full or being read from when empty. Depth expansion pins are provided which allow these FIFOs to be expanded in depth without speed penalty. Retransmit capability is provided. Activating the Retransmit pin resets the read pointer to zero, and is useful for data communications and digital filtering applications.

SIGNAL DESCRIPTION

DATA INPUTS

D_0-D_8
The Data In lines D_0 to D_8 provide data to be written into the FIFO. Note: unused inputs must be tied to Vcc or Gnd.

CONTROL INPUTS

Reset ($\overline{RS}$)
The Reset input resets the Read and Write pointers and the flags to zero. The FIFO must be reset at power-up to insure proper operation of the pointers and flags. This is done by asserting the Reset line to a LOW state, which causes the FIFO flags to be set to empty. This causes the Empty flag is asserted and the Full and Half Full flags to be deasserted. Read and Write lines must be HIGH for t RSS before and t RSR after the rising edge of the Reset signal for a valid reset operation.

Write ($\overline{W}$)
The Write line caused data to be written into the FIFO. A write cycle is initiated by the falling edge of the Write signal. A write will occur if the full flag was not asserted, indicative of at least one empty location in the FIFO. Data is stored in the FIFO on the rising edge of the Write signal using the data set-up and hold times specified. Data is stored in a sequential manner in the FIFO, and the read and write operations can be asynchronous. The falling edge of the Write signal asserts the Half full and Full flags when the next word after half full is written and when the last word has been written, respectively. The rising edge of the Write line deasserts the empty flag when the first write is performed after an empty or reset condition. When the Full flag is asserted, subsequent writes are blocked. The user can apply a write pulse after the full condition is deasserted.

Read ($\overline{R}$)
The Read signal causes data to be read from the FIFO. A read cycle is initiated by the falling edge of the Read signal. A read is performed if the empty flag is not asserted, indicative of at least one word being present in the FIFO. The data is accessed in a First-In-First-Out basis asynchronous to the Write operations. After the Read control is deasserted the data outputs go from a valid state into high-impedance. The outputs remain in high-impedance until the next read cycle. When all the data is read on the last read cycle, the Empty flag is asserted, and will inhibit any subsequent reads. The outputs will be in high-impedance for subsequent read operation until a write occurs that deasserts the Empty flag, allowing a read cycle to begin. The outputs may also be in high impedance when the FIFOs are

cascaded in depth. In this case, only the active FIFO asserts data , and the other FIFOs data outputs are in high-impedance. The falling edge of the read signal will set the Empty Flag during the read of the last word in the FIFO. The rising edge of the Read signal will deassert the Half Full and the Full flags when the FIFO has reached half full and when the FIFO was full, respectively.

First Load/ Retransmit ($\overline{FL}/\overline{RT}$)
This is a dual purpose input. In the depth expansion mode, this pin indicates the first FIFO device that will be loaded or read from after a reset operation. In the standalone or width expansion mode (when the the expansion input is grounded) this pin initiates the a retransmit function.

Retransmit resets the read pointer to zero. The Read and Write signals must be HIGH before and after the rising edge of the retransmit pulse. The retransmit feature is useful when the same data needs to be read again without rewriting it into the FIFO. Pulsing retransmit pin will cause the read pointer to be reset to zero and the previously read data can be read again. The flags will change according to the relative location of the pointers after the retransmit pulse.

Expansion In ($\overline{XI}$)
This is a dual purpose pin. When it is grounded then it indicates that the FIFO is a standalone device. When it is not grounded, it indicates that the FIFO is in the depth expansion mode. In the depth expansion mode this pin is connected to the $\overline{XO}$ pin of the previous device.

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DATA OUTPUTS

Data Outputs Q_0-Q_8
The 9-bit data output bus, Q_0-Q_8 receives the read data from the FIFO. It is active whenever the Read signal is low. It is in a high impedance state when the Read signal is high. It is also in high impedance when the FIFO Empty flag is active (i.e., when the FIFO is empty).

CONTROL OUTPUTS

Full Flag ($\overline{FF}$)
The Full Flag indicates that the FIFO is full. The Full Flag is asserted when there is only one empty location in the FIFO and a falling edge of the Write signal initiates the last write operation. The rising edge of the Read signal deasserts the flag, as at least one location has become available.

Empty Flag ($\overline{EF}$)
The Empty Flag indicates the FIFO is empty. It is asserted when there is only one word in the FIFO, and a falling edge of the Read signal initiates the last read operation. The rising edge of the write signal deasserts the flag, as one word is now present in the FIFO.

Expansion Out/Half Full flag ($\overline{XO}/\overline{HF}$)
This is a dual purpose flag. In the single device mode, the Expansion In is grounded and the Half Full flag output is present on this pin. Whenever the FIFO is more than half full the flag remains asserted . When the FIFO is exactly half full and the next falling edge of the Write signal asserts the flag. The rising edge of read that causes the FIFO to be half full, will deassert the half full flag. It will remain asserted until the FIFO is half full or less than half full. The name given to the flag is half full, but it is asserted on the one plus the half full condition.

In the depth expansion mode, the Expansion Out is connected to the Expansion In of the next device. This causes the next device to perform write or read operations.

OPERATING MODES

SINGLE DEVICE MODE

A FIFO is in standalone mode when the Expansion In control is grounded. In this mode the half full flag is available on the shared $\overline{XO}/\overline{HF}$ line. Figure 1 shows the standalone mode and this applies to FIFO width expansion, as shown in figure 2.

DEPTH EXPANSION MODE

A FIFO is in the depth expansion mode when the Expansion In control is not grounded but tied to the Expansion Out pin of the previous FIFO. Using the depth expansion mode, the 8201/02 can be easily cascaded to create FIFOs of larger depth. The devices are cascaded as shown in figure 3. In the depth expansion mode, the device that receives the first word of data has its First Load input grounded. The other devices have their First Load inputs in the high state. Two 4-input OR gates are required to create the composite Full and Empty flags for the FIFO array. In using the depth expansion mode, care must be taken to keep the traces short between the Expansion In of one device to the Expansion Out of the next device to minimize crosstalk noise.

FLOW-THROUGH MODES

Flow-through modes refer to the internal operation of the FIFO in empty and full conditions. Flow through modes allow data to flow directly through the FIFO from input to output under the appropriate empty and full conditions.

Two types of flow-through modes, a read flow-through and a write flow-through, are supported by the FIFO. In the read flow-through mode the FIFO is empty, and the read side is waiting for data from a write. Read flow-through is represented by an empty FIFO that has its Read line held low, and a write occurs. This rising edge of the Write would deassert the Empty flag and cause valid data to appear on the outputs after a certain time delay of $t_{WEF} + t_A$. The Read line being low would cause the data to be read and also assert the empty flag once again. The user must raise the Read line in order to increment the read pointer.

In the write flow-through mode, the FIFO is full and the write side is waiting for a word location to be made available by a read. A write flow-through operation permits the writing of a single word of data immediately after reading one word of of data from a full FIFO. This is similar to the read flow-through case, and the Write line must toggled to increment the write pointer.

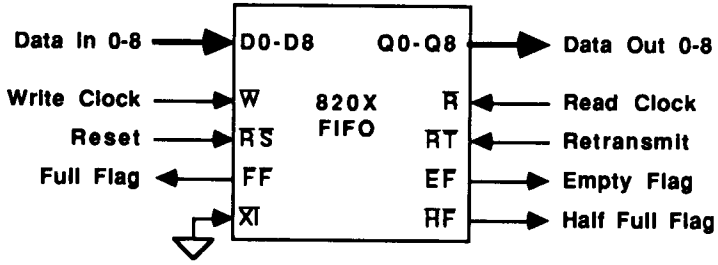

Figure 1. The FIFO in Standalone Mode.

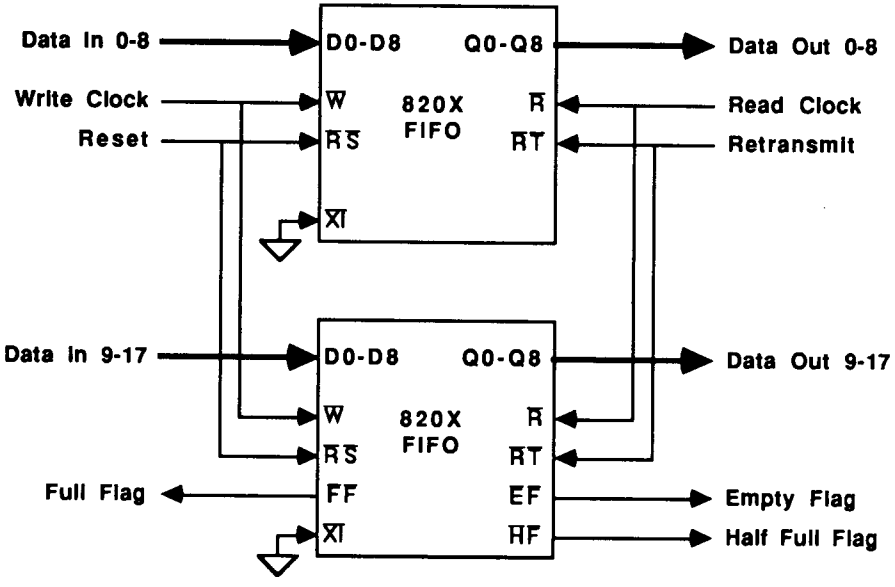

Figure 2. A 18-bit Wide FIFO Using 2 FIFOs

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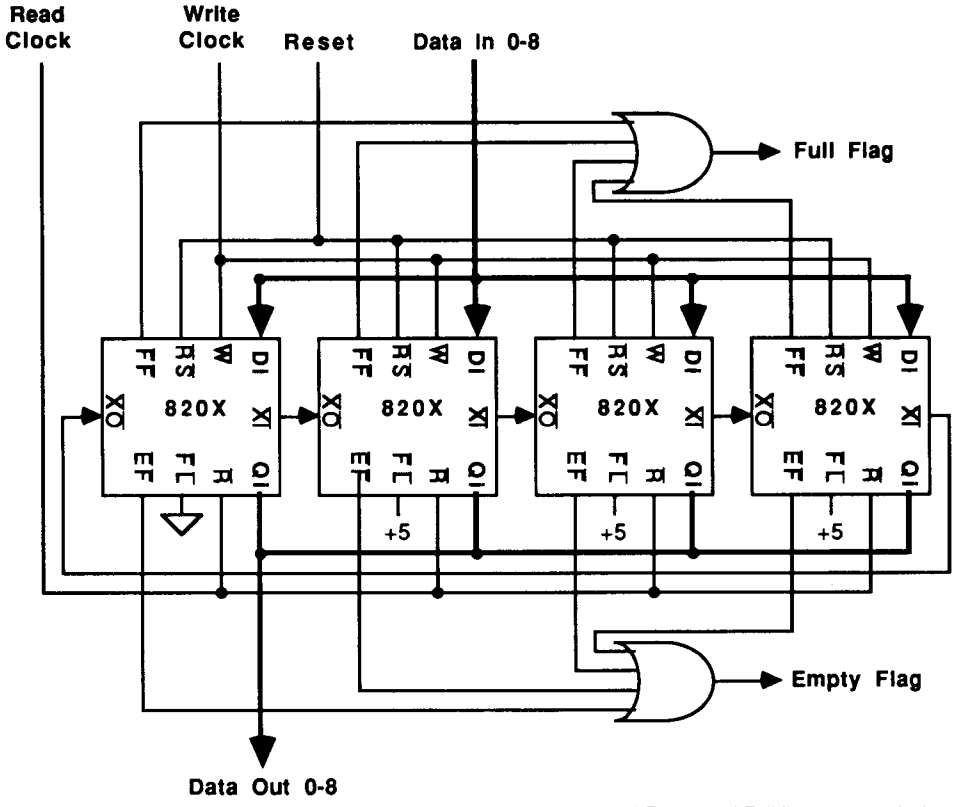

Note: The composite Empty and Full flags require the OR-ing of the individual Empty and Full flags, respectively

Figure 3. Building a 4N-deep FIFO Using Four N-deep FIFOs

FOR MORE INFORMATION CONTACT

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