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512K x 32 SRAM MODULE

PUMA 2/77S16000/A - 020/025/35

Issue 4.2 : November 1998

Description

Available in PGA (PUMA 2) and Gullwing (PUMA 77) footprints, the PUMA **S16000 is a 16 MBit SRAM module user configurable as 512K x 32, 1M x 16 or 2M x 8. The device is available with fast access times of 20,25 and 30ns. A low power standby and Data Retention mode is available. The device may be screened in accordance with MIL-STD-883.

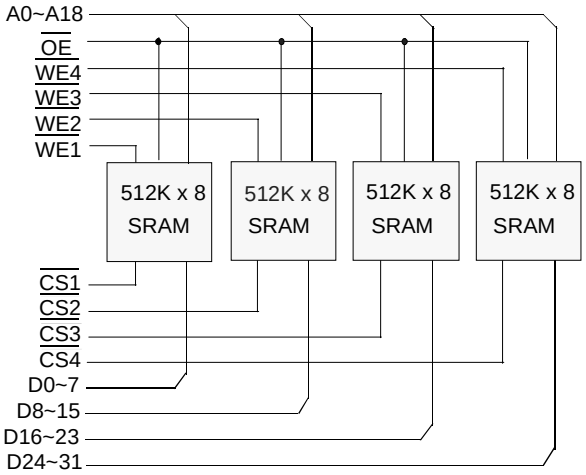
16,777,216 bit CMOS High Speed Static RAM

Features

- 16MBit Fast SRAM Module.
- Fast Access times of 20/25/35ns.
- Configurable as 8 / 16 / 32 bit wide output.
- Operating Power 2130 / 2800 / 4150 mW (max).
  Standby CMOS 220mW (max).
- Low voltage data retention.
- Single 5V±10% Power supply.
- TTL compatible inputs and outputs.
- May be screened in accordance with MIL-STD-883.
- PUMA 2 - 66 pin ceramic PGA
- PUMA77 - 68 pin ceramic Gullwing

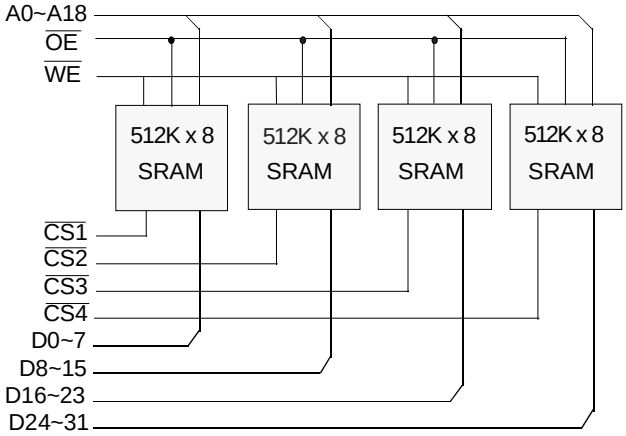
Block Diagram

PUMA 2S16000 and 77S16000A



Block Diagram

PUMA 77S16000



Pin Functions

A0~A18	Address Inputs	**D0~D31**	Data Inputs/Outputs
$\overline{CS1\sim4}$	Chip Select	**$\overline{OE}$**	Output Enable
$\overline{WE1\sim4}$	Write Enable	**NC**	No Connect
V_{cc}	Power (+5V)	**GND**	Ground

DC OPERATING CONDITIONS

Absolute Maximum Ratings (1)

Voltage on any pin relative to V_{ss} (2)	V_T	-0.5V to +7.0	V
Power Dissipation	P_D	4	W
Storage Temperature	T_{STG}	-55 to +150	˚C

Notes (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) Pulse width:- 3.0V for less than 10ns.

Recommended Operating Conditions

Parameter	*Symbol*	*min*	*typ*	*max*	*units*	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	
Input High Voltage	V_{IH}	2.2	-	V_{CC}+0.5	V	
Input Low Voltage	V_{IL}	-0.5	-	0.8	V	
Operating Temperature	T_A	0	-	70	˚C	
	T_{AI}	-40	-	85	˚C	(Suffix **I**)
	T_{AM}	-55	-	125	˚C	(Suffix **M**, **MB**)

DC Electrical Characteristics (V_{CC}=5V±10%,T_A=-55°C to +125°C)

Parameter		*Symbol*	*Test Condition*	*min*	*typ*(1)	*max*	*Unit*
Input Leakage Current	Address,$\overline{OE}$	I_{LI1}	V_{IN} = 0V to V_{CC}	-8	-	8	µA
	$\overline{WE}$, $\overline{CS}$	I_{LI2}	V_{IN} = 0V to V_{CC}	-2	-	2	µA
Output Leakage Current		I_{LO}	$\overline{CS}$(2) = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0V to V_{CC}	-8	-	8	µA
			$\overline{WE}$(2) = V_{IL}				
Average Supply Current	32 bit	I_{CC32}	$\overline{CS}$(2)=V_{IL}, Minumum cycle, $I_{I/O}$ = 0mA				
			$\overline{WE}$(2)=V_{IL} or $\overline{WE}$(2)=$\overline{OE}$=V_{IH}, 100% duty.	-	-	720	mA
	16 bit	I_{CC16}	As above	-	-	480	mA
	8 bit	I_{CC8}	As above	-	-	360	mA
Standby Supply Current	TTL levels	I_{SB}	$\overline{CS}$(2) = V_{IH}, V_{CC}=5.5V	-	-	240	mA
	CMOS levels	I_{SB1}	$\overline{CS}$(2) ≥ V_{CC}-0.2V, 0.2V ≥ V_{IN}≥ V_{CC}-0.2V	-	-	40	mA
Output Voltage Low		V_{OL}	I_{OL} = 8.0 mA	-	-	0.4	V
Output Voltage High		V_{OH}	I_{OH} = -4.0 mA	2.4	-	-	V

Notes: (1) Typical values are at V_{CC}=5.0V,T_A=25˚C and specified loading.

(2) $\overline{CS}$ and $\overline{WE}$ above are accessed through $\overline{CS1}$~$\overline{4}$ and $\overline{WE1}$~$\overline{4}$ respectively. These inputs must be operated simultaneously for 32 bit mode, in pairs for 16 bit mode and singly for 8 bit mode.

Capacitance (V_{CC}=5V±10%,T_A=25°C) Note: These parameters are calculated and not measured.

Parameter		*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance	Address, $\overline{OE}$	C_{IN1}	V_{IN}=0V	-	34	pF
	$\overline{WE1\sim4}$, $\overline{CS1\sim4}$	C_{IN2}	V_{IN}=0V	-	6	pF
I/O Capacitance	D0~31	$C_{I/O}$	$V_{I/O}$=0V	-	42	pF (8 bit mode)

Operating Modes

The Table below shows the logic inputs required to control the operating modes of each of the SRAMs on the device.

Mode	***$\overline{CS}$***	***$\overline{OE}$***	***$\overline{WE}$***	***V_{cc} Current***	***I/O Pin***	***Reference Cycle***
Not Selected	1	X	X	I_{SB1},I_{SB2}	High Z	Power Down
Output Disable	0	1	1	I_{CC}	High Z	
Read	0	0	1	I_{CC}	D_{OUT}	Read cycle
Write	0	X	0	I_{CC}	D_{IN}	Write Cycle

1 = V_{IH},
0 = V_{IL},
X = Don't Care

Note: $\overline{CS}$ above is accessed through $\overline{CS1\sim4}$ and $\overline{WE}$ is accessed through $\overline{WE1\sim4}$. For correct operation, $\overline{CS1\sim4}$ and $\overline{WE1\sim4}$ must operate simultaneously for 32 bit operation, in pairs for 16 bit operation, or singly for 8 bit operation.

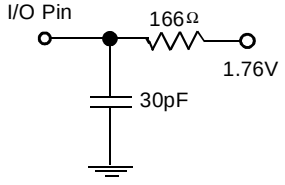
Low V_{cc} Data Retention Characteristics - L Version Only (T_A=-55°C to +125°C)

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
V_{CC} for Data Retention	V_{DR}	$\overline{CS1\sim4} \geq V_{CC}$-0.2V	2.0	-	5.5	V
Data Retention Current	I_{CCDR}	V_{CC}= 3.0V, $\overline{CS1\sim4} \geq V_{CC}$-0.2V, 0.2V ≥ $V_{IN} \geq V_{CC}$-0.2V	-	-	28	mA
Chip Deselect to Data Retention	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	5	-	-	ms

AC Test Conditions

*Input pulse levels: 0.0V to 3.0V
*Input rise and fall times: 3 ns
*Input and Output timing reference levels: 1.5V
*V_{cc}=5V±10%
*PUMA module is tested in 32 bit mode.

Output Load



AC OPERATING CONDITIONS

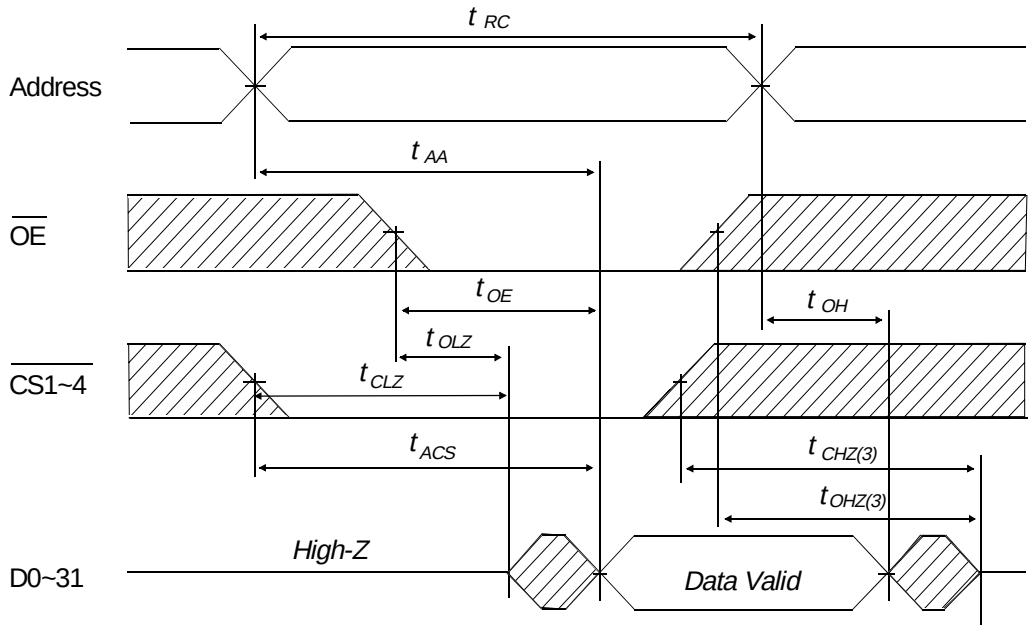
Read Cycle

		020		025		35		
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*min*	*max*	*Units*
Read Cycle Time	t_{RC}	20	-	25	-	35	-	ns
Address Access Time	t_{AA}	-	20	-	25	-	35	ns
Chip Select Access Time	t_{ACS}	-	20	-	25	-	35	ns
Output Enable to Output Valid	t_{OE}	-	10	-	15	-	15	ns
Output Hold from Address Change	t_{OH}	5	-	5	-	5	-	ns
Chip Selection to Output in Low Z	t_{CLZ}	5	-	5	-	5	-	ns
Output Enable to Output in Low Z	t_{OLZ}	5	-	0	-	0	-	ns
Chip Deselection to Output in High Z(3)	t_{CHZ}	-	10	0	10	0	10	ns
Output Disable to Output in High Z(3)	t_{OHZ}	0	10	0	10	0	10	ns

Write Cycle

		020		025		35		
Parameter	*Symbol*	*min*	*max*	*min*	*max*	*min*	*max*	*Unit*
Write Cycle Time	t_{WC}	20	-	25	-	35	-	ns
Chip Selection to End of Write	t_{CW}	15		15	-	15	-	ns
Address Valid to End of Write	t_{AW}	15	-	15	-	15	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	15	-	15	-	15	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Write to Output in High Z	t_{WHZ}	0	10	0	10	0	10	ns
Data to Write Time Overlap	t_{DW}	10	-	10	-	10	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW}	5	-	5	-	5	-	ns

Read Cycle Timing Waveform (1,2)



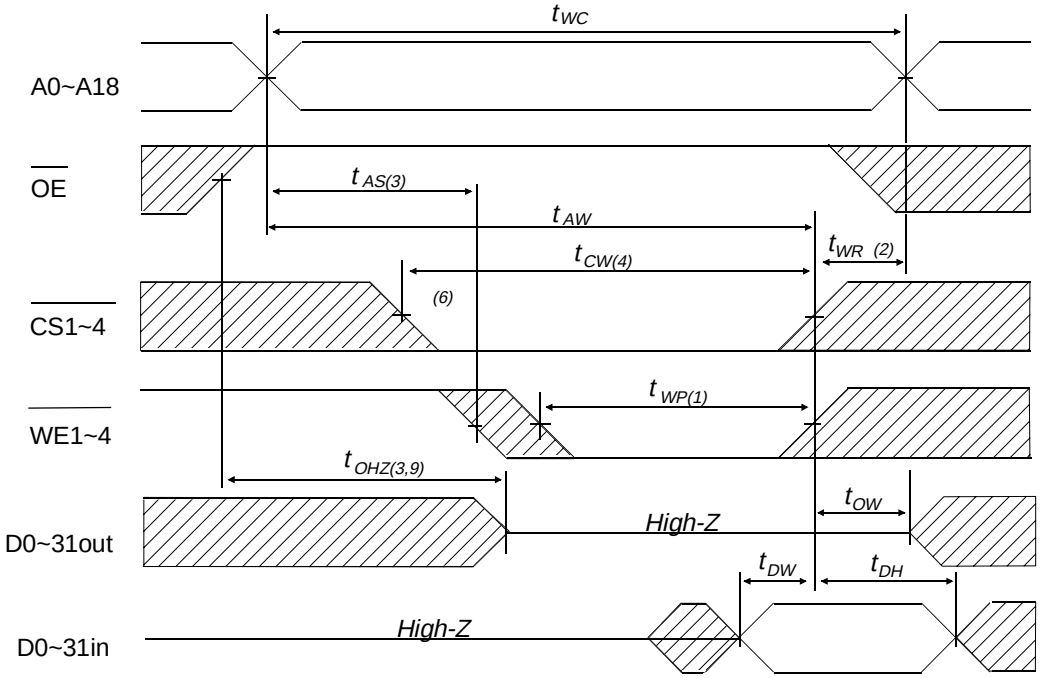
Notes:

(1) During the Read Cycle, $\overline{WE}$ is high for the module.

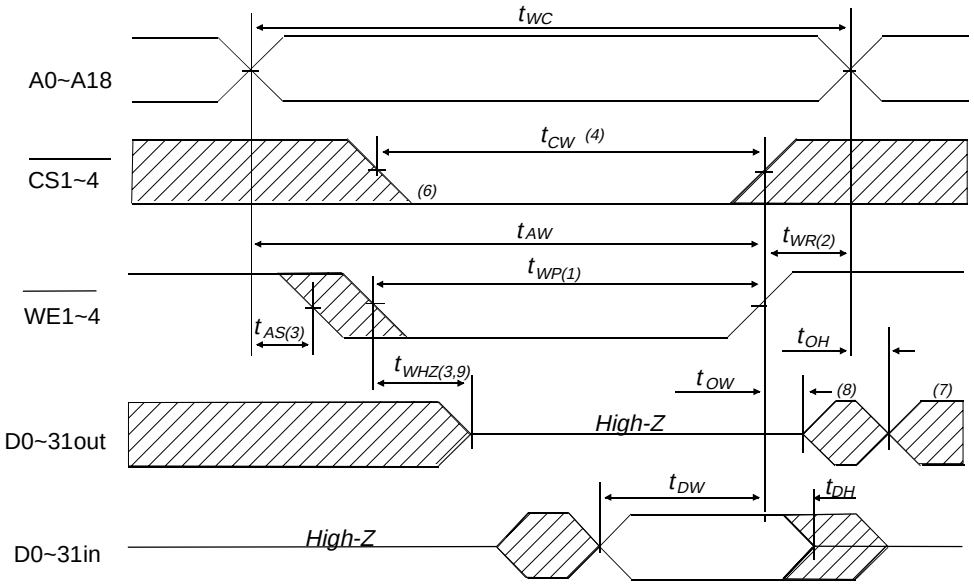
(2) Address valid prior to or coincident with $\overline{CS}$ transition Low.

(3) t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

Write Cycle No.1 Timing Waveform



Write Cycle No.2 Timing Waveform (5)



AC Characteristics Notes

(1) A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.

(2) t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.

(3) During this period, I/O pins are in the output state. Input signals out of phase must not be applied.

(4) If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.

(5) $\overline{OE}$ is continuously low. ($\overline{OE}$=V_{IL})

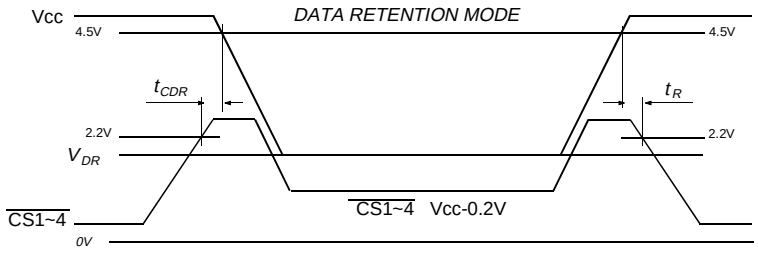
(6) D_{OUT} is in the same phase as written data of this write cycle.

(7) D_{OUT} is the read data of next address.

(8) If $\overline{CS}$ is low during this period, I/O pins are in the output state. Input signals out of phase must not be applied.

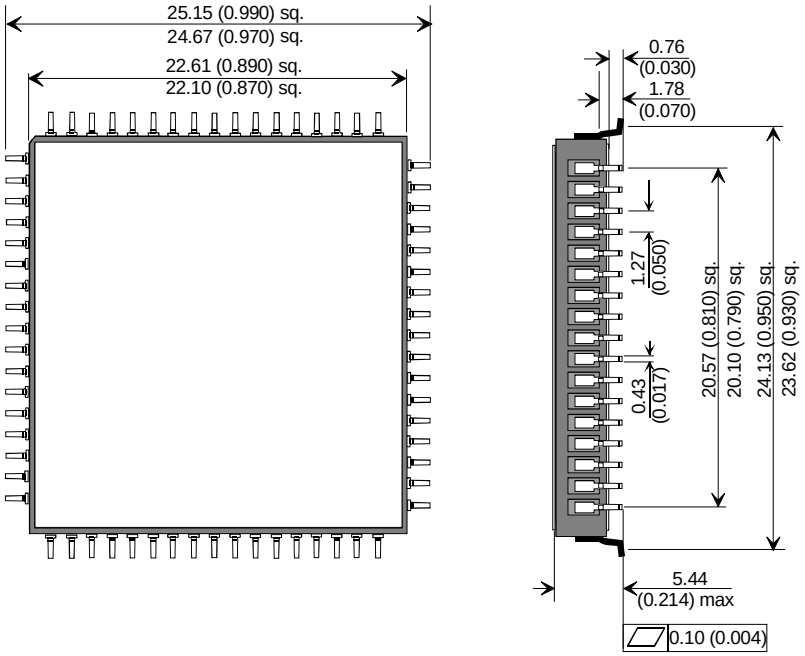
(9) t_{WHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

Low V_{CC} Data Retention Timing Waveform

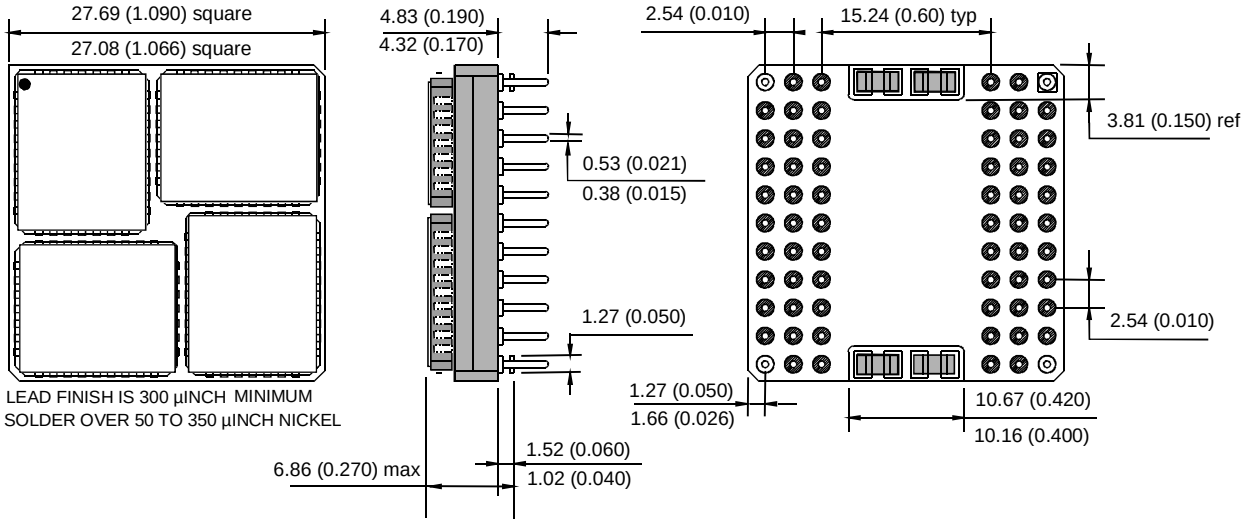


Package Details

PUMA 77S16000

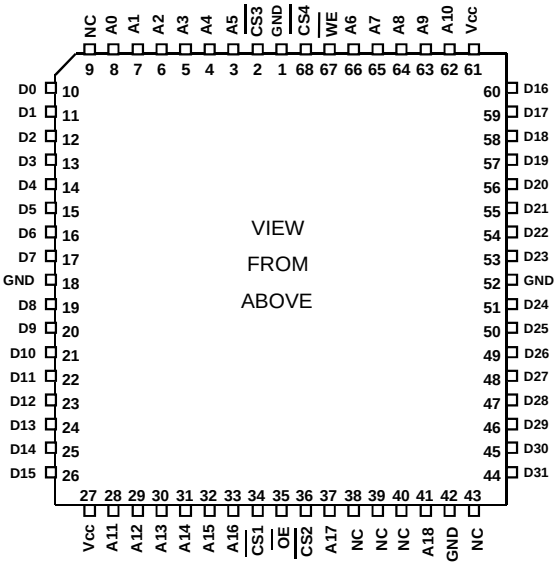


PUMA 2S16000

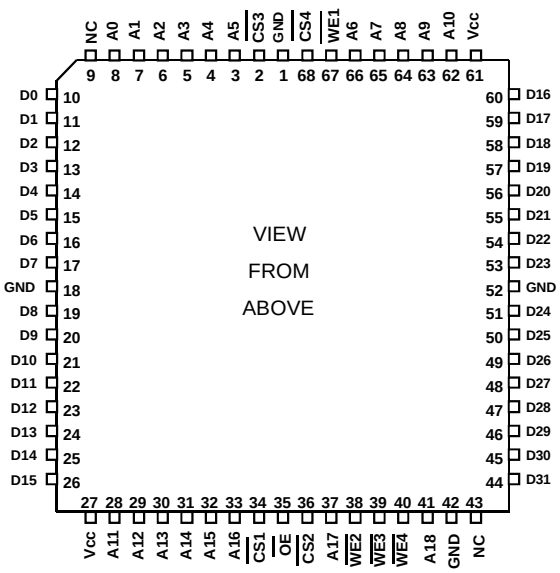


Pin Definitions

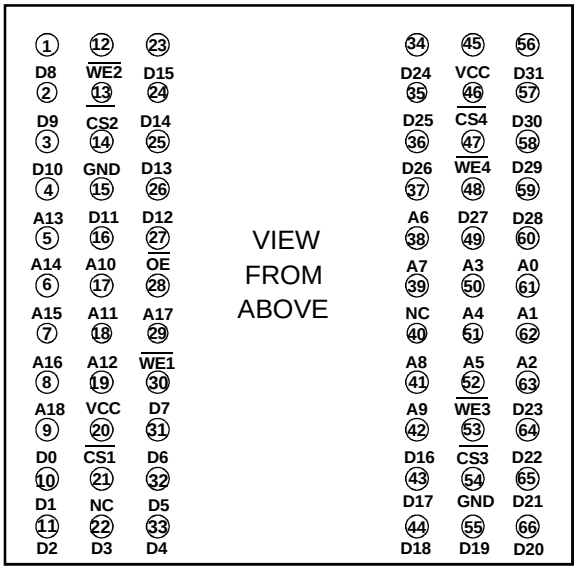
PUMA 77S16000



PUMA 77S16000A



PUMA 2S16000



Military Screening Procedure

MultiChip Screening Flow for high reliability product in accordance with Mil-883 method 5004 shown below

MB MULTICHIP MODULE SCREENING FLOW

SCREEN	*TEST METHOD*	*LEVEL*
Visual and Mechanical		
Internal visual	2017 Condition B or manufacturers equivalent	100%
Temperature cycle	1010 Condition B (10 Cycles,-55°C to +125°C)	100%
Constant acceleration	2001 Condition E (Y_1 only) (10,000g)	100%
Burn-In		
Pre-Burn-in electrical	Per applicable device specifications at T_A=+25°C	100%
Burn-in	Method 1015,Condition D,T_A=+125°C,160hrs min	100%
Final Electrical Tests	Per applicable Device Specification	
Static (dc)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Functional	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Switching (ac)	a) @ T_A=+25°C and power supply extremes	100%
	b) @ temperature and power supply extremes	100%
Percent Defective allowable (PDA)	Calculated at post burn-in at T_A=+25°C	10%
Hermeticity	1014	
Fine	Condition A	100%
Gross	Condition C	100%
Quality Conformance	Per applicable Device Specification	Sample
External Visual	2009 Per vendor or customer specification	100%

Ordering Information

PUMA 2S16000AMB-020

Speed	020	=	20 ns
	025	=	25 ns
	35	=	35 ns
Temp. range/screening	Blank	=	Commercial Temperature
	I	=	Industrial Temperature
	M	=	Military Temperature
	MB	=	May be processed in accordance with MIL-STD-883
$\overline{WE}$ Option	Blank	=	Single $\overline{WE}$ (PUMA 77 only) $\overline{WE1{\sim}4}$ (PUMA 2 only)
	A	=	$\overline{WE1{\sim}4}$ (PUMA 77 only)
Organisation	16000	=	512Kx 32, user confiurable as 1M x 16 and 2M x 8
Technology	S	=	SRAM MEMORY
Package	PUMA 2	=	JEDEC 66 Pin Ceramic PGA package
	PUMA 77	=	JEDEC 68 Leaded Gull Wing Ceramic Surface Mount package