

QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

D2804, MARCH 1984 — REVISED SEPTEMBER 1987

- Inputs are TTL-Voltage Compatible
- 2-Way Asynchronous Communication Between Data Buses
- High-Current Outputs Can Drive Up to 15 LSTTL Loads
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

description

These four-data line transceivers are designed for asynchronous two-way communications between data buses. The SN74HCT[®] devices can be used to drive terminated lines down to 133 Ω.

These parts differ from their TTL counterparts (LS, ALS, and AS) in that these CMOS parts do not have a bus-latching mode in which both the outputs are simultaneously enabled. Instead of this latched mode, the buses are isolated, thus preventing potential bus conflicts if both buses are active. However, with the exception of the fourth line of the function table, their functional operation is identical to their TTL counterparts. The two enables have been renamed G1 and G2 since they work together to determine the direction of transmission rather than each enable controlling one direction independently of the other. Whenever G1 and G2 are at opposite logic levels with respect to each other, isolation between buses results.

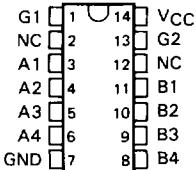
The SN54HCT[®] family is characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN74HCT[®] is characterized for operation from -40 °C to 85 °C.

FUNCTION TABLE

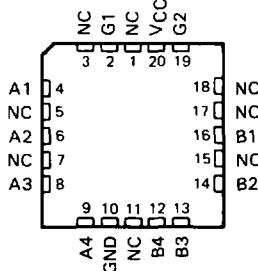
INPUTS	'HCT242	'HCT243
G1	G2	
L	L	Ā to B
H	H	Ā to A
H	L	B to A
L	H	Isolation

SN54HCT242, SN54HCT243 . . . J PACKAGE
SN74HCT242, SN74HCT243 . . . D OR N PACKAGE

(TOP VIEW)



SN54HCT242, SN54HCT243 . . . FK PACKAGE
(TOP VIEW)



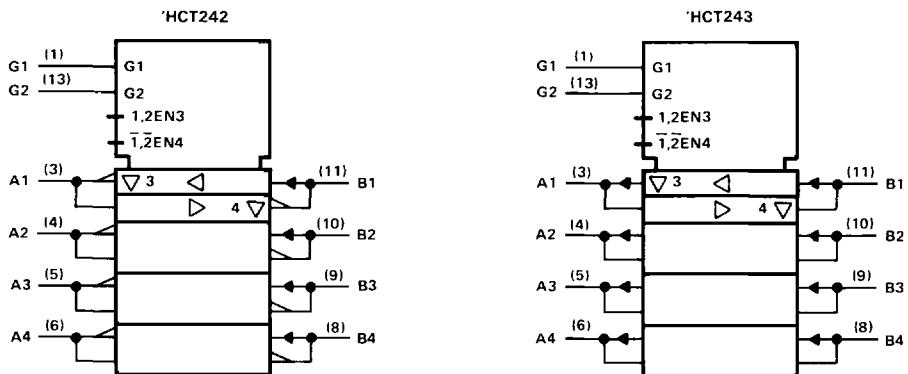
NC — No internal connection

**SN54HCT242, SN54HCT243
SN74HCT242, SN74HCT243
QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS**

logic symbols †

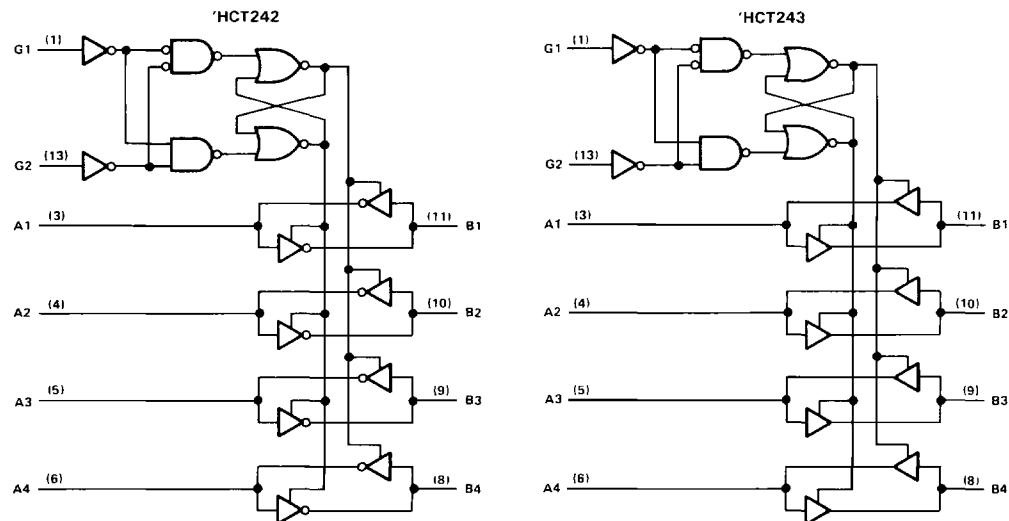
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†These symbols are in accordance with ANSI-IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for D, J, and N packages.

**SN54HCT242, SN54HCT243
SN74HCT242, SN74HCT243
QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS**

absolute maximum ratings over operating free-air temperature range[†]

Supply voltage, V _{CC}	-0.5 V to 7 V
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC})	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±20 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±35 mA
Continuous current through V _{CC} or GND pins	±70 mA
Lead temperature 1.6 mm (1/16 in) from case for 60 s: FK or J package	300°C
Lead temperature 1.6 mm (1/16 in) from case for 10 s: D or N package	260°C
Storage temperature range	-65°C to 150°C

[†]Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

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HCMOS Devices

recommended operating conditions

		SN54HCT242 SN54HCT243			SN74HCT242 SN74HCT243			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage V _{CC} = 4.5 V to 5.5 V	2			2			V
V _{IL}	Low-level input voltage V _{CC} = 4.5 V to 5.5 V	0	0.8	0	0	0.8	0	V
V _I	Input voltage	0	V _{CC}	0	V _{CC}	0	V _{CC}	V
V _O	Output voltage	0	V _{CC}	0	V _{CC}	0	V _{CC}	V
t _t	Input transition (rise and fall) times	0	500	0	0	500	0	V
T _A	Operating free-air temperature	-55	125	-40	-40	85	85	V

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54HCT242		SN74HCT242		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL} , I _{OH} = -20 μA	4.5 V	4.4	4.499		4.4		4.4		V
	V _I = V _{IH} or V _{IL} , I _{OH} = -6 mA	4.5 V	3.98	4.30		3.7		3.84		
V _{OL}	V _I = V _{IH} or V _{IL} , I _{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
	V _I = V _{IH} or V _{IL} , I _{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
I _I	V _I = V _{CC} or 0	5.5 V		±0.1	±100		±1000		±1000	nA
I _{OZ} [‡]	V _O = V _{CC} or 0, V _I = V _{IH} or V _{IL}	5.5 V		±0.01	±0.5		±10		±5	μA
I _{CC}	V _I = V _{CC} or 0, I _O = 0	5.5 V			8		160		80	μA
ΔI _{CC} [§]	One input at 0.5 V or 2.4 V Other inputs at 0 V or V _{CC}	5.5 V		1.4	2.4		2.9		3	mA
C _i [¶]		4.5 to 5.5 V		3	10		10		10	pF

[‡]For I/O ports, the parameter is included in the off-state output current.

[§]This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

[¶]This parameter, C_i, does not apply to transceiver I/O ports.

**SN54HCT242, SN54HCT243
SN74HCT242, SN74HCT243
QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS**

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), $C_L = 50 \text{ pF}$ (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	TA = 25°C			SN54HCT242		SN74HCT242		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A	4.5 V	15	30		45		38		ns
			5.5 V	13	27		41		34		
t _{en}	G1 or G2	A or B	4.5 V	21	40		60		50		ns
			5.5 V	19	36		54		45		
t _{dis}	G1 or G2	A or B	4.5 V	19	40		60		50		ns
			5.5 V	18	36		54		45		
t _t		A or B	4.5 V	8	12		18		15		ns
			5.5 V	7	11		16		14		

C _{pd}	Power dissipation capacitance per tranciever	No load, T _A = 25°C	40 pF typ
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switching characteristics over recommended operating free-air temperature range (unless otherwise noted), $C_L = 150 \text{ pF}$ (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	TA = 25°C			SN54HCT242		SN74HCT242		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A or B	B or A	4.5 V	21	47		71		59		ns
			5.5 V	18	42		64		53		
t _{en}	G1 or G2	A or B	4.5 V	27	57		86		71		ns
			5.5 V	24	51		77		64		
t _t		A or B	4.5 V	17	42		63		53		ns
			5.5 V	14	38		57		48		

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.