*i*Coupler®

High Speed Isolated RS-485 Transceiver

Preliminary Technical Data

ADM2486

FEATURES

High-Speed isolated RS-485 transceiver
Electrical Data Isolation
  2500V_{RMS} for 1 min (UL 1577 Certification)
PROFIBUS Compliant
Complies with ANSI TIA/EIA RS-485-A-1998 and
  ISO 8482:1987(E)
High data rate: 20 Mbaud (NRZ)
Low power operation:
  DC–5 MBd: 5.7 mA max
  12 MBd: 8.5 mA max
  20 MBd: 10 mA max
Suitable for 5 V or 3 V operation (V_{DD}1)
High common mode transient immunity: >25 KV/ µs
Dedicated Isolated DE Status Output
Receiver open-circuit fail-safe design
Glitch-free power-up/down protection
Thermal shutdown protection
Safety and regulatory approvals (pending)
CSA Component Acceptance Notice #5A
VDE Certificate of Conformity
  DIN EN 60747-5-2 (VDE 0884 Rev. 2):2003-01
  DIN EN 60950 (VDE 0805):2001-12;EN 60950:2000
  VIORM = 560 V PEAK
Operating Temperature Range: -40° to 85°C
Wide body 16-lead SOIC package

APPLICATIONS

Isolated RS-485/RS-422 Interfaces
PROFIBUS networks
Industrial field networks
Multipoint data transmission systems

FUNCTIONAL BLOCK DIAGRAM

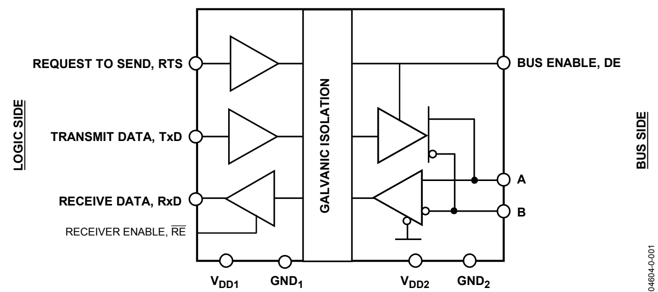

Figure 1.

GENERAL DESCRIPTION

The ADM2486[1] differential bus transceiver is an integrated, galvanically isolated component designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and complies with ANSI TIA/EIA RS-485-A and ISO 8482:1987(E).

The device employs Analog Devices' iCoupler technology to combine a 3-channel isolator, a 3-state differential line driver, and a differential input receiver into a single package. The logic side of the device can be powered with either a 5 V or a 3 V supply while the bus side is powered with a 5 V supply.

The ADM2486 driver has an active high enable. The driver differential outputs and the receiver differential inputs are connected internally to form a differential input/output port that imposes minimal loading on the bus when the driver is disabled or when VDD1 or VDD2 =0. Also provided is an active high receiver disable that causes the receive output to enter a high impedance state.

The device has current-limiting and thermal shutdown features to protect against output short circuits and situations where bus contention might cause excessive power dissipation.

[1] Protected by U.S. patent 5,952,849. Additional patents are pending.

Rev. PrA

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.326.8703

TABLE OF CONTENTS

REVISION HISTORY

1/04—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

Table 1. All voltages are relative to their respective ground; 2.7 ≤ V_{DD1} ≤ 5.5 V, 4.75 V ≤ V_{DD2} ≤ 5.25 V. All min/max specifications apply over the entire recommended operation range unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5.0 V unless otherwise noted.

Parameter	Symbol	Min.	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Supply Current, Logic Side, 5 V Operation[1]						
TxD/RxD Data Rate < 2 Mbps	$I_{DD1(2)}$			2.0	mA	4.5V ≤ V_{DD1} ≤ 5.5 V, Fig. 2
TxD/RxD Data Rate 12 Mbps	$I_{DD1(12)}$		3.5		mA	4.5V ≤ V_{DD1}≤ 5.5 V, Fig. 2
TxD/RxD Data Rate 20 Mbps	$I_{DD1(35)}$		5.4		mA	4.5V ≤ V_{DD1}≤ 5.5 V, Fig. 2
Supply Current, Logic Side, 3 V Operation[1]						
TxD/RxD Data Rate < 2 Mbps	I_{DD1}			1.1	mA	2.7V ≤ V_{DD1}≤ 3.3 V, Fig. 2
TxD/RxD Data Rate 12 Mbps	$I_{DD1(12)}$		1.9		mA	2.7V ≤ V_{DD1}≤ 3.3 V, Fig. 2
TxD/RxD Data Rate 20 Mbps	$I_{DD1(35)}$		2.9		mA	2.7V ≤ V_{DD1}≤ 3.3 V, Fig. 2
Supply Current, Bus Side[1]						
Driver Disabled	$I_{DD1(Q)}$			3.0	mA	V_{RTS} = 01, Fig. 2
TxD/RxD Data Rate < 2 Mbps	$I_{DD1(2)}$			3.5	mA	V_{RTS} = V_{DD}, Fig. 2
TxD/RxD Data Rate 12 Mbps	$I_{DD2(12)}$		4.7		mA	V_{RTS} = V_{DD}, Fig. 2
TxD/RxD Data Rate 20 Mbps	$I_{DD2(35)}$		6.6		mA	V_{RTS} = V_{DD}, Fig. 2
Transmit Data Input Current	I_{TXD}	-10	0.01	10	•A	V_{RxD} = V_{DD1}or 0
Request to Send Input Current	I_{RTS}	-10	0.01	10	•A	V_{RTS} = V_{DD1}or 0
Receiver Enable Input Current		-10	0.01	10	•A	$V_{\overline{RE}}$ = V_{DD1}or 0
Receiver Data:						
Logic High Output Voltage	V_{OHRXD}	V_{DD1} - 0.1	V_{DD1}		V	I_{ORXD} = -20 •A, VA-VB = 0.2V
		VD_{D1} - 0.4	V_{DD1}-0.2		V	I_{ORXD} = -4 mA, VA-VB = 0.2V
Logic Low Output Voltage	V_{OLRXD}		0.0	0.1	V	I_{ORXD} = 20 •A, VA-VB = -0.2V
			0.2	0.4	V	I_{ORXD} = 4 mA, VA-VB = -0.2V
Bus Enable:						
Logic High Output Voltage, Bus Enable	V_{OHDE}	V_{DD2} - 0.1	V_{DD2}		V	I_{ODE} = -20 •A
		V_{DD2} - 0.3	V_{DD2}-0.1		V	I_{ODE} = -1.6 mA
		V_{DD2} - 0.4	V_{DD2}-0.2		V	I_{ODE} = -4 mA
Logic Low Output Voltage, Bus Enable	V_{OLDE}		0.0	0.1	V	I_{ODE} = 20 •A
			0.1	0.3	V	I_{ODE} = 1.6 mA
			0.2	0.4	V	I_{ODE} = 4 mA
Receiver Enable:						
Logic High Output Voltage, Receive Enable	$V_{OH\overline{RE}}$	VDD2 - 0.1	V_{DD2}V		V	$I_{O\overline{RE}}$ = −20µA
		V_{DD2} - 0.3	V_{DD2}-0.1		V	$I_{O\overline{RE}}$ I = −1.6 mA
		V_{DD2} - 0.4	V_{DD2}-0.2		V	$I_{O\overline{RE}}$ = −4 mA
Logic Low Output Voltage, Receive Enable	$V_{OL\overline{RE}}$		0.0	0.1	V	$I_{O\overline{RE}}$ = −20µA
			0.1	0.3	V	$I_{O\overline{RE}}$ = −1.6 mA
			0.2	0.4	V	$I_{O\overline{RE}}$ = −4 mA
Driver Outputs:						
Differential Output Voltage, Unloaded	$\lvert V_{OD1}\rvert$			5.0	V	Output unloaded

[1] RTS data rate assumed to be <1 MBd and independent of TxD and RxD data rates. TxD and RxD duty cycles are 50%..

Parameter	Symbol	Min.	Typ	Max	Unit	Test Conditions
Differential Output Voltage, Loaded	$\|V_{OD2}\|$	2.1		5.0	V	V_{OC} = 5 V, R_L = 100 Ω, Fig. 3
	$\|V_{OD3}\|$	2.1		5.0	V	R_L = 54 Ω, Fig. 3
	$\|V_{OD4}\|$	2.1		5.0	V	-7 V ≤ V_{test1} ≤ 12 V, Fig. 4
Change in Differential Output Voltage Magnitude forComplementary Output States	$\Delta\|V_{OD}\|$			0.2	V	RL = 54 Ω or 100 Ω, Fig. 3
Common Mode Output Voltage	V_{OC}	-1		3.0	V	RL = 54 Ω or 100 Ω, Fig. 3
Change in Common Mode Output Voltage Magnitude for Complementary Output States	$\Delta\|V_{OC}\|$			0.2	V	RL = 54 Ω or 100 Ω, Fig. 3
Output Current	I_O				mA	See Receiver Input Current
Short Circuit Output Current[2]	I_{OS}	60		200	mA	
Receiver Inputs:						
Differential Input Threshold Voltage	V_{TH}	-0.2		0.2	V	
Input Voltage Hysteresis	V_{HYS}		70		mV	V_{OC} = 0 V
Input Current (A, B)	I_I			1.0	mA	V_{OC} = 12 V
		-0.8			mA	V_{OC} = -7 V
Line Input Resistance	R_{IN}	20			kΩ	
AC SPECIFICATIONS						
Drive Enable						
Propagation Delay[3, 4]	t_{RTSLH}, t_{RTSHL}	20	35	45	ns	RL = 54 Ω, CL1 = CL2 = 100 pF, Fig. 5
Pulse Width Distortion, |tRTSH-tRTSL|	PWD_{RTS}		1	3	ns	RL = 54 Ω, CL1 = CL2 = 100 pF, Fig. 5
Receive Enable/Disable Time	t_{RE}		3	5	ns	CL = 15pF, Fig. 7
Transmit Data/Driver Outputs:						
Propagation Delay[4]	t_{TALH}, t_{TAHL}, t_{TBLH}, t_{TBHL}	25	45	55	ns	RL = 54 Ω, CL1 = CL2 = 100 pF, Fig. 5 and Fig. 9
Switching Skew, $t_{MLH} = \|t_{TALH}-t_{TBLH}\|$, $t_{MHL} = \|t_{TAHL}-t_{TBHL}\|$	t_{MLH}, t_{MHL}		2	5	ns	RL = 54 Ω, CL1 = CL2 = 100 pF, Fig. 5 and Fig. 9
Pulse Width Distortion,						
$PWD_{TXDA} = \|t_{TALH}-t_{TAHL}\|$, $PWD_{TXDB} = \|t_{TBLH}-t_{TBHL}\|$	PWD_{TXDA}, PWD_{TXDB}			3	ns	RL = 54 Ω, CL1 = CL2 = 100 pF, Fig. 5 and Fig. 9
Differential Output Rise/Fall Time[5]	t_R, t_F		5	8	ns	RL = 54 Ω, CL1 = CL2 = 100 pF, Fig. 5 and Fig. 9
Driver Enable Time, High Impedance Low/High[5]	t_{AZL}, t_{BZL}, t_{AZH}, t_{BZH}		43	53	ns	$V_{TXD} = V_{DD1}$ or 0, Fig. 6 and Fig. 10
Driver Disable Time, Low/High to High Impedance[5]	t_{ALZ}, t_{BLZ}, t_{AHZ}, t_{BHZ}		43	53	ns	$V_{TXD} = V_{DD1}$ or 0, Fig. 6 and Fig. 10
Enable Skew, $t_{MZL} = \|t_{TAZL}-t_{TBZL}\|$, $t_{MZH} = \|t_{TAZH}-t_{TBZH}\|$	t_{MZL}, t_{MZH}		1	3	ns	$V_{TXD} = V_{DD1}$ or 0, Fig. 6 and Fig.10
Disable Skew, $t_{MLZ} = \|t_{TALZ}-t_{TBLZ}\|$, $t_{MHZ} = \|t_{TAHZ}-t_{TBHZ}\|$	t_{MLZ}, t_{MHZ}		2	5	ns	$V_{TXD} = V_{DD1}$ or 0, Fig. 6 and Fig.10
Receive Data/Receiver Inputs:						
Propagation Delay[4]	t_{RALH}, t_{RAHL}, t_{RBLH}, t_{RBHL}	25	45	55	ns	CL = 15 pF, Fig. 7 and Fig.11

[2] Short circuit output current must not oscillate or vary for the first 100 µs after the short circuit is present.
[3] t_{RALH} and t_{RBLH} propagation delays are measured from the 50% level of the falling edge of the RTS signal to the 50% level of the falling edge of the DE signal. tRTSLH propagation delay is measured from the 50% level of the rising edge of the RTS signal to the 50% level of the rising edge of the DE signal.
[4] Measurement is made with an input signal having a frequency > 1 MHz, rise/fall times < 6 ns, and a duty cycle =50%.
[5] CM is the maximum common mode voltage slew rate that can be sustained while maintaining specification-compliant operation. VCM is the common mode potential difference between the logic and bus sides. The transient magnitude is the range over which the common mode is slewed. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.

Parameter	Symbol	Min.	Typ	Max	Unit	Test Conditions
Pulse Width Distortion,						
$PWD_{RXDA} = \|t_{RALH}-t_{RAHL}\|$, $PWD_{RXDB} = \|t_{RBLH}-t_{RBHL}\|$	PWD_{RXDA}, PWD_{RXDB}			3	ns	CL = 15 pF, Fig. 7 and 11
Input Capacitance, A-B	C_I		4	10	pF	
Common Mode Transient Immunity6	CM	25			KV/µs	$V_{TXD} = V_{DD}$ or 0, V_{CM} = 1000 V, transient magnitude = 800 V
High Frequency Common Mode Noise Immunity	$V_{CM(HF)}$		100		mV	V_{HF} = ±5 V, -2V ≤ V_{test2} ≤ 7 V, 1 ≤ f_{test} ≤ 50 MHz, Fig. 8

PACKAGE CHARACTERISTICS

Table 2. Device considered a two-terminal device: Pins 1 to 8 shorted together and Pins 9 to16 shorted together.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-Output)	R_{I-O}		10^{12}		Ω	
Capacitance (Input-Output)	C_{I-O}		3		pF	f = 1 MHz
Input IC Junction-to-Case Thermal Resistance	θ_{JCI}		33		°C/W	
Output IC Junction-to-Case Thermal Resistance	θ_{JCO}		28		°C/W	
Package Power Dissipation	P_{PD}			600	mW	

REGULATORY INFORMATION

Table 3. The ADM2486 meets these regulations upon product release.

Organization	Regulation	Notes
UL	Recognized under 1577 component recognition program.	In accordance with UL1577, each ADM2486 is proof tested by applying an insulation test voltage ≥ 3000 Vrms for 1 second. (Current leakage detection limit = 5 µA.)
CSA	Approved under CSA Component Acceptance Notice #5A.	
VDE	Approved according to: DIN EN 60747-5-2 (VDE 0884 Rev. 2): 2002-04 DIN EN 60950 (VDE 0805):2001-12; EN 60950: 2000.	In accordance with VDE 0884, each ADM2486 is proof tested by applying an insulation test voltage ≥ 1050 V_{PEAK} for 1 second. (Partial discharge detection limit = 5 pC.)

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 4.

Parameter	Symbol	Value	Unit	Conditions
Rated dielectric insulation voltage		2500	V_{RMS}	1-minute duration.
Minimum external air gap (clearance)	L(I01)	7.40 min.	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum external tracking (creepage)	L(I02)	8.51 min.	mm	Measured from input terminals to output terminals, shortest distance path along body.
.				
Minimum internal gap (internal clearance)		0.02 min.	mm	Insulation distance through insulation.
Tracking resistance (comparative tracking index)	CTI	>175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation group		IIIa		Material Group (DIN VDE 0110,1/89,Table 1)

VDE 0884 INSULATION CHARACTERISTICS

Table 5. This isolator is suitable for "safe electrical isolation" only within the safety limit data. Maintenance of the safety date shall be ensured by means of protective circuits.
"*" marking on packages denotes VDE 0884 approval for 560 VPEAK working voltage.

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110, for rated mains voltage			
≤ 150 Vrms		I to IV	
≤ 300 Vrms		I to III	
≤ 400 Vrms		I to II	
Climatic classification		40/85/21	
Pollution degree (DIN VDE 0110, Table 1)		2	
Maximum working insulation voltage	V_{IORM}	400	V_{PEAK}
Input to output test voltage, Method b1 $V_{IORM} \times 1.875 = V_{PR}$, 100% production test, t_m = 1sec, partial discharge < 5 pC	V_{PR}	1050	V_{PEAK}
Input to output test voltage, Method a			
(After environmental tests Subgroup 1)			
V_{IORM} x 1.6 = V_{PR}, t_m = 60 sec, partial discharge < 5 pC		896	Vpeak
(After input and/or safety test Subgroup 2/3)			
V_{IORM} x 1.2 = V_{PR}, t_m = 60 sec, partial discharge < 5 pC	V_{PR}	672	Vpeak
Highest allowable over-voltage (Transient over-voltage, t_{TR} =10 sec)	V_{TR}	4000	V_{PEAK}
Safety-limiting values (maximum value allowed in the event of a failure. See thermal derating curve, Figure 1)			
Case temperature	TS		°C
Input current	$I_{S, INPUT}$		mA
Output current	$I_{S,OUTPUT}$		mA
Insulation resistance at Ts, V_{IO} = 500 V	Rs	$>10^9$	Ω

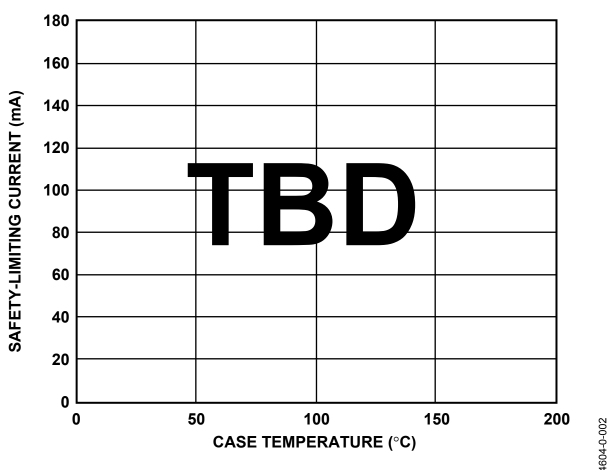

Figure 2. Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per VDE 0884.

RECOMMENDED OPERATING CONDITIONS

Table 6.All voltages are relative to their respective ground.

Parameter	Symbol	Min.	Max.	Unit
Operating temperature	T_A	-40	85	°C
Supply voltages	V_{DD1}	2.7	5.5	V
	V_{DD1}	4.75	5.25	V
Input bus voltage (separately or common mode)	V_{IB}	-7	12	V
Differential input bus magnitude	$\|V_{ID}\|$		12	V
Logic high input voltages, 5 V operation1	V_{TxDH}, V_{RTSH}, $V_{\overline{RE}H}$	0.7 V_{DD1}	V_{DD1}	V
Logic low input voltages, 5 V operation1	V_{TxDL}, V_{RTSL}, $V_{\overline{RE}L}$	0.0	0.3 V_{DD1}	V
Logic high input voltages, 3 V operation1	V_{TxDH}, V_{RTSH}, $V_{\overline{RE}H}$	0.7 V_{DD1}	V_{DD1}	V
Logic low input voltage, 3 V operation1	V_{TxDL}, V_{RTSL}, $V_{\overline{RE}L}$	0.0	0.25 $_{VDD1}$	V
Input signal rise and fall times			1.0	ms
Data rate (NRZ)	r_{BIT}	0	35	MBd

ABSOLUTE MAXIMUM RATINGS

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute maximum ratings apply individually only, not in combination.

Table 7. Ambient temperature = 25 °C unless otherwise noted. All voltages are relative to their respective ground.

Parameter	Symbol	Min.	Max.	Unit
Storage temperature	T_S	-55	150	°C
Ambient operating temperature	T_A	-40	100	°C
Supply voltages	V_{DD1},V_{DD2}	-0.5	6.5	V
Logic input voltages	V_{TxD}, V_{RTS}, $V_{\overline{RE}}$	-0.5	V_{DD1} + 0.5	V
Bus terminal voltages	A, B	-9	14	V
Logic output voltages	R×D, DE	-0.5	V_{DDO} + 0.5	V
Average output current, per pin	I_O	-35	35	mA
ESD (human body model)		-2.0	2.0	KV
Thermal impedance	Θ_{JC}		TBD	°C/W
	Θ_{JA}		105	°C/W
Lead solder temperature (hand soldering) Heating at lead tip 275°C ±10° for 20 seconds				
Solder reflow temperature profile JEDEC Standard 20A				

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TRUTH TABLES

The truth tables in this section use these abbreviations:

Letter	Description
H	High level
L	Low level
X	Irrelevant
Z	High impedance (off)
NC	Disconnected

See the Power Up/Power-Down Characteristics section for additional information.

Table 8.Transmitting

	INPUTS		OUTPUTS		
SUPPLIES	**RTS**	**T×D**	**A**	**B**	**DE**
V_{DD1} and V_{DD2} On	H	H	H	L	H
V_{DD1} and V_{DD2} On	H	L	L	H	H
V_{DD1} and V_{DD2} On	L	X	Z	Z	L
V_{DD1} and/or V_{DD2} Off	X	X	Z	Z	L

Table 9. Receiving

	INPUTS		OUTPUT
SUPPLIES	**A-B**	$\overline{RE}$	**R×D**
VDD1 and VDD2 On	> 0.2V	L or NC	H
VDD1 and VDD2 On	< -0.2V	L or NC	L
VDD1 and VDD2 On	-0.2 <A-B< 0.2	L or NC	Indeterminate
VDD1 and VDD2 On	Inputs Open	L or NC	H
VDD1 and VDD2 On	X	H	Z
VDD1 and/or VDD2 Off	X	L or NC	H

PIN CONFIGURATION

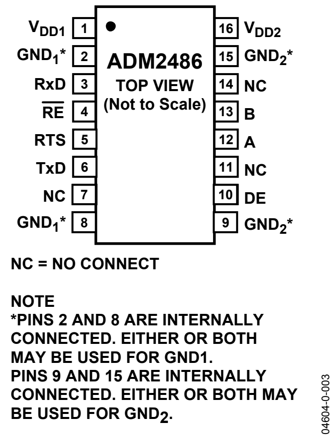

Figure 3.

Table 10.Pin Function Description

Pin(s)	Mnemonic	Function
1	V_{DD1}	Power supply, logic side
2, 8	GND_1	Ground, logic side
3	R × D	Receiver output.
4	$\overline{RE}$	Receiver enable
5	RTS	Request to send
6	TxD	Transmit data
9, 15	GND2	Ground, bus side
10	DE	Driver output enable
12	A	Noninverting receiver input/driver output
13	B	Inverting receiver input/driver output
16	V_{DD2}	Power supply, bus side

TEST CIRCUITS

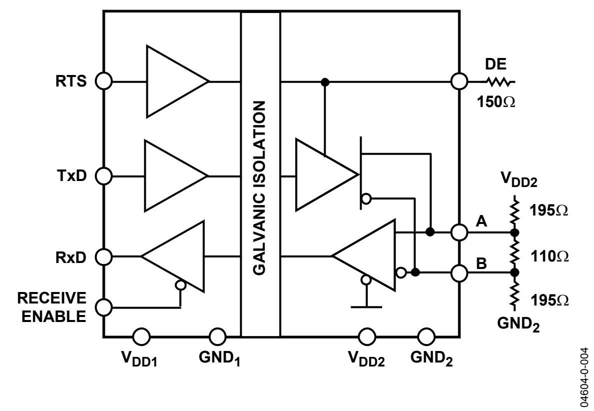

Figure 4. Supply Current Measurement Test Circuit

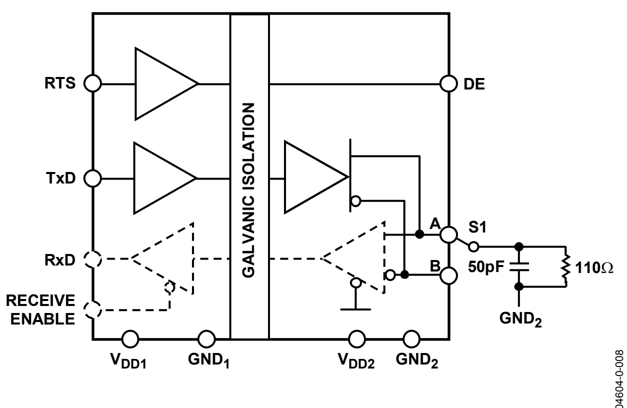

Figure 5. Driver Enable Test Circuit

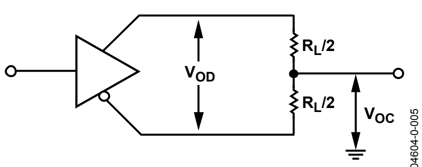

Figure 6. Driver Voltage Measurement Test Circuit

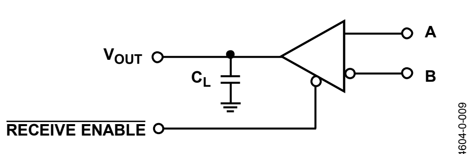

Figure 7. Receiver Propagation Delay Test Circuit

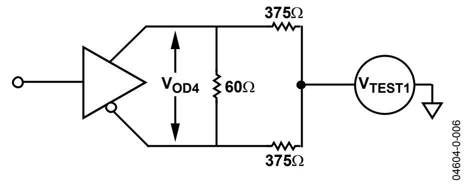

Figure 8. Driver Voltage Measurement Test Circuit

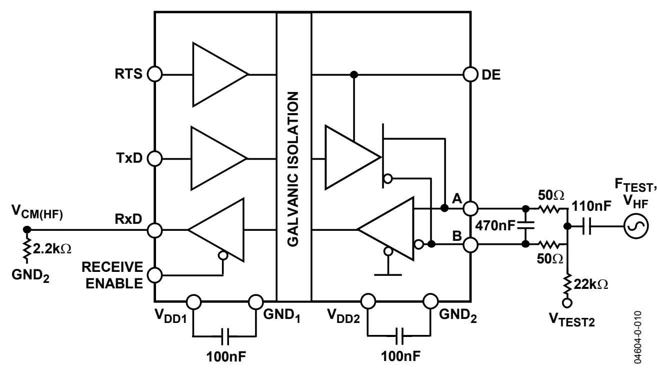

Figure 9. High Frequency Common Mode Noise Test Circuit

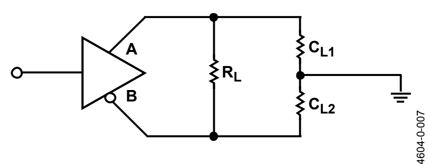

Figure 10. Driver Propagation Delay Test Circuit

SWITCHING CHARACTERISTICS

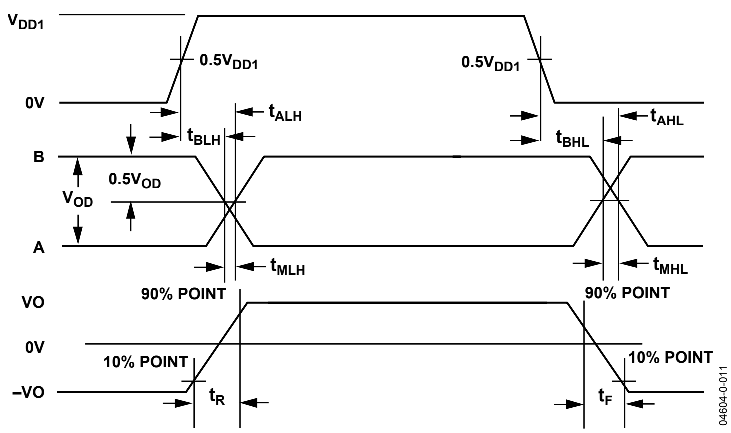

Figure 11. Driver Propagation Delay, Rise/Fall Timing

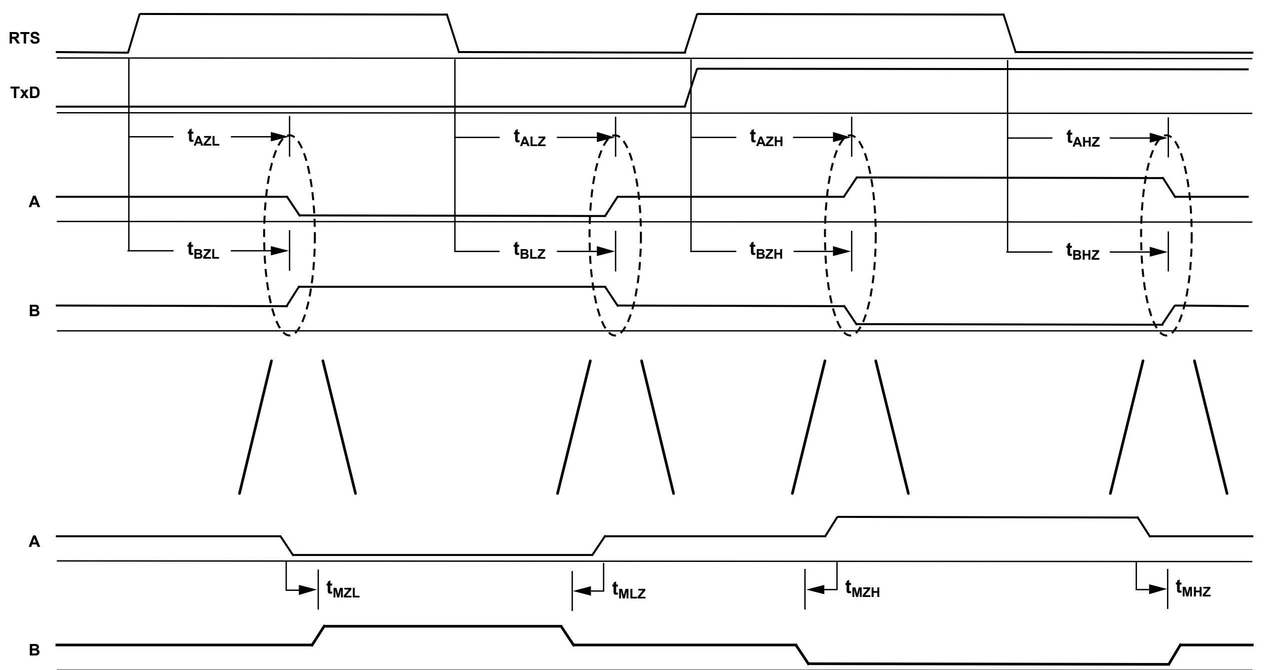

Figure 12 Driver Enable/Disable Timing

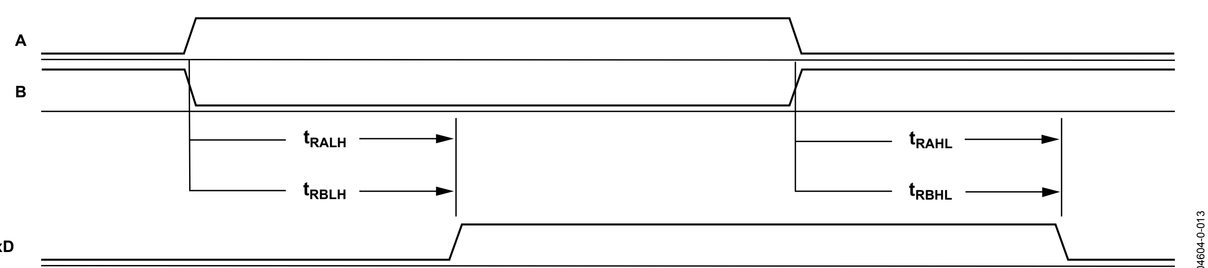

Figure 13. Receiver Propagation Delay

APPLICATION INFORMATION

POWER-UP/POWER-DOWN CHARACTERISTICS

The power-up/power-down characteristics of the ADM2486 are in accordance with the supply thresholds shown in **Table 11**. Upon power-up, the ADM2486 output signals (A, B, RxD and DE) reach their correct state once both supplies have exceeded their thresholds. Upon power-down, the ADM2486 output signals retain their correct state until at least one of the supplies drops below its power down threshold. When the VDD1 power-down threshold is crossed, the ADM2486 output signals reach their unpowered states within 4 µs.

Table 11.Power Up/Power-Down Thresholds

			Unpowered States			
Supply	**Transition**	**Threshold**	**A**	**B**	**RxD**	**DE**
VDD1	Power Up	2.0V	Z	Z	H	L
VDD1	Power Down	1.0V				
VDD2	Power Up	3.3V				
VDD2	Power Down	2.4V				

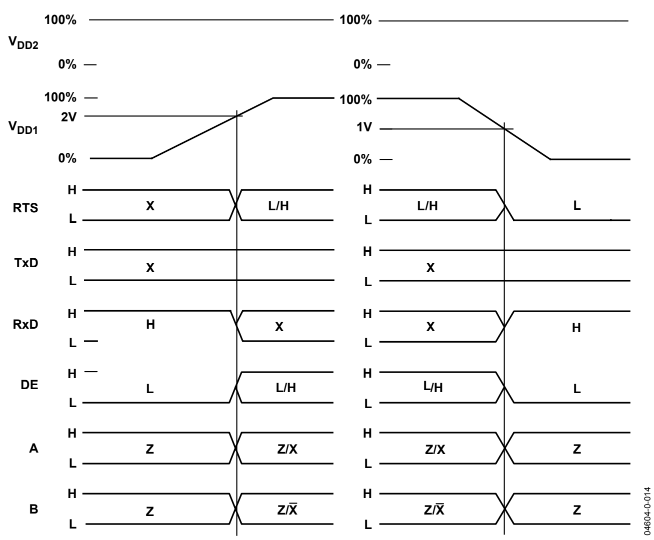

Figure 14. VDD1 Power Up/Down

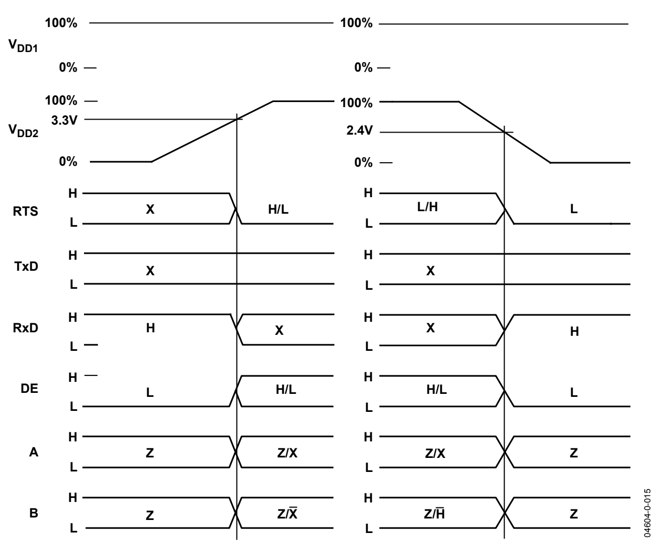

Figure 15. VDD2 Power Up/Down

THERMAL SHUTDOWN

The ADM2486 contains thermal shutdown circuitry that protects the part from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature under this condition and disables the driver outputs. This circuitry is designed to disable the driver outputs when a die temperature of 150°C is reached. As the device cools, the drivers are re-enabled at a temperature of 140°C.

RECEIVER OPEN-CIRCUIT FAIL-SAFE

The receiver input includes a fail-safe feature that guarantees a logic high RxD output when the A and B inputs are floating or open circuited.

MAGNETIC FIELD IMMUNITY

The ADM2486 is immune to external magnetic fields. The ADM2486's magnetic field immunity is set by the condition in which induced voltage in the transformer's receiving coil is sufficiently large to either falsely set or reset the Decoder. The analysis below defines the conditions under which this may occur. The ADM2486's 3 V operating condition is examined as it represents the most susceptible mode of operation.

The pulses at the transformer output are greater than 1.0 V in amplitude. The Decoder has sensing thresholds at about 0.5 V, therefore establishing a 0.5 V margin in which induced voltages can be tolerated. The induced voltage induced across the receiving coil is given by $V = (-d\ /dt)\ rn2;\ n = 1,2,\ldots,N$ where:

β = magnetic flux density (Gauss)

N = number of turns in receiving coil

r_n = radius of nth turn in receiving coil (cm)

Given the geometry of the receiving coil and an imposed requirement that the induced voltage be at most 50% of the 0.5 V margin at the Decoder, a maximum allowable magnetic field is calculated as shown in Figure 16.

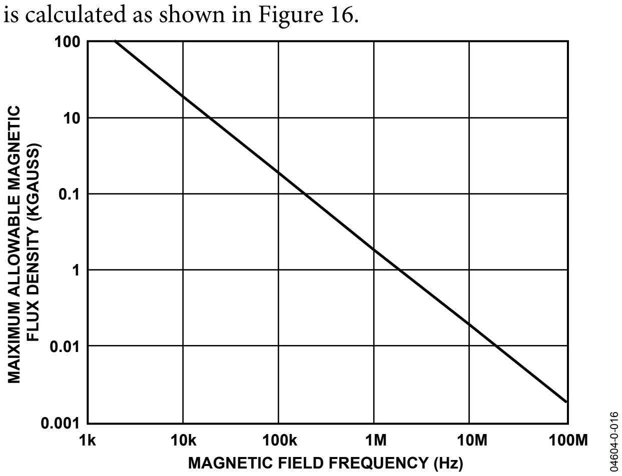

Figure 16. Maximum Allowable External Magnetic Flux Density.

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 KGauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurred during a transmitted pulse (and was of the worst-case polarity) it would reduce the received pulse from > 1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the Decoder.

As a convenience to the user, the above magnetic flux density values are shown below in terms of more familiar quantities such as maximum allowable current flow at given distances away from the ADM2486 transformers.

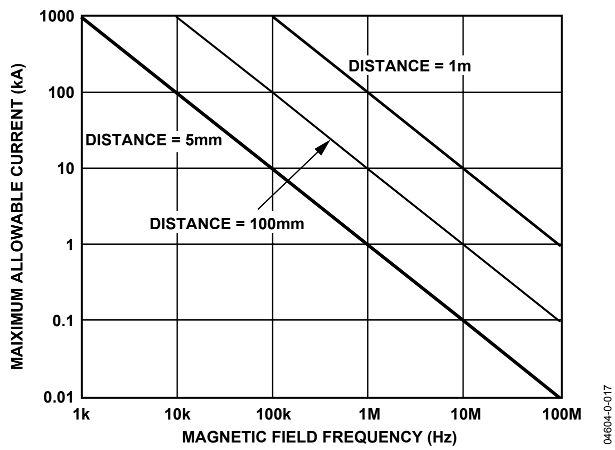

Figure 17. Maximum Allowable Current for Various Current-to-ADM2486 Spacings.

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces could induce sufficiently large error voltages to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

OUTLINE DIMENSIONS

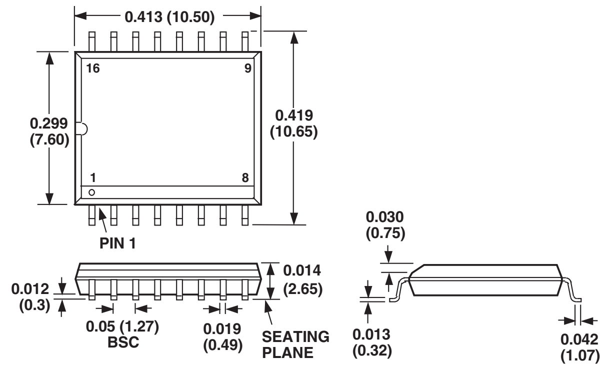

Figure 18. 16-Lead Wide-Body Small Outline Package [SOIC]

(RW-16)

Dimensions shown in millimeters

ORDERING GUIDE

Model	Max. Data Rate (Mbps)	Temperature Range	Package Description	Package Option
ADM2486BRW	35	−40°C to +85°C	16-Lead Wide Body SOIC	

The addition of an "-RL" suffix designates a 13" (1000 units) tape and reel option.

.

PR04604-0-2/04(PrA)