# 54F/74F175

## Quad D Flip-Flop

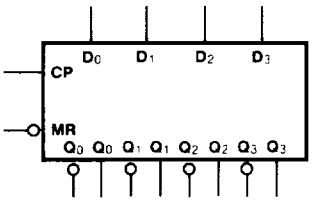
### Description

The 'F175 is a high-speed quad D flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

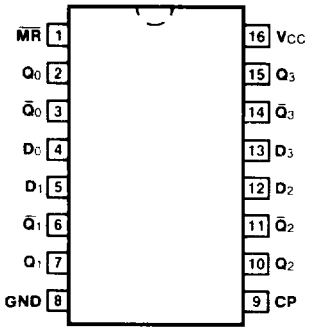
- **Edge-Triggered D-Type Inputs**
- **Buffered Positive Edge-Triggered Clock**
- **Asynchronous Common Reset**
- **True and Complement Output**

**Ordering Code:** See Section 5

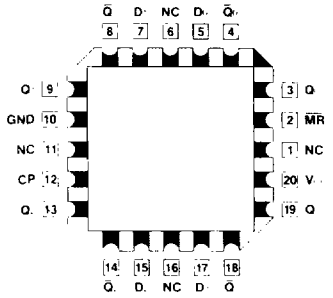
### Logic Symbol




### Connection Diagrams




**Pin Assignment for DIP and SOIC**




**Pin Assignment for LCC and PCC**

**Input Loading/Fan-Out:** See Section 3 for U.L. definitions

| Pin Names | Description | 54F/74F(U.L.) HIGH/LOW |
|---|---|---|
| $D_0$-$D_3$ | Data Inputs | 0.5/0.375 |
| CP | Clock Pulse Input (Active Rising Edge) | 0.5/0.375 |
| $\overline{MR}$ | Master Reset Input (Active LOW) | 0.5/0.375 |
| $Q_0$-$Q_3$ | True Outputs | 25/12.5 |
| $\overline{Q}_0$-$\overline{Q}_3$ | Complement Outputs | 25/12.5 |

## Functional Description

The 'F175 consists of four edge-triggered D flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and $\overline{Q}$ outputs to follow. A LOW input on the Master Reset ($\overline{MR}$) will force all Q outputs LOW and $\overline{Q}$ outputs HIGH independent of Clock or Data inputs. The 'F175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

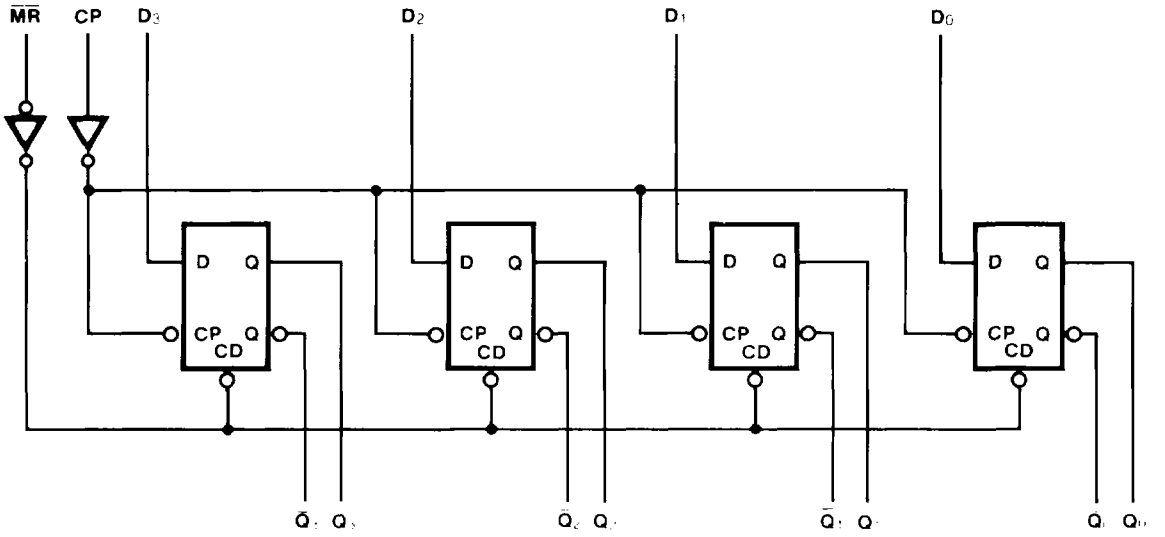
## Truth Table

| Inputs | Outputs | |
|---|---|---|
| $@t_n$, $\overline{MR} = H$ | $@t_{n+1}$ | |
| $D_n$ | $Q_n$ | $\overline{Q}_n$ |
| L | L | H |
| H | H | L |

H = HIGH Voltage Level
L = LOW Voltage Level
$t_n$ = Bit Time before Clock Pulse
$t_{n+1}$ = Bit Time after Clock Pulse

4

## Logic Diagram




Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## DC Characteristics over Operating Temperature Range (unless otherwise specified)

| Symbol | Parameter | 54F/74F | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| $I_{CC}$ | Power Supply Current | | 22.5 | 34.0 | mA | $V_{CC}$ = Max<br>$D_n$ = $\overline{MR}$ = HIGH<br>CP = ⨍ |

**AC Characteristics:** See Section 3 for waveforms and load configurations

| Symbol | Parameter | 54F/74F | | | 54F | | 74F | | Units | Fig. No. |
|---|---|---|---|---|---|---|---|---|---|---|
| | | $T_A = +25°C$ $V_{CC} = +5.0\ V$ $C_L = 50\ pF$ | | | $T_A$, $V_{CC}$ = Mil $C_L = 50\ pF$ | | $T_A$, $V_{CC}$ = Com $C_L = 50\ pF$ | | | |
| | | Min | Typ | Max | Min | Max | Min | Max | | |
| $f_{max}$ | Maximum Clock Frequency | 100 | 140 | | 100 | | 100 | | MHz | 3-1 |
| $t_{PHL}$<br>$t_{PLH}$ | Propagation Delay<br>CP to $Q_n$ or $\overline{Q}_n$ | 4.0<br>4.0 | 5.0<br>6.5 | 6.5<br>8.5 | 3.5<br>4.0 | 8.5<br>10.5 | 4.0<br>4.0 | 7.5<br>9.5 | ns | 3-1<br>3-7 |
| $t_{PHL}$ | Propagation Delay<br>$\overline{MR}$ to $Q_n$ | 4.5 | 9.0 | 11.5 | 4.5 | 15.0 | 4.5 | 13.0 | ns | 3-1<br>3-11 |
| $t_{PLH}$ | Propagation Delay<br>$\overline{MR}$ to $\overline{Q}_n$ | 4.0 | 6.5 | 8.5 | 4.0 | 10.0 | 4.0 | 9.0 | ns | 3-1<br>3-11 |

**AC Operating Requirements:** See Section 3 for waveforms

| Symbol | Parameter | 54F/74F | | | 54F | | 74F | | Units | Fig. No. |
|---|---|---|---|---|---|---|---|---|---|---|
| | | $T_A = +25°C$ $V_{CC} = +5.0\ V$ | | | $T_A$, $V_{CC}$ = Mil | | $T_A$, $V_{CC}$ = Com | | | |
| | | Min | Typ | Max | Min | Max | Min | Max | | |
| $t_s(H)$<br>$t_s(L)$ | Setup Time, HIGH or LOW<br>$D_n$ to CP | 3.0<br>3.0 | | | 3.0<br>3.0 | | 3.0<br>3.0 | | ns | 3-5 |
| $t_h(H)$<br>$t_h(L)$ | Hold Time, HIGH or LOW<br>$D_n$ to CP | 1.0<br>1.0 | | | 1.0<br>1.0 | | 1.0<br>1.0 | | | |
| $t_w(H)$<br>$t_w(L)$ | CP Pulse Width<br>HIGH or LOW | 4.0<br>5.0 | | | 4.0<br>5.0 | | 4.0<br>5.0 | | ns | 3-7 |
| $t_w(L)$ | $\overline{MR}$ Pulse Width, LOW | 5.0 | | | 5.0 | | 5.0 | | ns | 3-11 |
| $t_{rec}$ | Recovery Time, $\overline{MR}$ to CP | 5.0 | | | 5.0 | | 5.0 | | ns | 3-11 |