P54/74FCT833AT/BT/CT—P54/74FCT834AT/BT/CT
P54/74FCT853AT/BT/CT—P54/74FCT854AT/BT/CT
FAST CMOS PARITY BUS TRANSCEIVER

FEATURES

- Function, Pinout and Drive Compatible with the FCT, F and AM29833/853 Logic
- FCT-C speed at 5.3ns max. (Com'l)
  FCT-B speed at 7.0ns max. (Com'l)
- Reduced V_{OH} (typically = 3.3V) versions of Equivalent and FCT functions
- Edge-rate Control Circuitry for Significantly Improved Noise Characteristics
- ESD protection exceeds 2000V
- Power-off disable feature
- Matched Rise and Fall times
- Fully Compatible with TTL Input and Output Logic Levels
- 64 mA Sink Current (Com'l), 32 mA (Mil)
  15 mA Source Current (Com'l), 12 mA (Mil)
- Manufactured in 0.7 micron PACE Technology™

DESCRIPTION

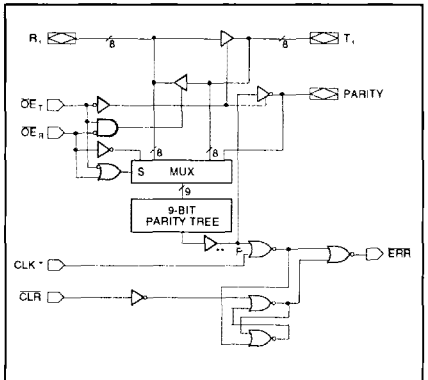
The 'FCT833T, 'FCT834T, 'FCT853T and 'FCT854T are high-performance bus transceivers designed for two-way communications. They contain an 8-bit data path from the R (port) to the T (port), an 8-bit data path from the T (port) to the R (port), and a 9-bit parity checker/generator. In the 'FCT833T and 'FCT834T, the error flag is clocked and stored in a register which is read at the open-drain $\overline{ERR}$ output. The $\overline{CLR}$ input is used to clear the error flag register. In the 'FCT853T and 'FCT854T, a latch replaces this register, and the $\overline{EN}$ and $\overline{CLR}$ controls are used to pass, store, sample or clear the error flag output. When both output enables are disabled, parity logic defaults to the transmit mode, so that the $\overline{ERR}$ pin reflects the parity of the R port. The output enable $\overline{OE}_T$ and $\overline{OE}_R$ are used to force the port outputs to the high impedance state so that the device can drive bus lines directly. In addition, $\overline{OE}_T$ and $\overline{OE}_R$ can be used to force a parity error by enabling both lines simultaneously. This transmission of inverting parity gives the designer more system diagnostic capability. The 'FCT833T and 'FCT834T are non-inverting, while the 'FCT853T and 'FCT854T present inverted data at the outputs.

The 'FCT833T,FCT834T,FCT853T and 'FCT854T are manufacturered using PACE Technology™ which is Performance Advanced CMOS Engineered to use 0.7 micron effective channel lengths resulting in 400 picoseconds loaded* internal gate delays. PACE Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection and single event upset protection, and is supported by a Class 1 environment volume production facility.

* For a fan-in/fan-out of 4 at 85°C junction temperature and 5.0 V supply. For a fan-in/fan-out of 1, the internal gate delay is 200 picoseconds at room temperature.

7

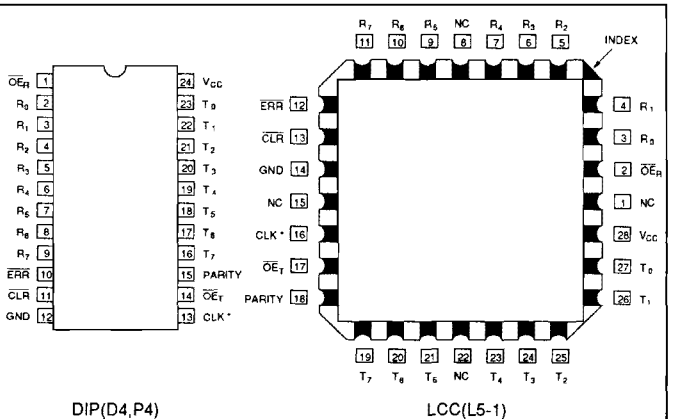
FUNCTIONAL BLOCK DIAGRAM



* $\overline{EN}$ on 'FCT853T and 'FCT854T
** 'FCT834T and 'FCT854T have inverting buffer

1722 01

PIN CONFIGURATIONS



DIP(D4,P4)
SOIC(S4)

LCC(L5-1)

* $\overline{EN}$ on 'FCT853T and 'FCT854T

1722 02

PIN DESCRIPTION

Pin No.	Name	I/O	Description
1	$\overline{OE}_R$	I	RECEIVE enable input.
2–9	R_i	I/O	8-bit RECEIVE data output.
10	$\overline{ERR}$	O	Output from fault registers. Registers detection of odd parity fault on using clock edge (CLK). A registered $\overline{ERR}$ output remains low until cleared. Open drain output, requires pull up resistor.
11	$\overline{CLR}$	O	Clears the fault register output.
16–23	T_i	I/O	8-bit TRANSMIT data output.
15	PARITY	I/O	1-bit PARITY output.
14	$\overline{OE}_T$	I	TRANSMIT enable input.
13 for 'FCT833T 'FCT834T	CLK	I	External clock pulse input for fault register flag.
13 for 'FCT853T 'FCT854T	$\overline{EN}$	I	Latch enable for the Error Flag latch.

1722 Tbl 01

FUNCTION TABLE — 'FCT833T (NONINVERTING)

Inputs						Outputs				Function
$\overline{OE}_T$	$\overline{OE}_R$	$\overline{CLR}$	CLK	R_i (Σ of H'S)	T_i Incl PARITY (Σ of H'S)	R_i	T_i	PARITY	$\overline{ERR}$(1)	
L	H	–	–	H (Odd)	NA	NA	H	L	NA	Transmit data from R Port to T Port with parity; receiving path is disabled.
L	H	–	–	H (Even)	NA	NA	H	H	NA	
L	H	–	–	L (Odd)	NA	NA	L	L	NA	
L	H	–	–	L (Even)	NA	NA	L	H	NA	
H	L	H	⌐	NA	H (Odd)	H	NA	NA	H	Receive data from T Port to R Port with parity test resulting in flag; transmitting path is disabled.
H	L	H	⌐	NA	H (Even)	H	NA	NA	L	
H	L	H	⌐	NA	L (Odd)	L	NA	NA	H	
H	L	H	⌐	NA	L (Even)	L	NA	NA	L	
–	–	L	–	–	–	–	NA	NA	H	Clear the state of error flag register.
H	H	H	–	–	–	Z	Z	Z	NC	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
H	H	L	–	–	–	Z	Z	Z	H	
H	H	H	⌐	L (Odd)	–	Z	Z	Z	H	
H	H	H	⌐	H (Even)	–	Z	Z	Z	L	
L	L	–	–	H (Odd)	NA	NA	H	H	NA	Forced-error checking.
L	L	–	–	H (Even)	NA	NA	H	L	NA	
L	L	–	–	L (Odd)	NA	NA	L	H	NA	
L	L	–	–	L (Even)	NA	NA	L	L	NA	

1722 Tbl 02

FUNCTION TABLE — 'FCT834T (INVERTING[2])

Inputs						Outputs				Function
$\overline{OE}_T$	$\overline{OE}_R$	$\overline{CLR}$	CLK	R_i (Σ of H'S)	T_i Incl PARITY (Σ of H'S)	R_i	T_i	PARITY	$\overline{ERR}$(1)	
L	H	–	–	H (Odd)	NA	NA	L	H	NA	Transmit data from R Port to T Port with parity; receiving path is disabled.
L	H	–	–	H (Even)	NA	NA	L	L	NA	
L	H	–	–	L (Odd)	NA	NA	H	H	NA	
L	H	–	–	L (Even)	NA	NA	H	L	NA	
H	L	H	⌐	NA	H (Odd)	L	NA	NA	H	Receive data from T Port to R Port with parity test resulting in flag; transmitting path is disabled.
H	L	H	⌐	NA	H (Even)	L	NA	NA	L	
H	L	H	⌐	NA	L (Odd)	H	NA	NA	H	
H	L	H	⌐	NA	L (Even)	H	NA	NA	L	
–	–	L	–	–	–	–	–	–	H	Clear the state of error flag register.
H	H	H	–	–	–	Z	Z	Z	NC	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
H	H	L	–	–	–	Z	Z	Z	H	
H	H	H	⌐	L (Odd)	–	Z	Z	Z	L	
H	H	H	⌐	L (Even)	–	Z	Z	Z	H	
L	L	–	–	H (Odd)	NA	NA	L	L	NA	Forced-error checking.
L	L	–	–	H (Even)	NA	NA	L	H	NA	
L	L	–	–	L (Odd)	NA	NA	H	L	NA	
L	L	–	–	L (Even)	NA	NA	H	H	NA	

1722 Tbl 03

H = High
L = Low
NC = No Change

Z = High Impedance
NA = Not Applicable
– = Don't care or irrelevant

Odd = Odd number of logic one's
Even = Even number of logic one's
i = 0, 1, 2, 3, 4, 5, 6, 7
⌐ = Low to High transition of clock

Notes:
1. Output state assumes HIGH output pre-state.
2. For the negative logic levels on the B Port, an "H" represents a logic "0" while an "L" represents a logic "1."

FUNCTION TABLE — 'FCT853T (NONINVERTING)

Inputs						Outputs				Function
$\overline{OE}_T$	$\overline{OE}_R$	$\overline{CLR}$	CLK	R_i (Σ of H'S)	T_i Incl PARITY (Σ of H'S)	R_i	T_i	PARITY	$\overline{ERR}^{(1)}$	
L	H	–	–	H (Odd)	NA	NA	H	L	NA	Transmit data from R Port to T Port with parity; receiving path is disabled.
L	H	–	–	H (Even)	NA	NA	H	H	NA	
L	H	–	–	L (Odd)	NA	NA	L	L	NA	
L	H	–	–	L (Even)	NA	NA	L	H	NA	
H	L	L	L	NA	H (Odd)	H	NA	NA	H	Receive data from T Port to R Port with parity test resulting in flag; transmitting path is disabled.
H	L	L	L	NA	H (Even)	H	NA	NA	L	
H	L	L	L	NA	L (Odd)	L	NA	NA	H	
H	L	L	L	NA	L (Even)	L	NA	NA	L	
H	L	H	L	NA	H (Odd)	H	NA	NA	H	Receive data from T Port to R Port, pass the error test resulting in error flag; transmitting path is disabled.
H	L	H	L	NA	H (Even)	H	NA	NA	L	
H	L	H	L	NA	L (Odd)	L	NA	NA	H	
H	L	H	L	NA	H (Even)	L	NA	NA	L	
H	L	H	H	NA	–	–	NA	NA	$\overline{ERR}_{n-1}$	Store the state of error flag register.
–	–	L	H	–	–	–	NA	NA	H	Clear the state of error flag register.
H	H	H	H	–	–	Z	Z	Z	NC	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
H	H	L	H	–	–	Z	Z	Z	H	
H	H	–	L	L (Odd)	–	Z	Z	Z	H	
H	H	–	L	H (Even)	–	Z	Z	Z	L	
L	L	–	–	H (Odd)	NA	NA	H	H	NA	Forced-error checking.
L	L	–	–	H (Even)	NA	NA	H	L	NA	
L	L	–	–	L (Odd)	NA	NA	L	H	NA	
L	L	–	–	L (Even)	NA	NA	L	L	NA	

1722 Tbl 04

H = High
L = Low
NC = No Change

Z = High Impedance
NA = Not Applicable
$\overline{ERR}_{n-1}$ = Pre-state of $\overline{ERR}$
– = Don't care or irrelevant

Odd = Odd number of logic one's
Even = Even number of logic one's
i = 0, 1, 2, 3, 4, 5, 6, 7
⌐ = Low to High transition of clock

Note:
1. Output state assumes HIGH output pre-state.

FUNCTION TABLE — 'FCT854T (INVERTING[2])

Inputs						Outputs				Function
$\overline{OE}_T$	$\overline{OE}_R$	$\overline{CLR}$	CLK	R_i (Σ of H'S)	T_i Incl PARITY (Σ of H'S)	R_i	T_i	PARITY	$\overline{ERR}$[1]	
L	H	–	–	H (Odd)	NA	NA	L	H	NA	Transmit data from R Port to T Port with parity; receiving path is disabled.
L	H	–	–	H (Even)	NA	NA	L	L	NA	
L	H	–	–	L (Odd)	NA	NA	H	H	NA	
L	H	–	–	L (Even)	NA	NA	H	L	NA	
H	L	L	L	NA	H (Odd)	L	NA	NA	H	Receive data from T Port to R Port with parity test resulting in flag; transmitting path is disabled.
H	L	L	L	NA	H (Even)	L	NA	NA	L	
H	L	L	L	NA	L (Odd)	H	NA	NA	H	
H	L	L	L	NA	L (Even)	H	NA	NA	L	
H	L	H	L	NA	H (Odd)	L	NA	NA	H	Receive data from T Port to R Port, pass the error test resulting in error flag; transmitting path is disabled.
H	L	H	L	NA	H (Even)	L	NA	NA	L	
H	L	H	L	NA	L (Odd)	H	NA	NA	H	
H	L	H	L	NA	L (Even)	H	NA	NA	L	
H	L	H	H	NA	–	–	NA	NA	$\overline{ERR}_{n-1}$	Store the state of error flag register.
–	–	L	H	–	–	–	NA	NA	H	Clear the state of error flag register.
H	H	H	H	–	–	Z	Z	Z	NC	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode.
H	H	L	H	–	–	Z	Z	Z	H	
H	H	–	L	L (Odd)	–	Z	Z	Z	L	
H	H	–	L	L (Even)	–	Z	Z	Z	H	
L	L	–	–	H (Odd)	NA	NA	L	L	NA	Forced-error checking.
L	L	–	–	H (Even)	NA	NA	L	H	NA	
L	L	–	–	L (Odd)	NA	NA	H	L	NA	
L	L	–	–	L (Even)	NA	NA	H	H	NA	

1722 Tbl 05

H = High
L = Low
NC = No Change

Z = High Impedance
NA = Not Applicable
$\overline{ERR}_{n-1}$ = Pre-state of $\overline{ERR}$
– = Don't care or irrelevant

Odd = Odd number of logic one's
Even = Even number of logic one's
i = 0, 1, 2, 3, 4, 5, 6, 7
⌐ = Low to High transition of clock

Notes:
1. Output state assumes HIGH output pre-state.
2. For the negative logic levels on the B Port, an "H" represents a logic "0" while an "L" represents a logic "1."

7

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

1722 Tbl 06

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	–0.5 to +7.0	V

1722 Tbl 07

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

1722 Tbl 08

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1722 Tbl 09

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis[3]			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = –15mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = –24mA
V_{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	I_{OL} = 32mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 48mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 64mA
I_I	Input HIGH Current				20	µA	MAX	$V_{IN} = V_{CC}$
I_{IH}	Input HIGH Current (Except I/O Pins)				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current (Except I/O Pins)				–5	µA	MAX	V_{IN} = 0.5V
I_{IH}	Input HIGH Current (I/O Pins only)				15	µA	MAX	V_{OUT} = 2.7V
I_{IL}	Input LOW Current (I/O Pins only)				15	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120	–225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
$C_{I/O}$	I/O Capacitance[3]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC}-0.2V$

1722 Tbl 10

Notes:

1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{os} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ mHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}_T$ = GND, $\overline{OE}_R$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$,
I_C	Total Power Supply Current[5]	1.4	3.4	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling, f_0 = 10MHz, $\overline{OE}_T$ = GND, $\overline{OE}_R$ = V_{CC}, f_1 = 2.5MHz, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC}$ -0.2V
		1.9	5.4	mA	V_{CC} = MAX 50% Duty Cycle, Outputs Open, One Bit Toggling, f_0 = 10MHz, $\overline{OE}_T$ = GND, $\overline{OE}_R$ = V_{CC}, f_1 = 2.5MHz, V_{IN} = 3.4V or V_{IN} = GND
		4.0	7.8[4]	mA	V_{CC} = MAX 50% Duty Cycle, Outputs Open, Eight Bits Toggling, f_0 = 10MHz, $\overline{OE}_T$ = GND, $\overline{OE}_R$ = V_{CC}, f_1 = 2.5MHz, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		6.2	16.8[4]	mA	V_{CC} = MAX 50% Duty Cycle, Outputs Open, Eight Bits Toggling, f_0 = 10MHz, $\overline{OE}_T$ = GND, $\overline{OE}_R$ = V_{CC}, f_1 = 2.5MHz, V_{IN} = 3.4V or V_{IN} GND

1722 Tbl 11

Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

7

AC CHARACTERISTICS

Sym.	Parameter	Test Conditions	'FCT833AT/853AT 'FCT834AT/854AT				'FCT833BT/853BT 'FCT834BT/854BT				'FCT833CT/853CT 'FCT834CT/854CT				Units	Fig. No.
			MIL		COM'L		MIL		COM'L		MIL		COM'L			
			Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.		
t_{PLH} t_{PHL}	Propagation Delay R_i to T_i, T_i to R_i	C_L = 50pF	–	14.0	–	10.0	–	10.0	–	7.0	–	7.0	–	5.3	ns	1,5
t_{PLH} t_{PHL}	Propagation Delay R_i to T_i, T_i to R_i	C_L = 300pF[2]	–	21.5	–	17.5	–	17.5	–	14.5	–	15.0	–	13.0	ns	1,5
t_{PLH} t_{PHL}	Propagation Delay R_i to PARITY	C_L = 50pF	–	20.0	–	15.0	–	14.0	–	10.5	–	10.9	–	8.9	ns	1,5
t_{PLH} t_{PHL}	Propagation Delay R_i to PARITY	C_L = 300pF[2]	–	27.5	–	22.5	–	21.5	–	18.0	–	18.5	–	16.5	ns	1,5
t_{PLH} t_{PHL}	Propagation Delay $\overline{OE}_R$ to PARITY	C_L = 50pF	–	20.0	–	15.0	–	14.0	–	10.5	–	10.9	–	8.9	ns	1,5
t_{PLH} t_{PHL}	Propagation Delay $\overline{OE}_R$ to PARITY	C_L = 300pF[2]	–	27.5	–	22.5	–	21.5	–	18.0	–	18.0	–	16.5	ns	1,5
t_{PHL}	Propagation Delay CLK[3] to $\overline{ERR}$	C_L = 50pF	–	16.0	–	12.0	–	11.0	–	8.5	–	9.2	–	7.2	ns	1,5
t_{PLH}	Propagation Delay $\overline{CLR}$ to $\overline{ERR}$	C_L = 50pF	–	20.0	–	16.0	–	18.0	–	15.0	–	14.8	–	12.8	ns	1,5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}_R$, $\overline{OE}_T$ to R_i, T_i	C_L = 50pF	–	16.0	–	12.0	–	11.0	–	8.5	–	9.2	–	7.2	ns	1,7,8
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}_R$, $\overline{OE}_T$ to R_i, T_i	C_L = 300pF[2]	–	23.5	–	19.5	–	18.5	–	16.0	–	16.5	–	14.5	ns	1,7,8
t_{PZH} t_{PZL}	Output Disable Time $\overline{OE}_R$, $\overline{OE}_T$ to R_i, T_i	C_L = 50pF	–	16.0	–	12.0	–	11.0	–	8.5	–	9.4	–	7.4	ns	1,7,8
t_{PZH} t_{PZL}	Output Disable Time $\overline{OE}_R$, $\overline{OE}_T$ to R_i, T_i	C_L = 5pF[2]	–	14.7	–	10.7	–	9.8	–	7.2	–	8.2	–	6.2	ns	1,7,8

1722 Tbl 12

AC OPERATING REQUIREMENTS

Sym.	Parameter	Test Conditions	'FCT833AT/853AT 'FCT834AT/854AT				'FCT833BT/853BT 'FCT834BT/854BT				'FCT833CT/853CT 'FCT834CT/854CT				Units	Fig. No.
			MIL		COM'L		MIL		COM'L		MIL		COM'L			
			Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max.	Min.[1]	Max		
t_{SU}	T_i PARITY to CLK[3] Set-up Time	C_L = 50pF	16.0	–	12.0	–	11.0	–	8.5	–	9.0	–	7.3	–	ns	4
t_{SU}	Clear Recovery Time $\overline{CLR}$ to CLK[3]		20.0	–	15.0	–	14.0	–	10.5	–	12.0	–	8.9	–	ns	4
t_H	T_i PARITY to CLK[3] Hold Time		0	–	0	–	0	–	0	–	0	–	0	–	ns	4
t_w(H) t_w(L)	Clock Pulse Width[4] HIGH or LOW		9.5	–	7.0	–	7.0	–	5.5	–	6.0	–	5.0	–	ns	5
t_w(L)	Clear Pulse Width LOW		9.5	–	7.0	–	7.0	–	5.5	–	6.0	–	5.0	–	ns	5

1722 Tbl 13

Notes:

1. Minimum limits are guaranteed but not tested on Propagation Delays.
2. These parameters are guaranteed but not tested.
3. $\overline{EN}$ for 'FCT853AT/BT/CT.
4. Latch Enable Width Low for 'FCT853AT/BT/CT.

ERROR FLAG OUTPUT TRUTH TABLES

'FCT853T/'FCT834T

Inputs		Internal To Device	Outputs Pre-State	Output	Function
$\overline{EN}$	$\overline{CLR}$	Point "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	
L	L	L	–	L	Pass
L	L	H	–	H	
L	H	L	–	L	Sample
L	H	–	L	L	(1's
L	H	H	H	H	Capture)
H	L	–	–	H	Clear
H	H	–	L	L	Store
H	H	–	H	H	

1722 Tbl 11

$\overline{OE}_T$ is HIGH and $\overline{OE}_n$ is LOW.

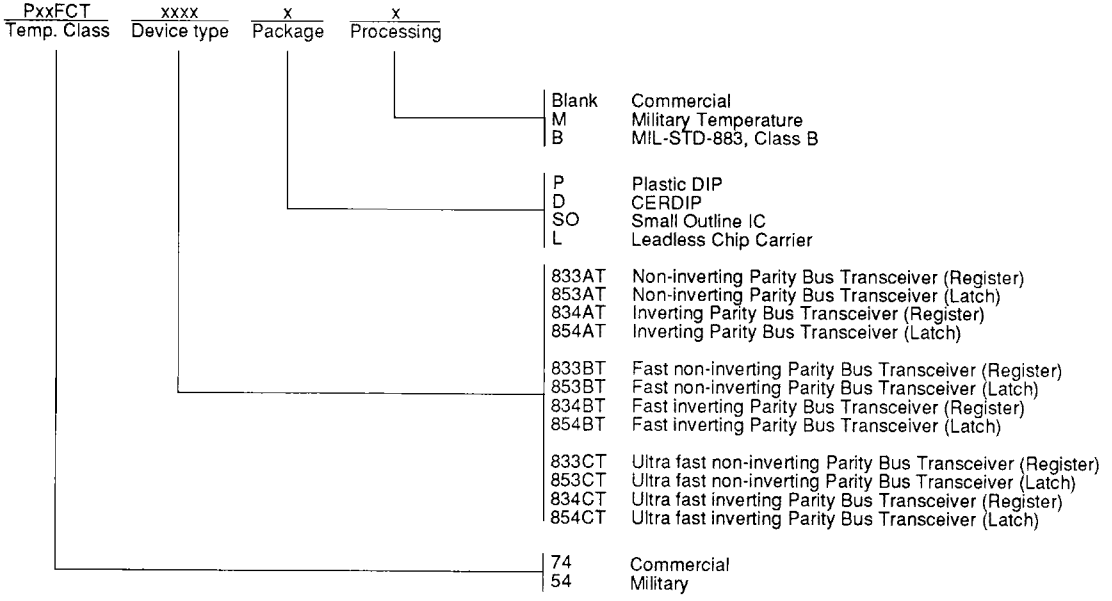
'FCT833T/'FCT834T

Inputs		Internal To Device	Outputs Pre-State	Output	Function
$\overline{CLR}$	CLK	Point "P"	$\overline{ERR}_{n-1}$	$\overline{ERR}$	
H	⌐	H	H	H	Sample
H	⌐	–	L	L	(1's
H	⌐	L	–	L	Capture)
L	–	–	–	H	Clear

1722 Tbl 12

Notes:
1. $\overline{OE}_T$ is HIGH and $\overline{OE}_n$ is LOW.
2. H = High
   L = Low
   – = Don't care or irrelevant
   ⌐ = Low to High transition of clock

ORDERING INFORMATION



1722 03

7