

CD54AC139/3A CD54ACT139/3A

SWITCHING CHARACTERISTICS: AC Series; $t_r, t_f = 3 \text{ ns}$, $C_L = 50 \text{ pF}$ (Worst Case)

CHARACTERISTICS	SYMBOL	V _{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delays A0, A1 to Outputs	t_{PLH} t_{PHL}	1.5	—	131	ns
		3.3*	4.4	14.7	
		5†	3.2	10.5*	
E to Outputs	t_{PLH} t_{PHL}	1.5	—	131	ns
		3.3	1.9	14.7	
		5	1.6	10.5*	
Power Dissipation Capacitance	C _{PD} §	—	83 Typ.		pF
Input Capacitance	C _I	—	—	10	pF

SWITCHING CHARACTERISTICS: ACT Series; $t_r, t_f = 3 \text{ ns}$, $C_L = 50 \text{ pF}$ (Worst Case)

CHARACTERISTICS	SYMBOL	V _{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delays A0, A1 to Outputs	t_{PLH} t_{PHL}	5†	3.5	11.5*	ns
E to Outputs	t_{PLH} t_{PHL}	5	3.6	12*	ns
Power Dissipation Capacitance	C _{PD} §	—	83 Typ.		pF
Input Capacitance	C _I	—	—	10	pF

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

(Limits with black dots (•) are tested 100%.)

§C_{PD} is used to determine the dynamic power consumption per decoder/demultiplexer.

For AC, $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$

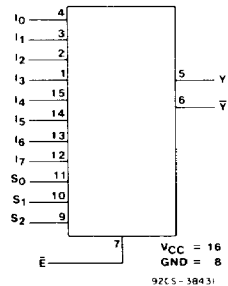
For ACT, $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency
 C_L = output load capacitance
 V_{CC} = supply voltage

CD54AC151/3A CD54ACT151/3A

8-Input Multiplexer

The RCA CD54AC151/3A and CD54ACT151/3A are 8-input digital multiplexers that utilize the new RCA ADVANCED CMOS LOGIC technology. They have three binary control inputs (S0, S1, and S2) and an active-LOW Enable (E) input. The three binary inputs select 1 of 8 channels. The output is both inverting (Y) and non-inverting (Y).

The CD54AC151/3A and CD54ACT151/3A are supplied in 16-lead dual-in-line ceramic packages (F suffix).



Package Specifications

See Section 11, Fig. 11

FUNCTIONAL DIAGRAM & TERMINAL ASSIGNMENT

CD54AC151/3A

CD54ACT151/3A

Static Electrical Characteristics (Limits with black dots (*) are tested 100%.)

CHARACTERISTICS	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A) - °C				UNITS	
				+25		-55 to +125			
	V_i (V)	I_o (mA)		MIN.	MAX.	MIN.	MAX.		
Quiescent Supply Current (MSI)	I_{CC}	V_{CC} or GND	0	5.5	—	8*	—	160*	μA

The complete static electrical test specification consists of the above by-type static tests combined with the standard static tests in the beginning of this section.

ACT INPUT LOADING TABLE

INPUT	UNIT LOAD*
I (All)	1
E	1
S	1

*Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

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Burn-In Test-Circuit Connections (Use Static II for /3A burn-in and Dynamic for Life Test.)

Static	STATIC BURN-IN I			STATIC BURN-IN II		
	OPEN	GROUND	V_{CC} (6V)	OPEN	GROUND	V_{CC} (6V)
CD54AC/ACT151	5,6	1-4,7-15	16	5,6	8	1-4,7,9-16
Dynamic	OPEN	GROUND	$1/2 V_{CC}$ (3V)	V_{CC} (6V)	OSCILLATOR	
CD54AC/ACT151	1,3,7-9, 12-15	5,6	2,4,16	11	50 kHz 25 kHz	—

NOTE: Each pin except V_{CC} and Gnd will have a resistor of 2k-47k ohms.

CD54AC151/3A

CD54ACT151/3A

SWITCHING CHARACTERISTICS: AC Series; $t_r, t_f = 3 \text{ ns}$, $C_L = 50 \text{ pF}$ (Worst Case)

CHARACTERISTICS	SYMBOL	V_{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delays Any Data to Y	t_{PLH}	1.5	—	169	ns
	t_{PHL}	3.3*	3.5	18.9	
Any Data to \bar{Y}	t_{PLH}	1.5	—	186	ns
	t_{PHL}	3.3	3.8	20.9	
Any Select to Y	t_{PLH}	5†	2.3	13.5*	ns
	t_{PHL}	1.5	—	228	
Any Select to \bar{Y}	t_{PLH}	3.3	4.7	25.5	ns
	t_{PHL}	5	3.1	18.2*	
Any Enable to Y	t_{PLH}	1.5	—	245	ns
	t_{PHL}	3.3	5	27.4	
Any Enable to \bar{Y}	t_{PLH}	5	3.4	19.6*	ns
	t_{PHL}	1.5	—	153	
Any \bar{E} to Y	t_{PLH}	3.3	3.2	17.1	ns
	t_{PHL}	5	2.1	12.2*	
Any \bar{E} to \bar{Y}	t_{PLH}	1.5	—	169	ns
	t_{PHL}	3.3	3.5	18.9	
Power Dissipation Capacitance	$C_{PD}\S$	—	—	13.5*	pF
	C_I	—	—	10	

SWITCHING CHARACTERISTICS: ACT Series; $t_r, t_f = 3 \text{ ns}$, $C_L = 50 \text{ pF}$ (Worst Case)

CHARACTERISTICS	SYMBOL	V_{CC} (V)	-55 to +125°C		UNITS
			MIN.	MAX.	
Propagation Delays Any Data to Y	t_{PLH}	5*	2.7	15.5*	ns
	t_{PHL}	5	2.9	16.9*	
Any Data to \bar{Y}	t_{PLH}	5	3.5	20.2*	ns
	t_{PHL}	5	3.7	21.6*	
Any Select to Y	t_{PLH}	5	2.1	12.1*	ns
	t_{PHL}	5	2.3	13.5*	
Any Select to \bar{Y}	t_{PLH}	5	—	—	ns
	t_{PHL}	5	—	—	
Any Enable to Y	t_{PLH}	—	—	—	pF
	t_{PHL}	—	—	—	
Any Enable to \bar{Y}	$C_{PD}\S$	—	—	10	pF
	C_I	—	—	—	

*3.3 V: min. is @ 3.6 V
max. is @ 3 V

†5 V: min. is @ 5.5 V
max. is @ 4.5 V

§ C_{PD} is used to determine the dynamic power consumption per device.

For AC, $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$

For ACT, $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency

C_L = output load capacitance

V_{CC} = supply voltage

(Limits with black dots (•) are tested 100%.)