



# LOW SKEW, 1-TO-5 DIFFERENTIAL-TO-3.3V LVPECL FANOUT BUFFER

IDT85304-01

## FEATURES:

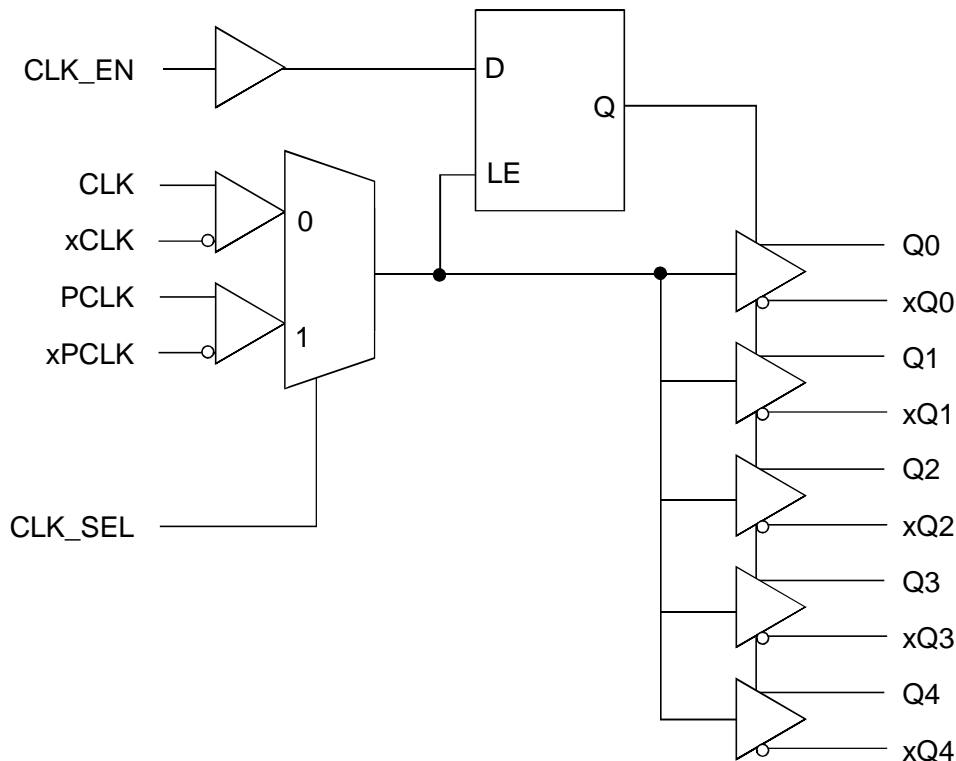
- Five differential 3.3V LVPECL outputs
- Selectable differential CLK, xCLK, or LVPECL clock inputs
- CLK, xCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, and HCSL
- PCLK, xPCLK supports the following input types: LVPECL, CML, and SSTL
- Maximum output frequency: 650MHz
- Translates any single-ended input signal to 3.3V LVPECL levels with resistor bias on xCLK input
- Output skew: 35ps (max.)
- Part-to-part skew: as low as 150ps
- Propagation delay: 2.1ns (max.)
- 3.3V operating supply
- Available in TSSOP package

## DESCRIPTION:

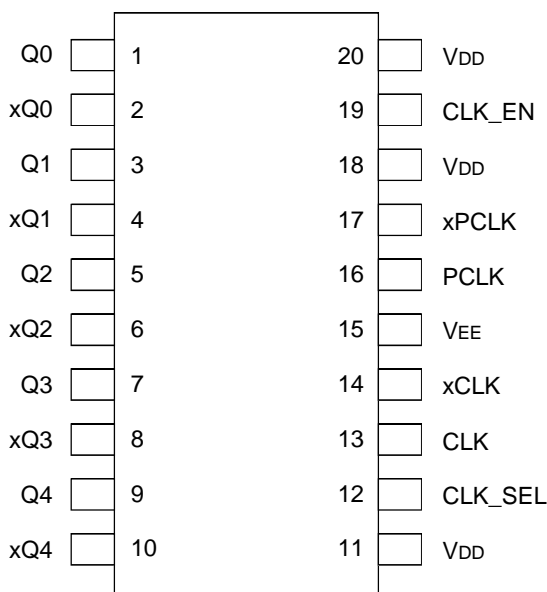
The IDT85304-01 is a low skew, high performance 1-to-5 differential-to-3.3V LVPECL clock generator-divider. It has two selectable clock inputs. The CLK/xCLK pair can accept most standard differential input levels. The PCLK/xPCLK pair can accept LVPECL, CML, or SSTL input levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the IDT85304-01 ideal for those applications that demand well-defined performance and repeatability.

## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION



TSSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

| Symbol           | Description                       | Max                          | Unit |
|------------------|-----------------------------------|------------------------------|------|
| V <sub>DD</sub>  | Power Supply Voltage              | 4.6                          | V    |
| V <sub>I</sub>   | Input Voltage                     | -0.5 to V <sub>DD</sub> +0.5 | V    |
| V <sub>O</sub>   | Output Voltage                    | -0.5 to V <sub>DD</sub> +0.5 | V    |
| θ <sub>JA</sub>  | Package Thermal Impedance (0lfpm) | 92.6                         | °C/W |
| T <sub>STG</sub> | Storage Temperature               | -65 to +150                  | °C   |

### NOTE:

- Stresses beyond those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1MHz, V<sub>IN</sub> = 0V)

| Parameter             | Description             | Typ. | Max. | Unit |
|-----------------------|-------------------------|------|------|------|
| C <sub>IN</sub>       | Input Capacitance       | —    | 4    | pF   |
| R <sub>PULLUP</sub>   | Input Pullup Resistor   | 51   | —    | KΩ   |
| R <sub>PULLDOWN</sub> | Input Pulldown Resistor | 51   | —    | KΩ   |

## PIN DESCRIPTION<sup>(1)</sup>

| Symbol          | Number     | Type   |          | Description  |
|-----------------|------------|--------|----------|--|
| xQ0, Q0         | 1, 2       | Output |          | Differential Output Pair. LVPECL interface levels.   |
| xQ1, Q1         | 3, 4       | Output |          | Differential Output Pair. LVPECL interface levels.   |
| xQ2, Q2         | 5, 6       | Output |          | Differential Output Pair. LVPECL interface levels.   |
| xQ3, Q3         | 7, 8       | Output |          | Differential Output Pair. LVPECL interface levels.   |
| xQ4, Q4         | 9, 10      | Output |          | Differential Output Pair. LVPECL interface levels.   |
| V <sub>DD</sub> | 11, 18, 20 | Power  |          | Positive Supply Pins   |
| CLK_SEL         | 12         | Input  | Pulldown | Clock Select Input. When HIGH, selects PCLK/xPCLK inputs. When LOW, selects CLK/xCLK inputs. LVTTTL/LVCMOS interface levels.   |
| CLK             | 13         | Input  | Pulldown | Non-Inverting Differential Clock Input   |
| xCLK            | 14         | Input  | Pullup   | Inverting Differential Clock Input   |
| V <sub>EE</sub> | 15         | Power  |          | Negative Supply Pin  |
| PCLK            | 16         | Input  | Pulldown | Non-Inverting Differential LVPECL Clock Input  |
| xPCLK           | 17         | Input  | Pullup   | Inverting Differential LVPECL Clock Input  |
| CLK_EN          | 19         | Input  | Pullup   | Synchronizing Clock Enable. When HIGH, clock outputs follow clock input. When LOW, Q outputs are forced LOW, xQ outputs are forced HIGH. LVTTTL/LVCMOS interface levels. |

### NOTE:

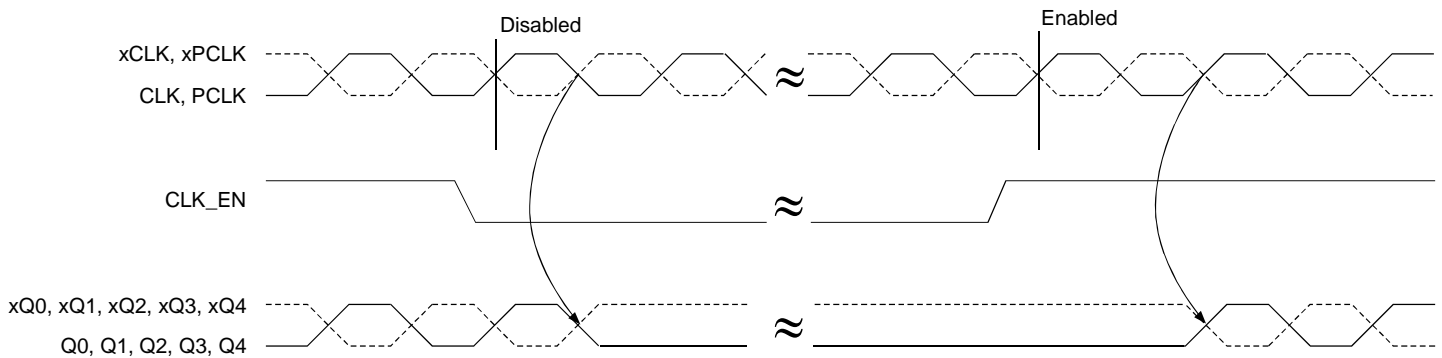
- Pullup and Pulldown refer to internal input resistors. See Capacitance table for typical values.

### CONTROL INPUT FUNCTION TABLE<sup>(1,2)</sup>

| Inputs |         |                 | Outputs       |                |
|--------|---------|-----------------|---------------|----------------|
| CLK_EN | CLK_SEL | Selected Source | Q0:Q4         | xQ0:xQ4        |
| 0      | 0       | CLK, xCLK       | Disabled; LOW | Disabled; HIGH |
| 0      | 1       | PCLK, xPCLK     | Disabled; LOW | Disabled; HIGH |
| 1      | 0       | CLK, xCLK       | Enabled       | Enabled        |
| 1      | 1       | PCLK, xPCLK     | Enabled       | Enabled        |

**NOTES:**

1. After CLK\_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in the CLK\_EN Timing Diagram below.
2. In active mode, the state of the outputs is a function of the CLK / xCLK and PCLK / xPCLK inputs as described in the Clock Input Function table.



*CLK\_EN Timing Diagram*

### CLOCK INPUT FUNCTION TABLE<sup>(1)</sup>

| Inputs                |                       | Outputs |         | Input to Output Mode         | Polarity      |
|-----------------------|-----------------------|---------|---------|------------------------------|---------------|
| CLK or PCLK           | xCLK or xPCLK         | Q0:Q4   | xQ0:xQ4 |                              |               |
| 0                     | 1                     | L       | H       | Differential to Differential | Non-Inverting |
| 1                     | 0                     | H       | L       | Differential to Differential | Non-Inverting |
| 0                     | Biased <sup>(2)</sup> | L       | H       | Single-Ended to Differential | Non-Inverting |
| 1                     | Biased <sup>(2)</sup> | H       | L       | Single-Ended to Differential | Non-Inverting |
| Biased <sup>(2)</sup> | 0                     | H       | L       | Single-Ended to Differential | Inverting     |
| Biased <sup>(2)</sup> | 1                     | L       | H       | Single-Ended to Differential | Inverting     |

**NOTES:**

1. H = HIGH  
L = LOW
2. See Single-Ended Signal diagram under Application Information at the end of this datasheet.

## POWER SUPPLY CHARACTERISTICS

| Symbol          | Parameter               | Test Conditions | Min.  | Typ. | Max.  | Unit |
|-----------------|-------------------------|-----------------|-------|------|-------|------|
| V <sub>DD</sub> | Positive Supply Voltage |                 | 3.135 | 3.3  | 3.465 | V    |
| I <sub>EE</sub> | Power Supply Current    |                 | —     | —    | 55    | mA   |

## DC ELECTRICAL CHARACTERISTICS, LVCMOS / LVTTTL

| Symbol          | Parameter           | Test Conditions   | Min. | Typ. | Max.                  | Unit |
|-----------------|---------------------|---|------|------|-----------------------|------|
| V <sub>IH</sub> | Input Voltage, HIGH | CLK_EN,<br>CLK_SEL  | 2    |      | V <sub>DD</sub> + 0.3 | V    |
| V <sub>IL</sub> | Input Voltage, LOW  | CLK_EN,<br>CLK_SEL  | -0.3 |      | 0.8                   | V    |
| I <sub>IH</sub> | Input Current HIGH  | CLK_EN<br>V <sub>IN</sub> = V <sub>DD</sub> = 3.465V      |      |      | 5                     | μA   |
|                 |                     | CLK_SEL<br>V <sub>IN</sub> = V <sub>DD</sub> = 3.465V     |      |      | 150                   |      |
| I <sub>IL</sub> | Input Current LOW   | CLK_EN<br>V <sub>IN</sub> = 0V, V <sub>DD</sub> = 3.465V  | -150 |      |                       | μA   |
|                 |                     | CLK_SEL<br>V <sub>IN</sub> = 0V, V <sub>DD</sub> = 3.465V | -5   |      |                       |      |

## DC ELECTRICAL CHARACTERISTICS, DIFFERENTIAL

| Symbol           | Parameter                                  | Test Conditions  | Min. | Typ. | Max.                   | Unit |
|------------------|--|--|------|------|------------------------|------|
| V <sub>PP</sub>  | Peak-to-Peak Input Voltage                 |  | 0.15 |      | 1.3                    | V    |
| V <sub>CMR</sub> | Common Mode Input Voltage <sup>(1,2)</sup> |  | 0.5  |      | V <sub>DD</sub> - 0.85 | V    |
| I <sub>IH</sub>  | Input Current HIGH                         | xCLK<br>V <sub>IN</sub> = V <sub>DD</sub> = 3.465V     |      |      | 5                      | μA   |
|                  |  | CLK<br>V <sub>IN</sub> = V <sub>DD</sub> = 3.465V      |      |      | 150                    |      |
| I <sub>IL</sub>  | Input Current LOW                          | xCLK<br>V <sub>IN</sub> = 0V, V <sub>DD</sub> = 3.465V | -150 |      |                        | μA   |
|                  |  | CLK<br>V <sub>IN</sub> = 0V, V <sub>DD</sub> = 3.465V  | -5   |      |                        |      |

### NOTES:

- For single-ended applications, the max. input voltage for CLK / xCLK is V<sub>DD</sub> + 0.3V.
- Common mode voltage is defined as V<sub>IH</sub>.

## DC ELECTRICAL CHARACTERISTICS, LVPECL

| Symbol             | Parameter                                  | Test Conditions   | Min.                  | Typ. | Max.                  | Unit |
|--------------------|--|---|-----------------------|------|-----------------------|------|
| I <sub>IH</sub>    | Input Current HIGH                         | PCLK<br>V <sub>IN</sub> = V <sub>DD</sub> = 3.465V      |                       |      | 150                   | μA   |
|                    |  | xPCLK<br>V <sub>IN</sub> = V <sub>DD</sub> = 3.465V     |                       |      | 5                     |      |
| I <sub>IL</sub>    | Input Current LOW                          | PCLK<br>V <sub>IN</sub> = 0V, V <sub>DD</sub> = 3.465V  | -5                    |      |                       | μA   |
|                    |  | xPCLK<br>V <sub>IN</sub> = 0V, V <sub>DD</sub> = 3.465V | -150                  |      |                       |      |
| V <sub>PP</sub>    | Peak-to-Peak Input Voltage                 |   | 0.15                  |      | 1.3                   | V    |
| V <sub>CMR</sub>   | Common Mode Input Voltage <sup>(1,2)</sup> |   | V <sub>EE</sub> + 1.5 |      | V <sub>DD</sub>       | V    |
| V <sub>OH</sub>    | Output Voltage HIGH <sup>(3)</sup>         |   | V <sub>DD</sub> - 1.4 |      | V <sub>DD</sub> - 1   | V    |
| V <sub>OL</sub>    | Output Voltage LOW <sup>(3)</sup>          |   | V <sub>DD</sub> - 2   |      | V <sub>DD</sub> - 1.7 | V    |
| V <sub>SWING</sub> | Peak-to-Peak Output Voltage Swing          |   | 0.6                   |      | 0.85                  | V    |

### NOTES:

- For single-ended applications, the max. input voltage for PCLK / xPCLK is V<sub>DD</sub> + 0.3V.
- Common mode voltage is defined as V<sub>IH</sub>.
- Outputs terminated with 50Ω to V<sub>DD</sub> - 0.2V.

## AC ELECTRICAL CHARACTERISTICS

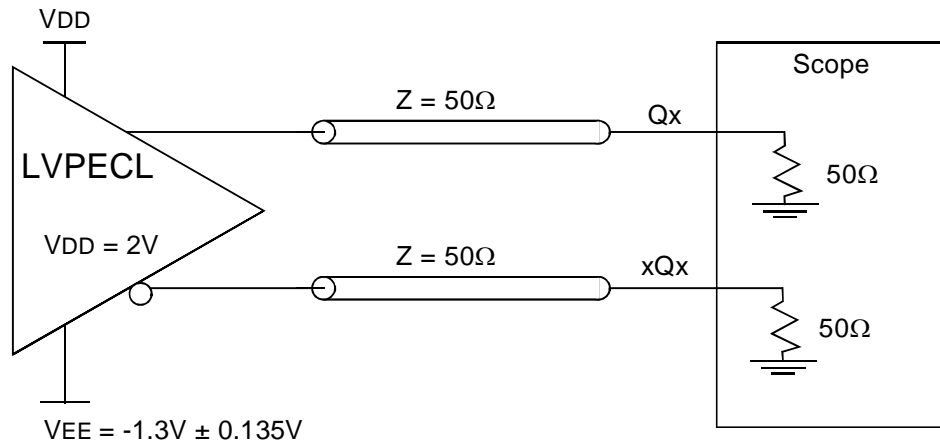
All parameters measured at 500MHz unless noted otherwise;  
 Cycle-to-cycle jitter = jitter on output; the part does not add jitter

| Symbol              | Parameter                          | Test Conditions  | Min. | Typ. | Max. | Unit |
|---------------------|------------------------------------|------------------|------|------|------|------|
| F <sub>MAX</sub>    | Output Frequency                   |                  |      |      | 650  | MHz  |
| t <sub>PD</sub>     | Propagation Delay <sup>(1)</sup>   | f ≤ 650MHz       | 1    |      | 2.1  | ns   |
| t <sub>sk(o)</sub>  | Output Skew <sup>(2,4)</sup>       |                  |      |      | 35   | ps   |
| t <sub>sk(pp)</sub> | Part-to-Part Skew <sup>(3,4)</sup> |                  |      |      | 150  | ps   |
| t <sub>r</sub>      | Output Rise Time                   | 20 - 80% @ 50MHz | 300  |      | 700  | ps   |
| t <sub>f</sub>      | Output Fall Time                   | 20 - 80% @ 50MHz | 300  |      | 700  | ps   |
| odc                 | Output Duty Cycle                  |                  | 48   | 50   | 52   | %    |

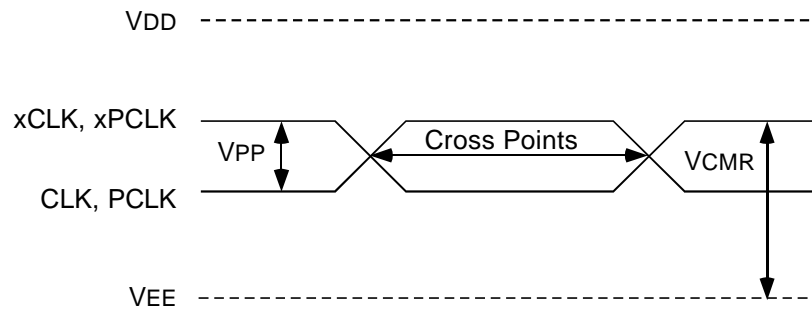
### NOTES:

1. Measured from the differential input crossingpoint to the differential output crossingpoint.
2. Defined as skew between outputs as the same supply voltage and with equal load conditions. Measured at the output differential crosspoints
3. Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoints.
4. This parameter is defined in accordance with JEDEC Standard 65.

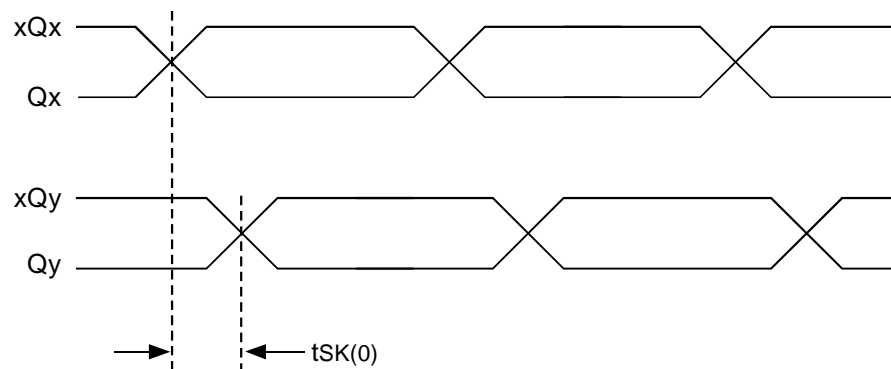
PARAMETER MEASUREMENT INFORMATION



Output Load Test Circuit

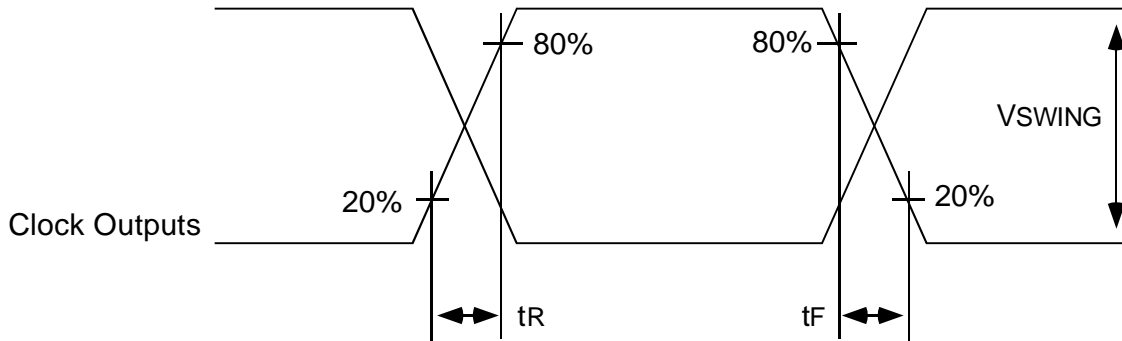


Differential Input Level

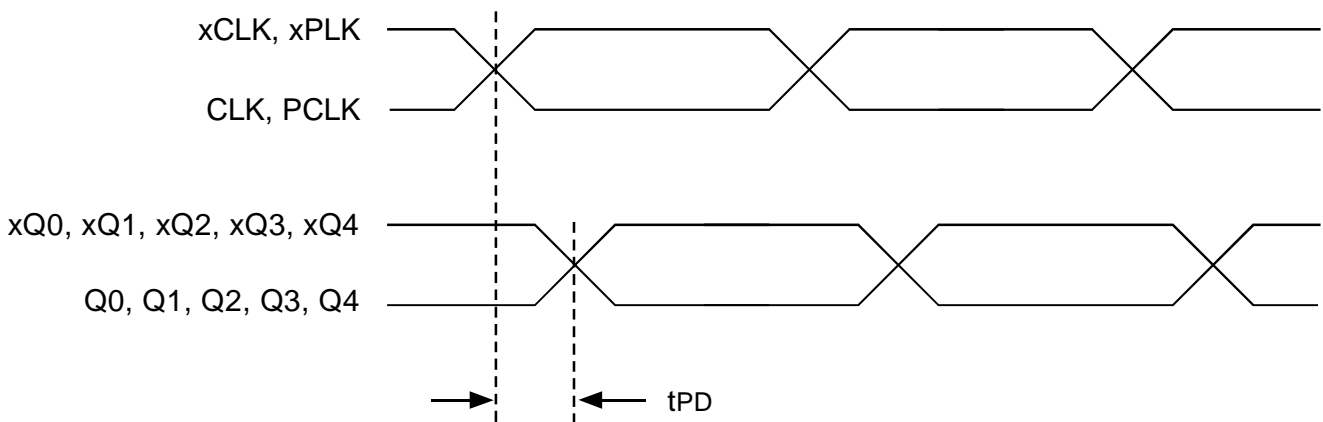


Output Skew

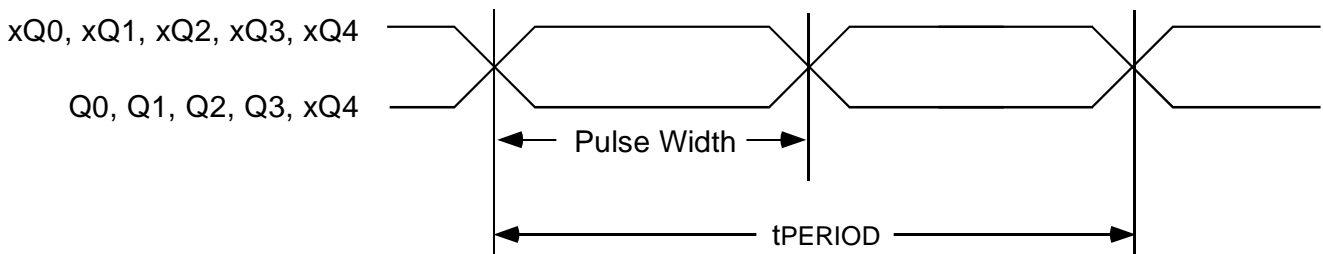
PARAMETER MEASUREMENT INFORMATION - CONTINUED



*Input and Output Rise and Fall Time*



*Propagation Delay*



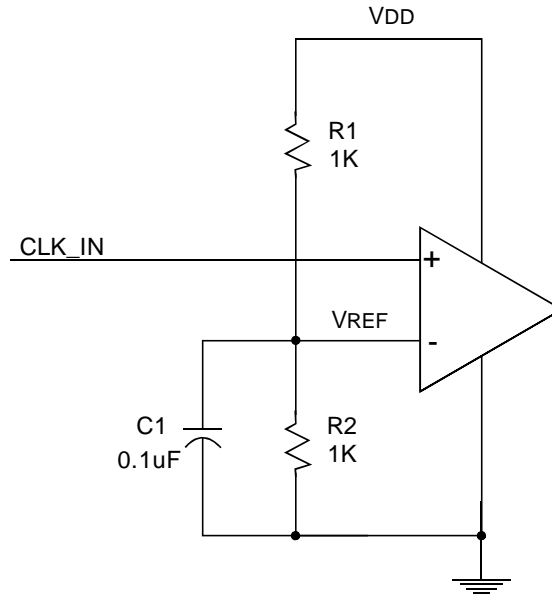
$$odc = \frac{tW}{t_{PERIOD}}$$

*odc and  $t_{PERIOD}$*

## APPLICATION INFORMATION

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE-ENDED LEVELS

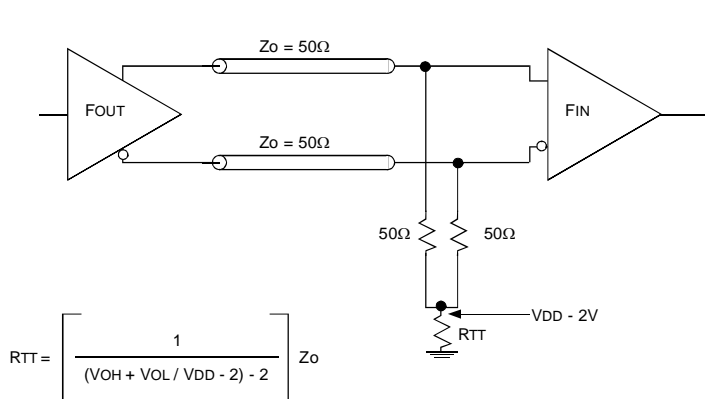
The diagram below shows how the differential input can be wired to accept single-ended levels. The reference voltage  $V_{REF} \sim V_{DD}/2$  is generated by the bias resistors R1, R2, and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{DD} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .



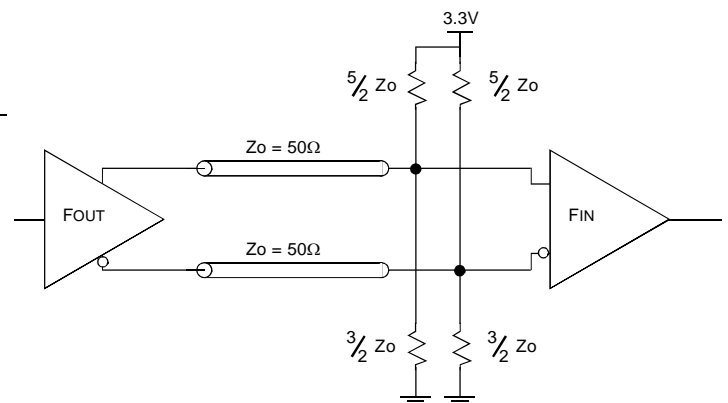
*Single-Ended Signal Driving Differential Input*

### TERMINATION FOR LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.  $F_{OUT}$  and  $xF_{OUT}$  are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive  $50\Omega$  transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. The diagrams below show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist. It is recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.



*LVPECL Output Termination, layout A*



*LVPECL Output Termination, layout B*



## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the IDT85304-01. Equations and example calculations are also provided.

### POWER DISSIPATION:

The total power dissipation for the IDT85304-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for the  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results. Please refer to the following section, **Calculations and Equations**, for details on calculating power dissipated in the load.

$$\text{Power (core)}_{MAX} = V_{DD\_MAX} * I_{EE\_MAX} = 3.465 * 55mA = 190.57mW$$

$$\text{Power (outputs)}_{MAX} = 30.2mW/\text{Loaded Output Pair}$$

$$\text{If all outputs are loaded, the total power is } 5 * 30.2mW = 151mW$$

$$\text{Total Power}_{MAX} (3.465V, \text{ with all outputs switching}) = 190.57mW + 151mW = 341.57mW$$

### JUNCTION TEMPERATURE:

Junction temperature ( $t_J$ ) is the temperature at the junction of the bond wire and bond pad. It directly affects the reliability of the device. The maximum recommended junction temperature for this device is 125°C.

The equation for is as follows:  $t_J = \theta_{JA} * Pd_{total} + T_A$

$t_J$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd_{total}$  = Total Device Power Dissipation (example calculation is in **Power Dissipation**, above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance ( $\theta_{JA}$ ) must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 77.6°C/W per the following **Thermal Resistance** table. Therefore,  $t_J$  for an ambient temperature of 85°C with all its outputs switching is:

$$85^\circ C + 0.341W * 77.6^\circ C/W = 111.5^\circ C. \text{ This is well below the limit of } 125^\circ C.$$

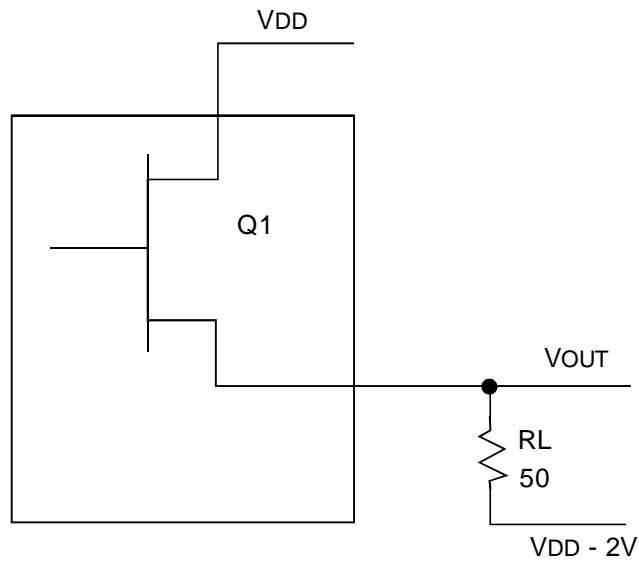
This calculation is only an example.  $t_J$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single-layer or multi-layer).

## THERMAL RESISTANCE

$\theta_{JA}$  for 20-pin TSSOP, forced convection

| $\theta_{JA}$ by Velocity (Linear Feet per minute) |      |      |      |      |
|--|------|------|------|------|
|  | 0    | 200  | 400  | Unit |
| Multi-Layer PCB, JEDEC Standard Test boards        | 92.6 | 77.6 | 70.9 | °C/W |

## CALCULATIONS AND EQUATIONS



*LVPECL Output Driver Circuit and Termination*

To calculate worst case power dissipation into the load, use the following equations, which assume a  $50\Omega$  load and a termination voltage of  $V_{DD} - 2V$ .

For Logic HIGH:  $V_{OUT} = V_{OH\_MAX} = V_{DD\_MAX} - 1V$ .  
 $(V_{DD\_MAX} - V_{OH\_MAX}) = 1V$

For Logic LOW:  $V_{OUT} = V_{OL\_MAX} = V_{DD\_MAX} - 1.7V$ .  
 $(V_{DD\_MAX} - V_{OL\_MAX}) = 1.7V$

$Pd\_H$  is power dissipation when the output drives HIGH.

$Pd\_L$  is power dissipation when the output drives LOW.

$$Pd\_H = \left\{ \frac{V_{OH\_MAX} - (V_{DD\_MAX} - 2V)}{R_L} \right\} \cdot (V_{DD\_MAX} - V_{OH\_MAX}) = \left\{ \frac{2V - (V_{DD\_MAX} - V_{OH\_MAX})}{R_L} \right\} \cdot (V_{DD\_MAX} - V_{OH\_MAX}) = \left[ \frac{(2V - 1V)}{50\Omega} \right]^2 \cdot 1V = 20mW.$$

$$Pd\_L = \left\{ \frac{V_{OL\_MAX} - (V_{DD\_MAX} - 2V)}{R_L} \right\} \cdot (V_{DD\_MAX} - V_{OL\_MAX}) = \left\{ \frac{2V - (V_{DD\_MAX} - V_{OL\_MAX})}{R_L} \right\} \cdot (V_{DD\_MAX} - V_{OL\_MAX}) = \left[ \frac{(2V - 1.7V)}{50\Omega} \right]^2 \cdot 1.7V = 10.2mW.$$

$$\text{Total Power Dissipation per output pair} = Pd\_H + Pd\_L = 30.2mW$$

## ORDERING INFORMATION

| IDT | XXXXX       | XX      | X       |          |   |
|-----|-------------|---------|---------|----------|---|
|     | Device Type | Package | Process |          |   |
|     |             |         |         | Blank    | Commercial (0°C to +70°C)<br>Industrial (-40°C to +85°C)      |
|     |             |         |         | I        |   |
|     |             |         |         | PG       | Thin Shrink Small Outline Package                             |
|     |             |         |         | 85304-01 | Low Skew, 1-to-5 Differential-to-3.3V LVPECL<br>Fanout Buffer |



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