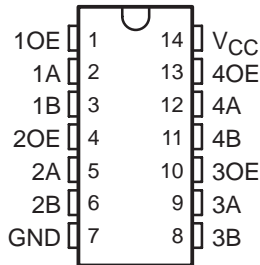


# SN74CBTLV3126 LOW-VOLTAGE QUADRUPLE FET BUS SWITCH

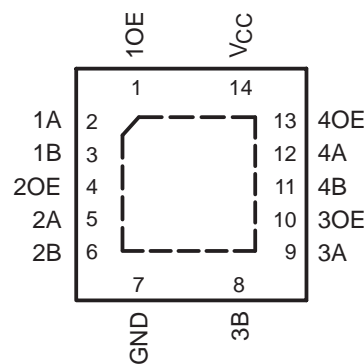
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- Standard '126-Type Pinout
- 5-Ω Switch Connection Between Two Ports
- Rail-to-Rail Switching on Data I/O Ports
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-up Performance Exceeds 100 mA per JESD 78, Class II

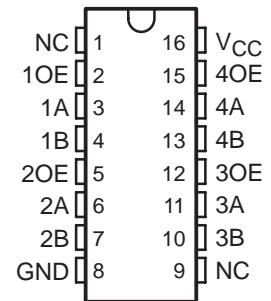
D, DGV, OR PW PACKAGE  
(TOP VIEW)



RGY PACKAGE  
(TOP VIEW)



DBQ PACKAGE  
(TOP VIEW)



NC – No internal connection

## description/ordering information

The SN74CBTLV3126 quadruple FET bus switch features independent line switches. Each switch is disabled when the associated output-enable (OE) input is low.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pull-down resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## ORDERING INFORMATION

| $T_A$         | PACKAGE†          |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|-------------------|---------------|-----------------------|------------------|
| –40°C to 85°C | QFN – RGY         | Tape and reel | SN74CBTLV3126RGYR     | CL126            |
|               | SOIC – D          | Tube          | SN74CBTLV3126D        | CBTLV3126        |
|               |                   | Tape and reel | SN74CBTLV3126DR       |                  |
|               | SSOP (QSOP) – DBQ | Tape and reel | SN74CBTLV3126DBQR     | CL126            |
|               | TSSOP – PW        | Tape and reel | SN74CBTLV3126PWR      | CL126            |
|               | TVSOP – DGV       | Tape and reel | SN74CBTLV3126DGV      | CL126            |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

FUNCTION TABLE  
(each bus switch)

| INPUT OE | FUNCTION        |
|----------|-----------------|
| L        | Disconnect      |
| H        | A port = B port |



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 **TEXAS  
INSTRUMENTS**

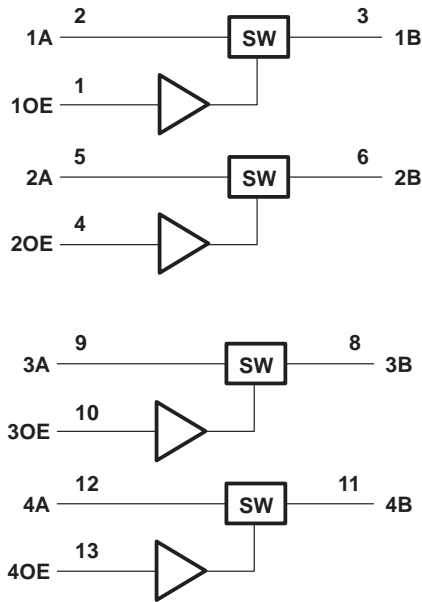
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# SN74CBTLV3126 LOW-VOLTAGE QUADRUPLE FET BUS SWITCH

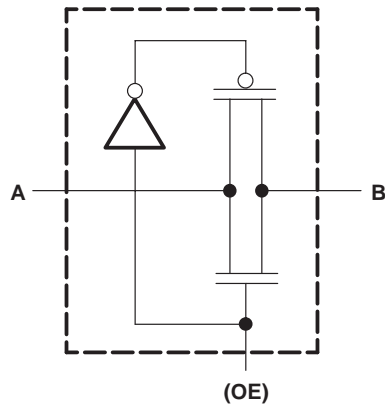
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## logic diagram (positive logic)



Pin numbers shown are for the D, DGV, PW, and RGY packages.

## simplified schematic, each FET switch



# SN74CBTLV3126

## LOW-VOLTAGE QUADRUPLE FET BUS SWITCH

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

|  |                 |
|--|-----------------|
| Supply voltage range, $V_{CC}$ .....                                   | –0.5 V to 4.6 V |
| Input voltage range, $V_I$ (see Note 1) .....                          | –0.5 V to 4.6 V |
| Continuous channel current .....                                       | 128 mA          |
| Input clamp current, $I_{IK}$ ( $V_{I/O} < 0$ ) .....                  | –50 mA          |
| Package thermal impedance, $\theta_{JA}$ (see Note 2): D package ..... | 86°C/W          |
| (see Note 2): DBQ package .....  | 90°C/W          |
| (see Note 2): DGV package .....  | 127°C/W         |
| (see Note 2): PW package .....   | 113°C/W         |
| (see Note 3): RGY package .....  | 47°C/W          |
| Storage temperature range, $T_{stg}$ .....                             | –65°C to 150°C  |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.  
 3. The package thermal impedance is calculated in accordance with JESD 51-5.

### recommended operating conditions (see Note 4)

|          |                                  | MIN                                     | MAX | UNIT |
|----------|----------------------------------|---|-----|------|
| $V_{CC}$ | Supply voltage                   | 2.3                                     | 3.6 | V    |
| $V_{IH}$ | High-level control input voltage | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 1.7 | V    |
|          |                                  | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | 2   |      |
| $V_{IL}$ | Low-level control input voltage  | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ | 0.7 | V    |
|          |                                  | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | 0.8 |      |
| $T_A$    | Operating free-air temperature   | –40                                     | 85  | °C   |

NOTE 4: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER            | TEST CONDITIONS   |  | MIN                  | TYP‡ | MAX  | UNIT |
|----------------------|---|--|----------------------|------|------|------|
| $V_{IK}$             | $V_{CC} = 3\text{ V}$ ,                                     | $I_I = -18\text{ mA}$  |                      |      | –1.2 | V    |
| $I_I$                | $V_{CC} = 3.6\text{ V}$ ,                                   | $V_I = V_{CC}$ or GND  |                      |      | ±1   | µA   |
| $I_{off}$            | $V_{CC} = 0$ ,  | $V_I$ or $V_O = 0$ to 3.6 V  |                      |      | 10   | µA   |
| $I_{CC}$             | $V_{CC} = 3.6\text{ V}$ ,                                   | $I_O = 0$ , $V_I = V_{CC}$ or GND  |                      |      | 10   | µA   |
| $\Delta I_{CC}^{\S}$ | Control inputs  | $V_{CC} = 3.6\text{ V}$ ,<br>One input at 3 V, Other inputs at $V_{CC}$ or GND |                      |      | 300  | µA   |
| $C_i$                | Control inputs  | $V_I = 3\text{ V}$ or 0  |                      |      | 2.5  | pF   |
| $C_{io(OFF)}$        |   | $V_O = 3\text{ V}$ or 0, OE = GND  |                      |      | 7    | pF   |
| $r_{on}^{\parallel}$ | $V_{CC} = 2.3\text{ V}$ ,<br>TYP at $V_{CC} = 2.5\text{ V}$ | $V_I = 0$  | $I_I = 64\text{ mA}$ | 5    | 8    | Ω    |
|                      |   |  | $I_I = 24\text{ mA}$ | 5    | 8    |      |
|                      |   | $V_I = 1.7\text{ V}$ ,   | $I_I = 15\text{ mA}$ | 27   | 40   |      |
|                      | $V_{CC} = 3\text{ V}$                                       | $V_I = 0$  | $I_I = 64\text{ mA}$ | 5    | 7    |      |
|                      |   |  | $I_I = 24\text{ mA}$ | 5    | 7    |      |
|                      |   | $V_I = 2.4\text{ V}$ ,   | $I_I = 15\text{ mA}$ | 10   | 15   |      |

‡ All typical values are at  $V_{CC} = 3.3\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

§ This is the increase in supply current for each input that is at the specified voltage level, rather than  $V_{CC}$  or GND.

∥ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



# SN74CBTLV3126

## LOW-VOLTAGE QUADRUPLE FET BUS SWITCH

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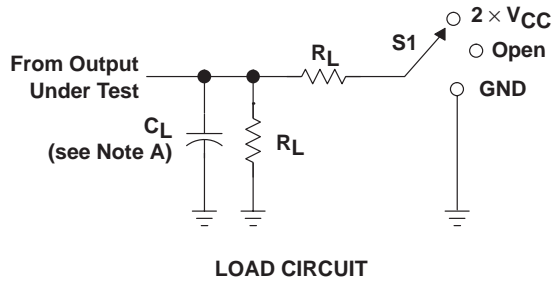
switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| PARAMETER                    | FROM<br>(INPUT) | TO<br>(OUTPUT) | V <sub>CC</sub> = 2.5 V<br>± 0.2 V |     | V <sub>CC</sub> = 3.3 V<br>± 0.3 V |     | UNIT |
|------------------------------|-----------------|----------------|------------------------------------|-----|------------------------------------|-----|------|
|                              |                 |                | MIN                                | MAX | MIN                                | MAX |      |
| t <sub>pd</sub> <sup>†</sup> | A or B          | B or A         | 0.15                               |     | 0.25                               |     | ns   |
| t <sub>en</sub>              | OE              | A or B         | 1.6                                | 4.5 | 1.9                                | 4.2 | ns   |
| t <sub>dis</sub>             | OE              | A or B         | 1.3                                | 4.7 | 1                                  | 4.8 | ns   |

<sup>†</sup> The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

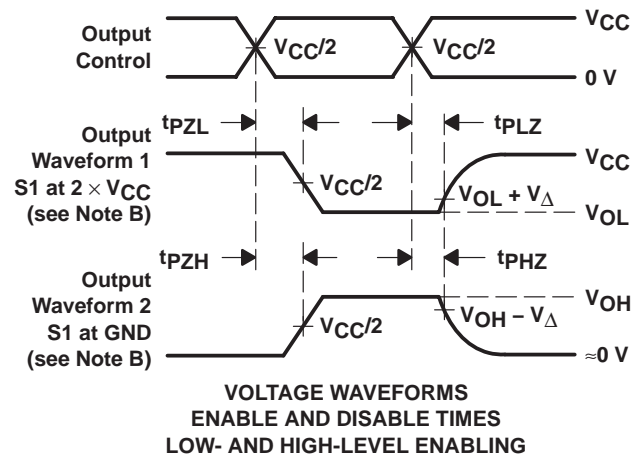
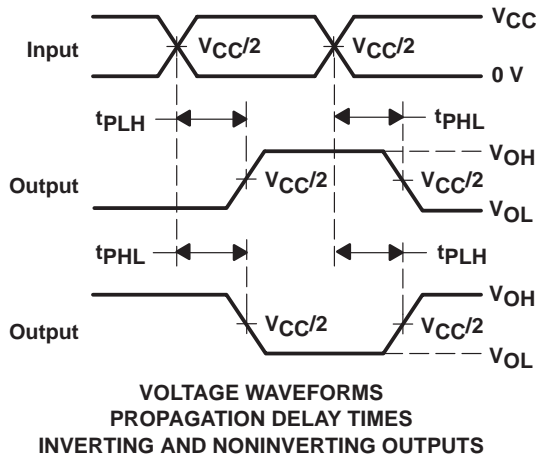
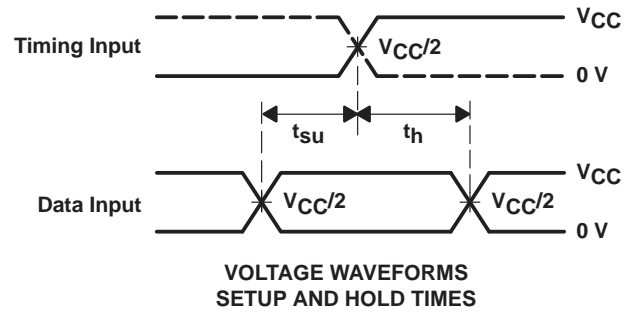
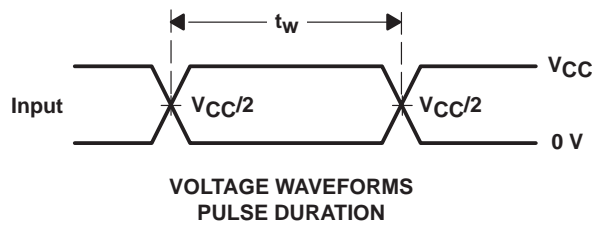


## PARAMETER MEASUREMENT INFORMATION



| TEST              | S1                |
|-------------------|-------------------|
| $t_{PLH}/t_{PHL}$ | Open              |
| $t_{PLZ}/t_{PZL}$ | $2 \times V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND               |

| $V_{CC}$                          | $C_L$ | $R_L$        | $V_{\Delta}$ |
|-----------------------------------|-------|--------------|--------------|
| $2.5 \text{ V} \pm 0.2 \text{ V}$ | 30 pF | 500 $\Omega$ | 0.15 V       |
| $3.3 \text{ V} \pm 0.3 \text{ V}$ | 50 pF | 500 $\Omega$ | 0.3 V        |



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

| Orderable Device  | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish | MSL Peak Temp<br>(3) | Op Temp (°C) | Top-Side Markings<br>(4) | Samples                 |
|-------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| 74CBTLV3126DBQRE4 | ACTIVE        | SSOP         | DBQ             | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR  | -40 to 85    | CL126                    | <a href="#">Samples</a> |
| 74CBTLV3126DBQRG4 | ACTIVE        | SSOP         | DBQ             | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR  | -40 to 85    | CL126                    | <a href="#">Samples</a> |
| 74CBTLV3126DGVRE4 | ACTIVE        | TVSOP        | DGV             | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | CL126                    | <a href="#">Samples</a> |
| 74CBTLV3126DGVRG4 | ACTIVE        | TVSOP        | DGV             | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | CL126                    | <a href="#">Samples</a> |
| 74CBTLV3126PWRE4  | ACTIVE        | TSSOP        | PW              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | CL126                    | <a href="#">Samples</a> |
| 74CBTLV3126PWRG4  | ACTIVE        | TSSOP        | PW              | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | CL126                    | <a href="#">Samples</a> |
| 74CBTLV3126RGYRG4 | ACTIVE        | VQFN         | RGY             | 14   | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR  | -40 to 85    | CL126                    | <a href="#">Samples</a> |
| 74CBTLV3216PWRE4  | ACTIVE        | TSSOP        | PW              | 14   |             | TBD                     | Call TI          | Call TI              | -40 to 85    |                          | <a href="#">Samples</a> |
| SN74CBTLV3126D    | ACTIVE        | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | CBTLV3126                | <a href="#">Samples</a> |
| SN74CBTLV3126DBQR | ACTIVE        | SSOP         | DBQ             | 16   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR  | -40 to 85    | CL126                    | <a href="#">Samples</a> |
| SN74CBTLV3126DE4  | ACTIVE        | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | CBTLV3126                | <a href="#">Samples</a> |
| SN74CBTLV3126DG4  | ACTIVE        | SOIC         | D               | 14   | 50          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | CBTLV3126                | <a href="#">Samples</a> |
| SN74CBTLV3126DGV  | ACTIVE        | TVSOP        | DGV             | 14   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | CL126                    | <a href="#">Samples</a> |
| SN74CBTLV3126DR   | ACTIVE        | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | CBTLV3126                | <a href="#">Samples</a> |
| SN74CBTLV3126DRE4 | ACTIVE        | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | CBTLV3126                | <a href="#">Samples</a> |
| SN74CBTLV3126DRG4 | ACTIVE        | SOIC         | D               | 14   | 2500        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | CBTLV3126                | <a href="#">Samples</a> |
| SN74CBTLV3126PW   | ACTIVE        | TSSOP        | PW              | 14   | 90          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | CL126                    | <a href="#">Samples</a> |

| Orderable Device  | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish | MSL Peak Temp<br>(3) | Op Temp (°C) | Top-Side Markings<br>(4) | Samples                 |
|-------------------|---------------|--------------|--------------------|------|----------------|----------------------------|------------------|----------------------|--------------|--------------------------|-------------------------|
| SN74CBTLV3126PWE4 | ACTIVE        | TSSOP        | PW                 | 14   | 90             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | CL126                    | <a href="#">Samples</a> |
| SN74CBTLV3126PWG4 | ACTIVE        | TSSOP        | PW                 | 14   | 90             | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | CL126                    | <a href="#">Samples</a> |
| SN74CBTLV3126PWR  | ACTIVE        | TSSOP        | PW                 | 14   | 2000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   | -40 to 85    | CL126                    | <a href="#">Samples</a> |
| SN74CBTLV3126RGYR | ACTIVE        | VQFN         | RGY                | 14   | 3000           | Green (RoHS<br>& no Sb/Br) | CU NIPDAU        | Level-2-260C-1 YEAR  | -40 to 85    | CL126                    | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


|    |   |
|----|---|
| A0 | Dimension designed to accommodate the component width     |
| B0 | Dimension designed to accommodate the component length    |
| K0 | Dimension designed to accommodate the component thickness |
| W  | Overall width of the carrier tape                         |
| P1 | Pitch between successive cavity centers                   |

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74CBTLV3126DGVR | TVSOP        | DGV             | 14   | 2000 | 330.0              | 12.4               | 6.8     | 4.0     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74CBTLV3126DR   | SOIC         | D               | 14   | 2500 | 330.0              | 16.4               | 6.5     | 9.0     | 2.1     | 8.0     | 16.0   | Q1            |
| SN74CBTLV3126PWR  | TSSOP        | PW              | 14   | 2000 | 330.0              | 12.4               | 6.9     | 5.6     | 1.6     | 8.0     | 12.0   | Q1            |
| SN74CBTLV3126RGYR | VQFN         | RGY             | 14   | 3000 | 330.0              | 12.4               | 3.75    | 3.75    | 1.15    | 8.0     | 12.0   | Q1            |



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74CBTLV3126DGVR | TVSOP        | DGV             | 14   | 2000 | 367.0       | 367.0      | 35.0        |
| SN74CBTLV3126DR   | SOIC         | D               | 14   | 2500 | 367.0       | 367.0      | 38.0        |
| SN74CBTLV3126PWR  | TSSOP        | PW              | 14   | 2000 | 367.0       | 367.0      | 35.0        |
| SN74CBTLV3126RGYR | VQFN         | RGY             | 14   | 3000 | 367.0       | 367.0      | 35.0        |

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN

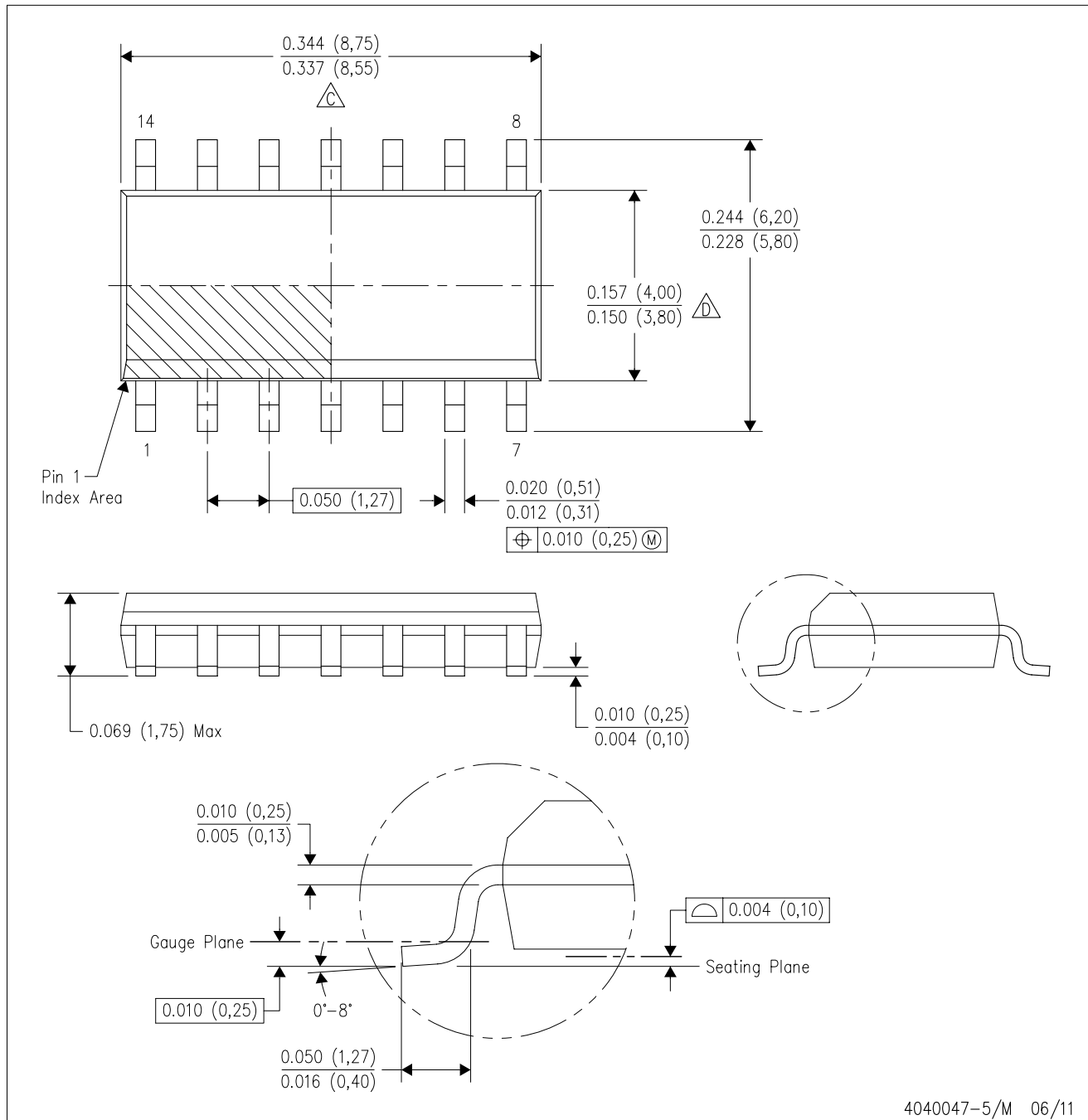


4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

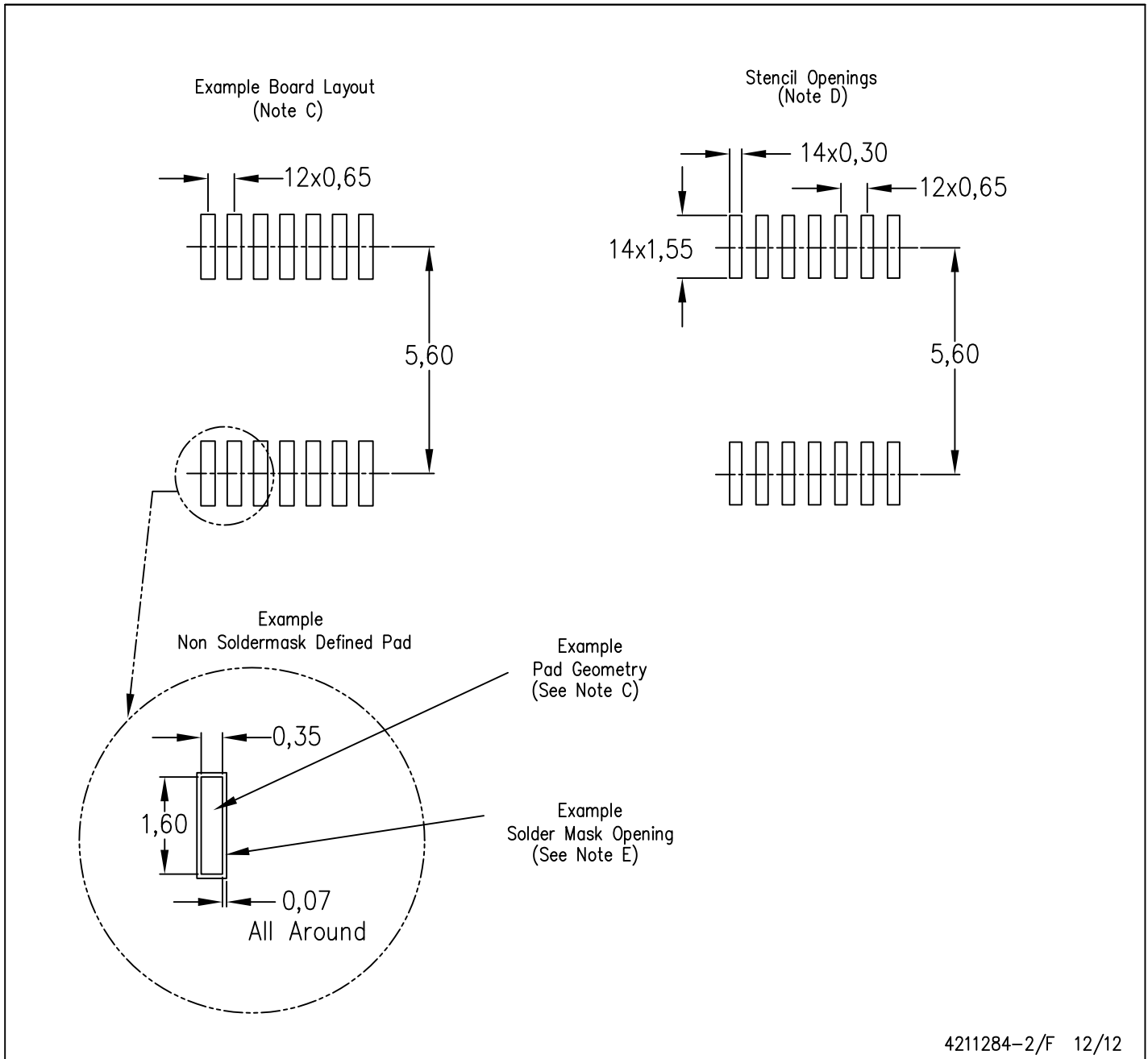


4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - Package complies to JEDEC MO-241 variation BA.

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD

**THERMAL INFORMATION**

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters



RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD

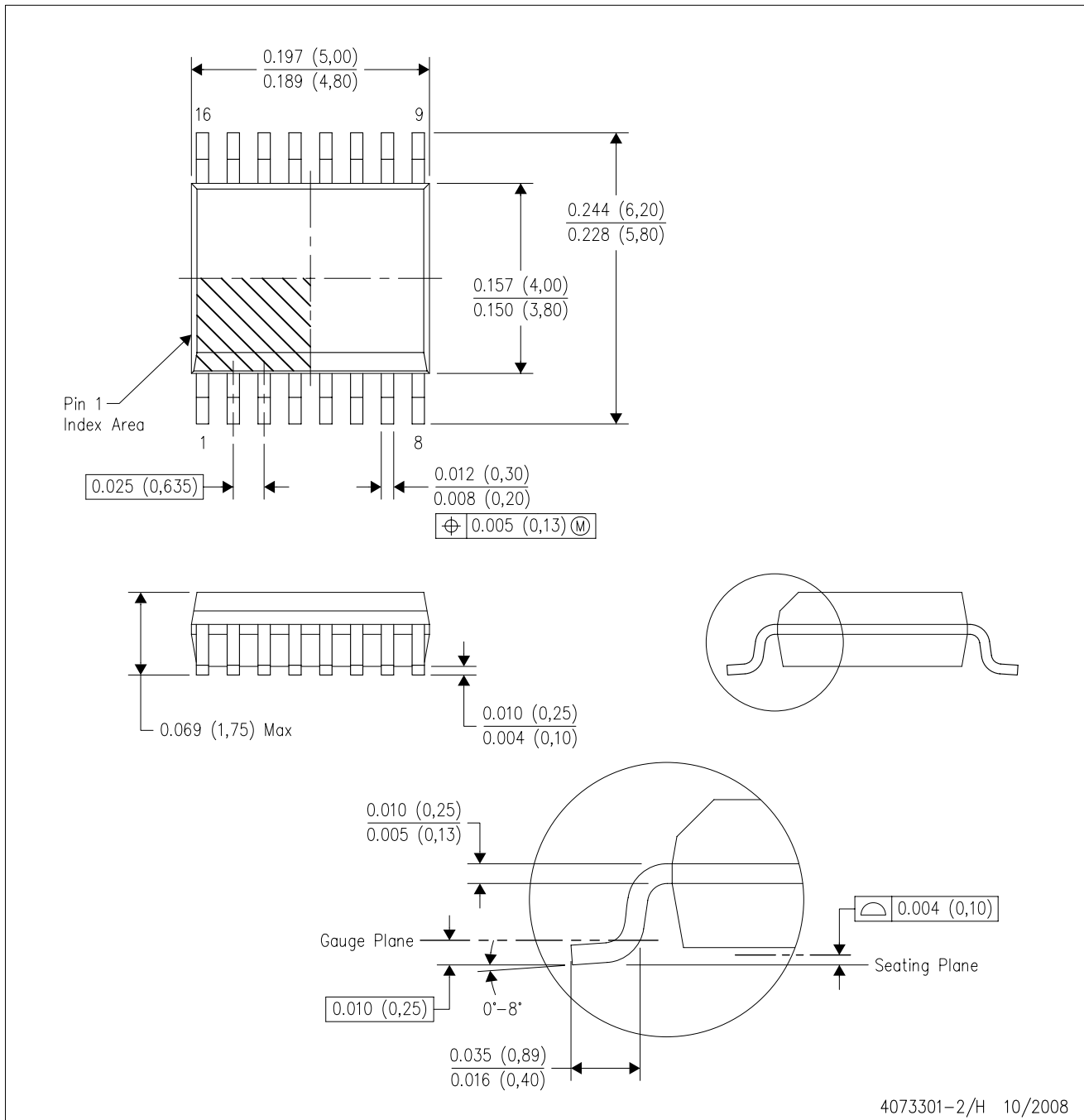


4208122-2/P 03/14

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

DBQ (R-PDSO-G16)

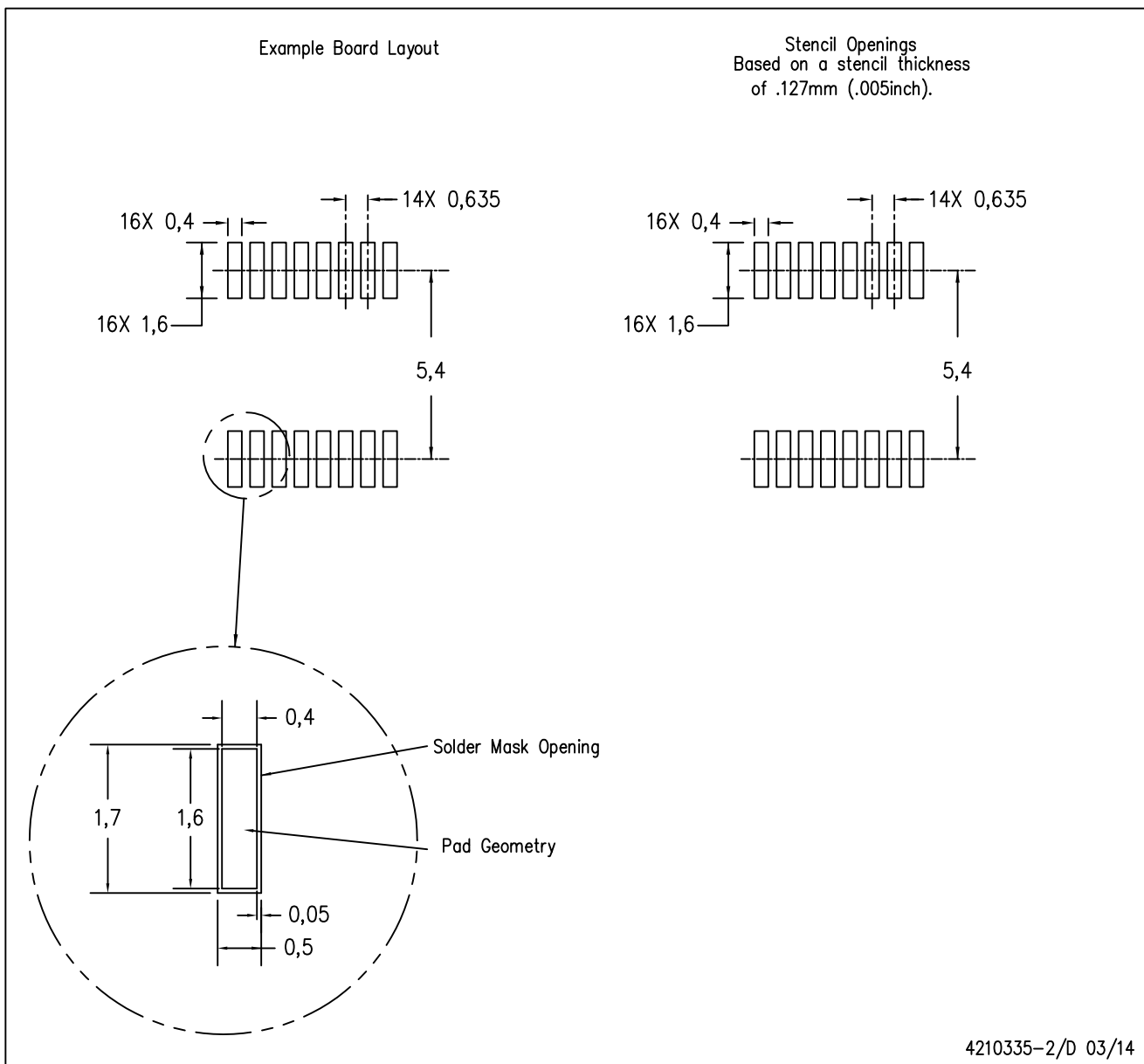
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
  - D. Falls within JEDEC MO-137 variation AB.

DBQ (R-PDSO-G16)

PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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