128Kx32 SRAM MODULE, SMD 5962-93187 & 5962-95595

FEATURES

- Access Times of 15, 17, 20, 25, 35, 45, 55ns
- MIL-STD-883 Compliant Devices Available
- Packaging
  - 66 pin, PGA Type, 1.075" square, Hermetic Ceramic HIP (Package 400)
  - 68 lead, 40mm CQFP (G4T)[1], 3.56mm (0.140") (Package 502)
  - 68 lead, 22.4mm CQFP (G2U), 3.56mm (0.140"), (Package 510)
  - 68 lead, 22.4mm (0.880") square, CQFP (G2L), 5.08mm (0.200") high, (Package 528).
  - 68 lead, 23.9mm Low Profile CQFP (G1U)[1], 3.57mm (0.140"), (Package 519)
  - 68 lead, 23.9mm Low Profile CQFP (G1T), 4.06 mm (0.160"), (Package 524)
- Organized as 128Kx32; User Configurable as 256Kx16 or 512Kx8
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Built in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight:
  WS128K32-XG1UX[1] - 5 grams typical
  WS128K32-XG1TX - 5 grams typical
  WS128K32-XG2UX - 8 grams typical
  WS128K32-XG2LX - 8 grams typical
  WS128K32-XH1X - 13 grams typical
  WS128K32-XG4TX[1] - 20 grams typical
- All devices are upgradeable to 512Kx32

Note 1: Package Not Recommended For New Design

FIG. 1 PIN CONFIGURATION FOR WS128K32N-XH1X

TOP VIEW

1	12	23		34	45	56
I/O8	$\overline{WE}_2$	I/O15		I/O24	VCC	I/O31
I/O9	$\overline{CS}_2$	I/O14		I/O25	$\overline{CS}_4$	I/O30
I/O10	GND	I/O13		I/O26	$\overline{WE}_4$	I/O29
A14	I/O11	I/O12		A7	I/O27	I/O28
A16	A10	$\overline{OE}$		A12	A4	A1
A11	A9	NC		NC	A5	A2
A0	A15	$\overline{WE}_1$		A13	A6	A3
NC	VCC	I/O7		A8	$\overline{WE}_3$	I/O23
I/O0	$\overline{CS}_1$	I/O6		I/O16	$\overline{CS}_3$	I/O22
I/O1	NC	I/O5		I/O17	GND	I/O21
I/O2	I/O3	I/O4		I/O18	I/O19	I/O20
11	22	33		44	55	66

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM

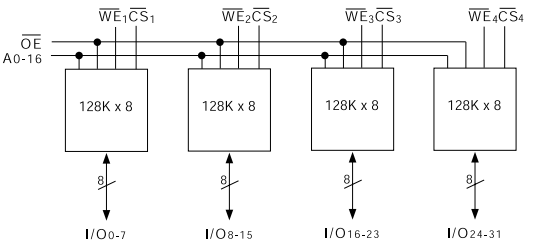
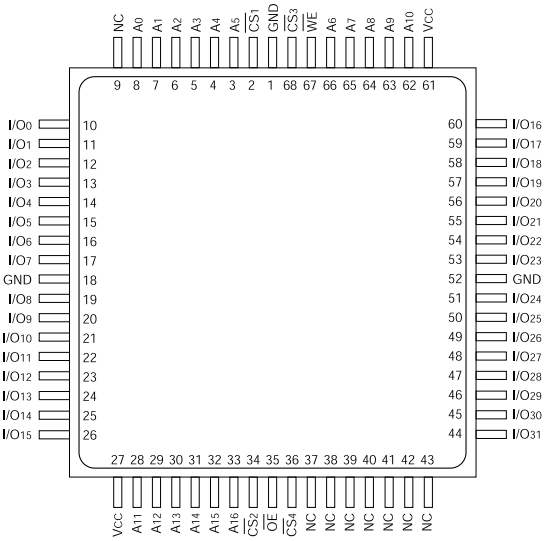


FIG. 2 PIN CONFIGURATION FOR WS128K32-XG4TX[1]

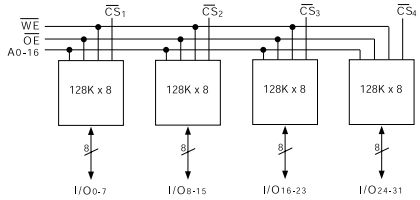
TOP VIEW



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}$	Write Enables
$\overline{CS}$1-4	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

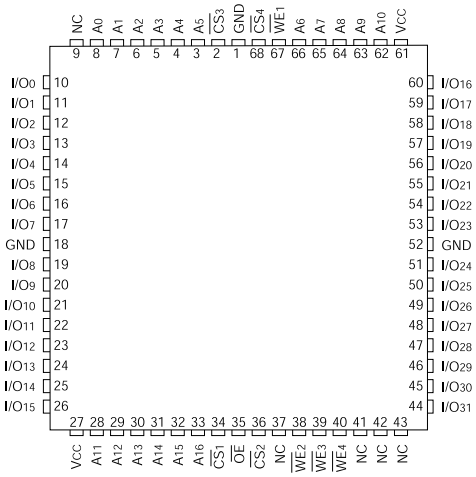
BLOCK DIAGRAM



Note 1: Package Not Recommended For New Design

FIG. 3 PIN CONFIGURATION FOR WS128K32-XG2UX, WS128K32-XG2LX, WS128K32-XG1TX AND WS128K32-XG1UX[1]

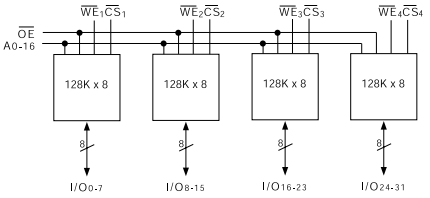
TOP VIEW



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-16	Address Inputs
$\overline{WE}$1-4	Write Enables
$\overline{CS}$1-4	Chip Selects
$\overline{OE}$	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM



Note 1: Package Not Recommended For New Design

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	Vcc+0.5	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.3	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

CAPACITANCE
(TA = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C_{OE}	V_{IN} = 0V, f = 1.0 MHz	50	pF
$\overline{WE}_{1-4}$ capacitance	C_{WE}	V_{IN} = 0V, f = 1.0 MHz		pF
HIP (PGA) H1			20	
CQFP G4T			50	
CQFP G2U/G2L			20	
CQFP G1U/G1T			20	
$\overline{CS}_{1-4}$ capacitance	C_{CS}	V_{IN} = 0V, f = 1.0 MHz	20	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V, f = 1.0 MHz	20	pF
Address input capacitance	C_{AD}	V_{IN} = 0V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS
(VCC = 5.0V, GND = 0V, TA = -55°C TO +125°C)

Parameter	Sym	Conditions	-15		-17		-20		-25		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10		10		10		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10		10		10		10	µA
Operating Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 5.5		600		600		600		600	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 5.5		80		80		80		60	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA, V_{CC} = 4.5		0.4		0.4		0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA, V_{CC} = 4.5	2.4		2.4		2.4		2.4		V

Parameter	Sym	Conditions	-35		-45		-55		Units
			Min	Max	Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10		10		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10		10		10	µA
Operating Supply Current	I_{CC}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 5.5		600		600		600	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 5.5		60		60		60	mA
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA, V_{CC} = 4.5		0.4		0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0mA, V_{CC} = 4.5	2.4		2.4		2.4		V

NOTE: *DC test conditions: VIH = VCC -0.3V, VIL = 0.3V*

DATA RETENTION CHARACTERISTICS (FOR WS128K32L-XXX ONLY)
(TA = -55°C TO +125°C), (TA = -40°C TO +85°C)

Characteristic	Sym	Conditions	Min	Typ	Max	Units
Data Retention Voltage	V_{CC}	V_{CC} = 2.0V	2	-	-	V
Data Retention Quiescent Current	ICCDR	CS ≥ VCC -0.2V	-	1	2	mA
Chip Disable to Data Retention Time (1)	T_{CDR}	V_{IN} ≥ V_{CC} -0.2V	0	-	-	ns
Operation Recovery Time (1)	T_R	or V_{IN} - 0.2V	T_{RC}		-	ns

NOTE: *Parameter guaranteed, but not tested.*

AC CHARACTERISTICS
(V_{CC} = 5.0V, GND = 0V, T_A = -55°C TO +125°C)

Parameter	Symbol	-15		-17		-20		-25		-35		-45		-55		Units
Read Cycle		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		17		20		25		35		45		55		ns
Address Access Time	t_{AA}		15		17		20		25		35		45		55	ns
Output Hold from Address Change	t_{OH}	0		0		0		0		0		0		0		ns
Chip Select Access Time	t_{ACS}		15		17		20		25		35		45		55	ns
Output Enable to Output Valid	t_{OE}		10		10		12		15		20		25		30	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	3		3		3		3		3		3		3		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		0		0		0		0		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		12		12		12		12		20		20		20	ns
Output Disable to Output in High Z	t_{OHZ}[1]		12		12		12		12		20		20		20	ns

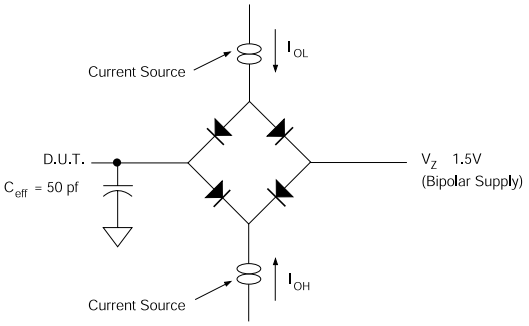
1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS
(V_{CC} = 5.0V, GND = 0V, T_A = -55°C TO +125°C)

Parameter	Symbol	-15		-17		-20		-25		-35		-45		-55		Units
Write Cycle		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		17		20		25		35		45		55		ns
Chip Select to End of Write	t_{CW}	14		14		15		20		25		30		45		ns
Address Valid to End of Write	t_{AW}	14		15		15		20		25		30		45		ns
Data Valid to End of Write	t_{DW}	10		10		12		15		20		25		25		ns
Write Pulse Width	t_{WP}	14		14		15		20		25		30		45		ns
Address Setup Time	t_{AS}	0		0		0		0		0		0		0		ns
Address Hold Time	t_{AH}	0		0		0		0		0		0		0		ns
Output Active from End of Write	t_{OW}[1]	3		3		3		3		4		4		4		ns
Write Enable to Output in High Z	t_{WHZ}[1]		10		10		12		15		20		25		25	ns
Data Hold Time	t_{DH}	0		0		0		0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.

FIG. 4 AC TEST CIRCUIT

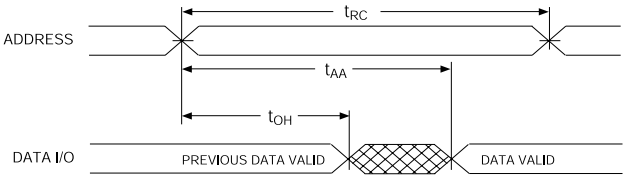


AC TEST CONDITIONS

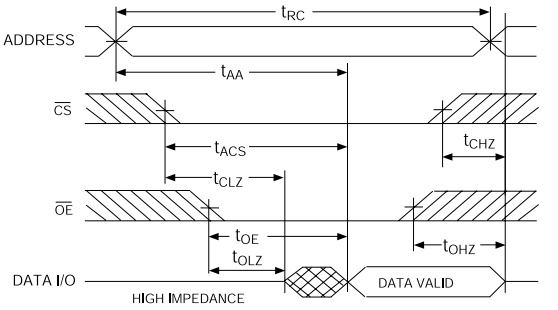
Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:
VZ is programmable from -2V to +7V.
IOL & IOH programmable from 0 to 16mA.
Tester Impedance Z0 = 75 Ω.
VZ is typically the midpoint of VOH and VOL.
IOL & IOH are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

FIG. 5 TIMING WAVEFORM - READ CYCLE

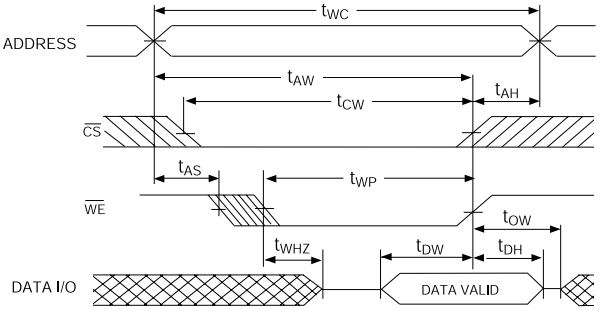


READ CYCLE 1 ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



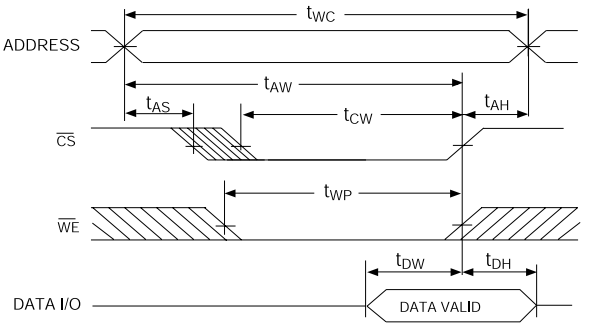
READ CYCLE 2 ($\overline{WE}$ = V_{IH})

FIG. 6 WRITE CYCLE - $\overline{WE}$ CONTROLLED



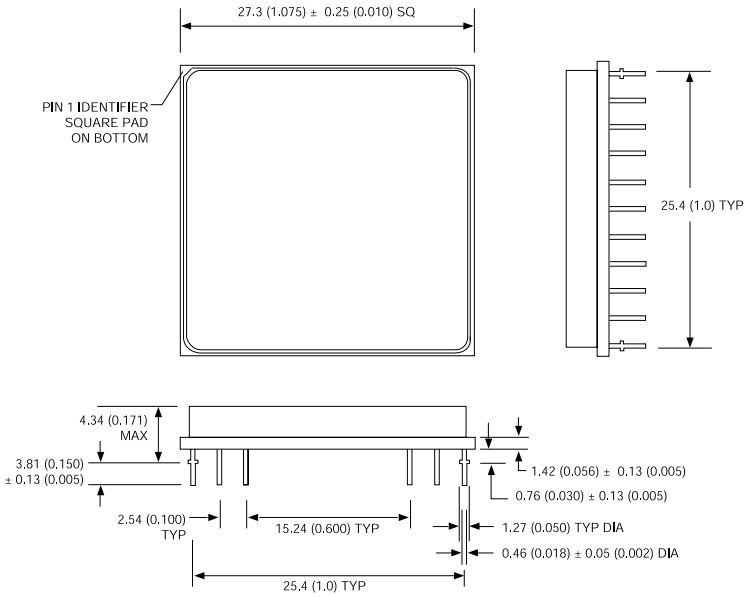
WRITE CYCLE 1, $\overline{WE}$ CONTROLLED

FIG. 7 WRITE CYCLE - $\overline{CS}$ CONTROLLED



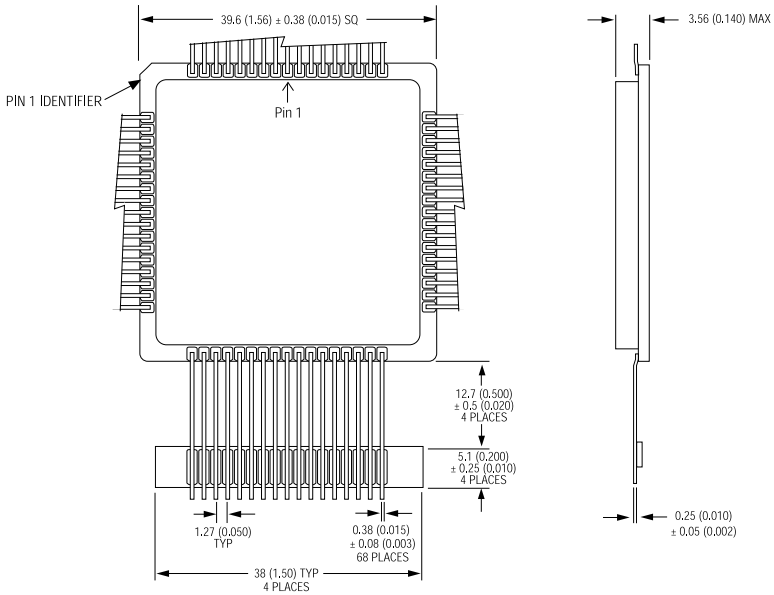
WRITE CYCLE 2, $\overline{CS}$ CONTROLLED

PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

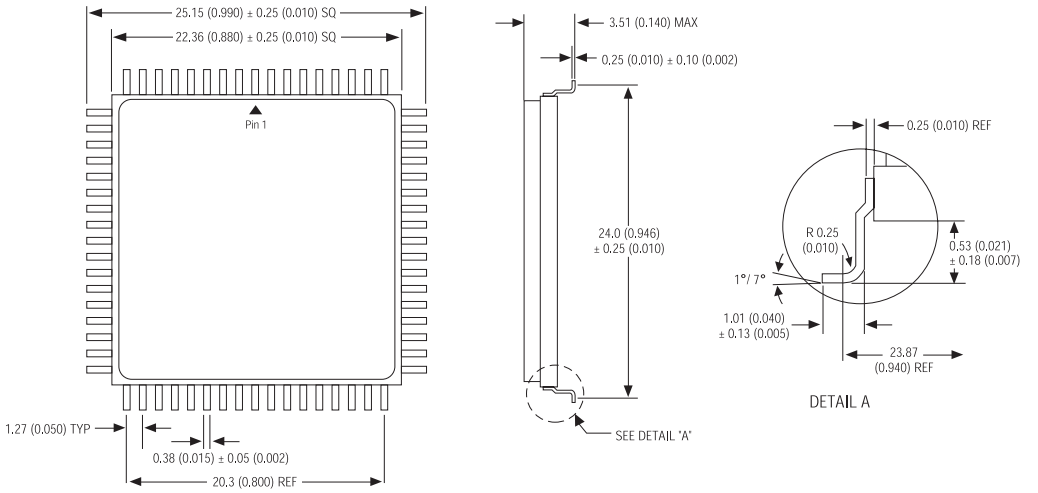
PACKAGE 502: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G4T)[1]



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

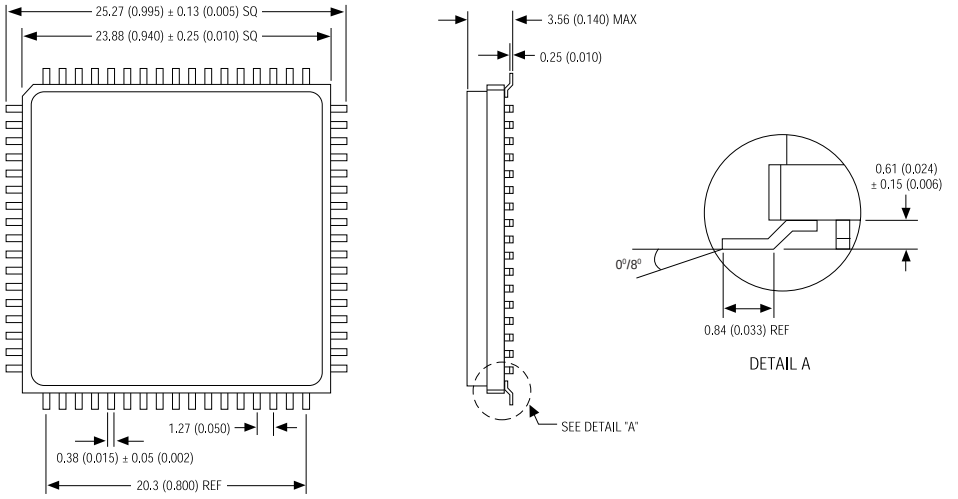
Note 1: Package Not Recommended For New Designs

PACKAGE 510: 68 LEAD, LOW PROFILE CERAMIC QUAD FLAT PACK, CQFP (G2U)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

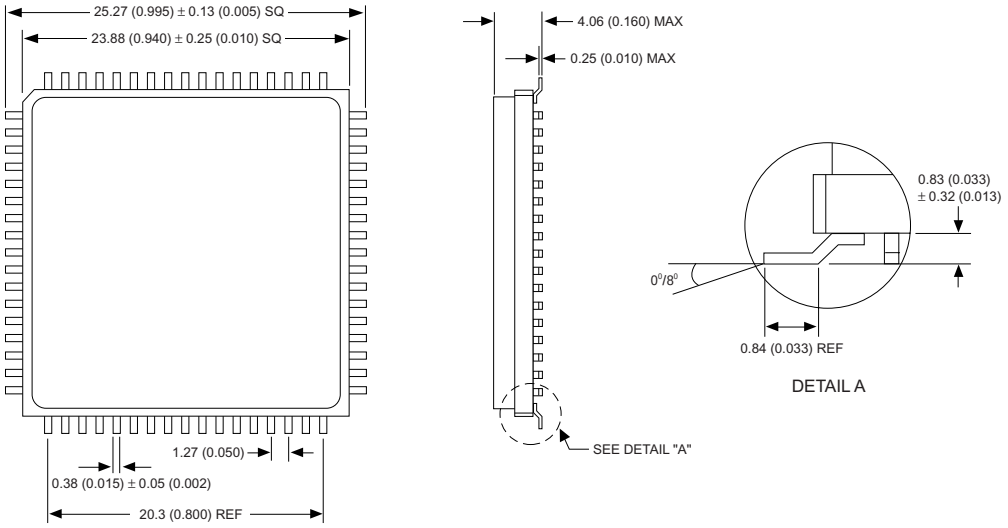
PACKAGE 519: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G1U)[1]



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

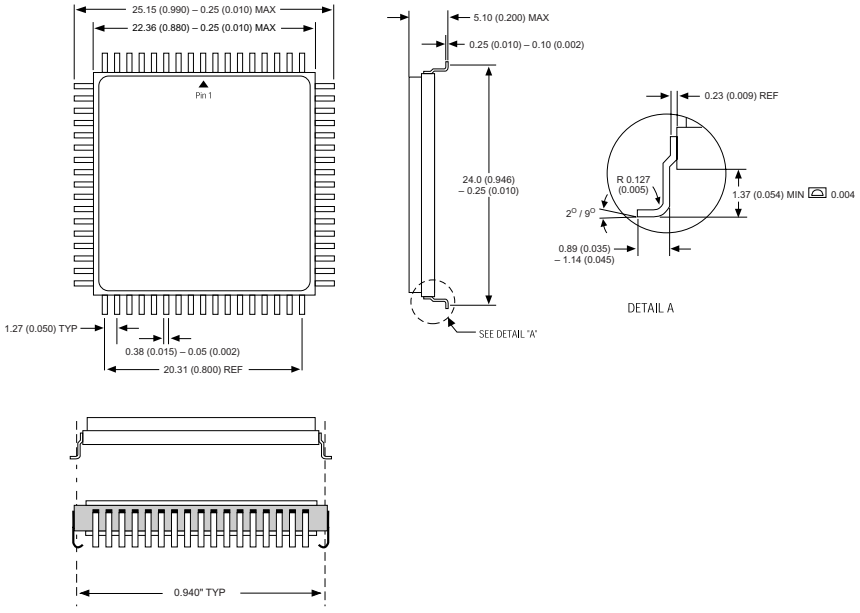
Note 1: Package Not Recommended For New Designs

PACKAGE 524: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G1T)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 528: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2L)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W S 128K 32 X - XXX X X X

LEAD FINISH:
- Blank = Gold plated leads
- A = Solder dip leads

DEVICE GRADE:
- Q = MIL-STD-883 Compliant
- M = Military Screened -55°C to +125°C
- I = Industrial -40°C to +85°C
- C = Commercial 0°C to +70°C

PACKAGE TYPE:
- H1 = 1.075" sq. Ceramic Hex-In-line Package, HIP (Package 400)
- G2U = 22.4mm Ceramic Quad Flat Pack, CQFP (Package 510)
- G2L = 22.4mm Ceramic Quad Flat Pack, CQFP (Package 528)
- G1U[1] = 23.9mm Ceramic Quad Flat Pack, Low Profile CQFP (Package 519)
- G1T = 23.9mm Ceramic Quad Flat Pack, Low Profile CQFP (Package 524)
- G4T[1] = 40 mm Low Profile CQFP (Package 502)

ACCESS TIME (ns)

IMPROVEMENT MARK:
- N = No Connect at pin 8, 21, 28 and 39 in HIP for Upgrades
- L = Low Power

ORGANIZATION, 128Kx32
- User configurable as 256Kx16 or 512Kx8

SRAM

WHITE ELECTRONIC DESIGNS CORPORATION

** Low Power Data Retention only available in G2T Package Type*

Note 1: Package Not Recommended For New Designs

DEVICE TYPE	SPEED	PACKAGE	SMD NO.
128K x 32 SRAM Module	55ns	66 pin HIP (H1)	5962-93187 05H4X
128K x 32 SRAM Module	45ns	66 pin HIP (H1)	5962-93187 06H4X
128K x 32 SRAM Module	35ns	66 pin HIP (H1)	5962-93187 07H4X
128K x 32 SRAM Module	25ns	66 pin HIP (H1)	5962-93187 08H4X
128K x 32 SRAM Module	20ns	66 pin HIP (H1)	5962-93187 09H4X
128K x 32 SRAM Module	17ns	66 pin HIP (H1)	5962-93187 10H4X
128K x 32 SRAM Module	15ns	66 pin HIP (H1)	5962-93187 11H4X
128K x 32 SRAM Module	55ns	68 lead CQFP Low Profile (G4T)[1]	5962-95595 05HYX[1]
128K x 32 SRAM Module	45ns	68 lead CQFP Low Profile (G4T)[1]	5962-95595 06HYX[1]
128K x 32 SRAM Module	35ns	68 lead CQFP Low Profile (G4T)[1]	5962-95595 07HYX[1]
128K x 32 SRAM Module	25ns	68 lead CQFP Low Profile (G4T)[1]	5962-95595 08HYX[1]
128K x 32 SRAM Module	20ns	68 lead CQFP Low Profile (G4T)[1]	5962-95595 09HYX[1]
128K x 32 SRAM Module	17ns	68 lead CQFP Low Profile (G4T)[1]	5962-95595 10HYX[1]
128K x 32 SRAM Module	15ns	68 lead CQFP Low Profile (G4T)[1]	5962-95595 11HYX[1]
128K x 32 SRAM Module	55ns	68 lead CQFP/J (G2U)	5962-95595 05HMX
128K x 32 SRAM Module	45ns	68 lead CQFP/J (G2U)	5962-95595 06HMX
128K x 32 SRAM Module	35ns	68 lead CQFP/J (G2U)	5962-95595 07HMX
128K x 32 SRAM Module	25ns	68 lead CQFP/J (G2U)	5962-95595 08HMX
128K x 32 SRAM Module	20ns	68 lead CQFP/J (G2U)	5962-95595 09HMX
128K x 32 SRAM Module	17ns	68 lead CQFP/J (G2U)	5962-95595 10HMX
128K x 32 SRAM Module	15ns	68 lead CQFP/J (G2U)	5962-95595 11HMX
128K x 32 SRAM Module	55ns	68 lead CQFP/J(G1U)[1]	5962-95595 05H9X
128K x 32 SRAM Module	45ns	68 lead CQFP/J (G1U)[1]	5962-95595 06H9X
128K x 32 SRAM Module	35ns	68 lead CQFP/J (G1U)[1]	5962-95595 07H9X
128K x 32 SRAM Module	25ns	68 lead CQFP/J (G1U)[1]	5962-95595 08H9X
128K x 32 SRAM Module	20ns	68 lead CQFP/J (G1U)[1]	5962-95595 09H9X
128K x 32 SRAM Module	17ns	68 lead CQFP/J (G1U)[1]	5962-95595 10H9X
128K x 32 SRAM Module	15ns	68 lead CQFP/J (G1U)[1]	5962-95595 11H9X
128K x 32 SRAM Module	55ns	68 lead CQFP/J (G2L)	5962-95595 05HAX
128K x 32 SRAM Module	45ns	68 lead CQFP/J(G2L)	5962-95595 06HAX
128K x 32 SRAM Module	35ns	68 lead CQFP/J(G2L)	5962-95595 07HAX
128K x 32 SRAM Module	25ns	68 lead CQFP/J(G2L)	5962-95595 08HAX
128K x 32 SRAM Module	20ns	68 lead CQFP/J(G2L)	5962-95595 09HAX
128K x 32 SRAM Module	17ns	68 lead CQFP/J(G2L)	5962-95595 010HAX
128K x 32 SRAM Module	15ns	68 lead CQFP/J(G2L)	5962-95595 011HAX

Note 1: Package Not Recommended For New Design