MOTOROLA Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14069B

HEX INVERTER

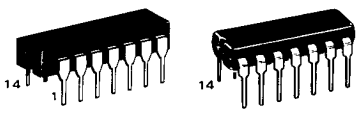
The MC14069B hex inverter is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These inverters find primary use where low power dissipation and/or high noise immunity is desired. Each of the six inverters is a single stage to minimize propagation delays.

- Quiescent Current = 0.5 nA typ/pkg @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typ
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads, One Low-Power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacement for CD4069B

McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

HEX INVERTER



L SUFFIX
CERAMIC PACKAGE
CASE 632

P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

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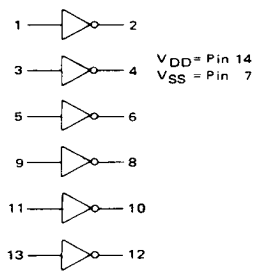
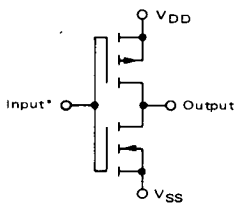
LOGIC DIAGRAM



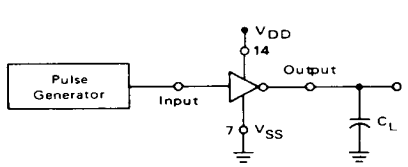
CIRCUIT SCHEMATIC
(1/6 OF CIRCUIT SHOWN)

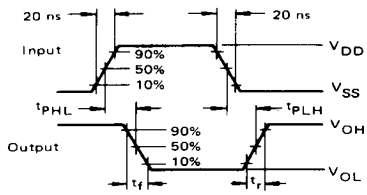


*Double diode protection on all inputs not shown.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

FIGURE 1 — SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 3.6 or 1.4 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.4	
(V_O = 7.2 or 2.8 Vdc)		10	–	3.0	–	4.50	3.0	–	2.9	
(V_O = 11.5 or 3.5 Vdc)		15	–	3.75	–	6.75	3.75	–	3.6	
"1" Level	V_{IH}									
(V_O = 1.4 or 3.6 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 2.8 or 7.2 Vdc)		10	7.1	–	7.0	5.50	–	7.0	–	
(V_O = 3.5 or 11.5 Vdc)		15	11.4	–	11.25	8.25	–	11.25	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	µAdc
		10	–	0.50	–	0.0010	0.50	–	15	
		15	–	1.00	–	0.0015	1.00	–	30	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	1.0	–	0.0005	1.0	–	7.5	µAdc
		10	–	2.0	–	0.0010	2.0	–	15	
		15	–	4.0	–	0.0015	4.0	–	30	
Total Supply Current**† (Dynamic plus Quiescent, Per Gate) (C_L = 50 pF)	I_T	5.0	I_T = (0.3 µA/kHz) f + I_{DD}/6							µAdc
		10	I_T = (0.6 µA/kHz) f + I_{DD}/6							
		15	I_T = (0.9 µA/kHz) f + I_{DD}/6							
Output Rise and Fall Times** (C_L = 50 pF)	t_r,t_f									ns
t_r,t_f = (1.35 ns/pF) C_L + 33 ns		5.0	–	–	–	100	200	–	–	
t_r,t_f = (0.60 ns/pF) C_L + 20 ns		10	–	–	–	50	100	–	–	
t_r,t_f = (0.40 ns/pF) C_L + 20 ns		15	–	–	–	40	80	–	–	
Propagation Delay Times** (C_L = 50 pF)	t_{PLH}, t_{PHL}									ns
t_{PLH},t_{PHL} = (0.90 ns/pF) C_L + 20 ns		5.0	–	–	–	65	125	–	–	
t_{PLH},t_{PHL} = (0.36 ns/pF) C_L + 22 ns		10	–	–	–	40	80	–	–	
t_{PLH},t_{PHL} = (0.26 ns/pF) C_L + 17 ns		15	–	–	–	30	60	–	–	

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 6 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.