STARTECH

ST49C103
ST49C104

Printed September 2, 1994

PREPROGRAMMED FREQUENCY GENERATOR

1

DESCRIPTION

The ST49C103 and ST49C104 are mask programmable monolithic analog CMOS devices designed to generate up to 8 single frequency outputs from a single input clock. The ST49C104 will provide eight different output frequencies and the ST49C103 will provide four different output frequencies. They are designed in a 1.2μ process to achieve 130 MHz speed for high end frequencies.

The ST49C103 and ST49C104 are designed to replace existing video clocks generated from individual oscillators in order to reduce board space and number of oscillators. To provide high speed and low jitter clock, the parts utilize a high speed analog CMOS phase locked loop using 14.318 MHz system clock as the reference clock (note that reference clock can be changed to generate optional frequencies from a standard programmed device). The programmed clock outputs are selectable via three address lines and address latch enable pin. The ST49C104 also includes a power on reset circuit which will cause the select logic to select the frequency at address "000" upon power up. The latch enable pin is also mask programmable to be active high, active low or rising or falling edge sensitive.

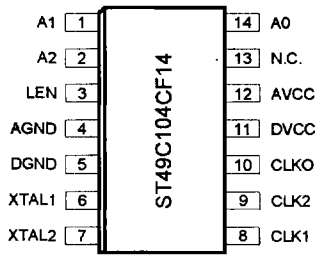
FEATURES

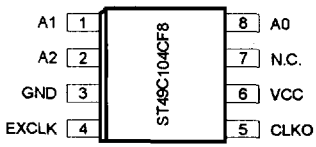
- Can replace up to 8 oscillators/crystals and a multiplexer
- Pin-to-pin compatible to Avasem AV9103/104
- Programmable analog phase locked loop
- Low power single 5V CMOS technology
- 8 or 14 pin DIP or SOIC package.

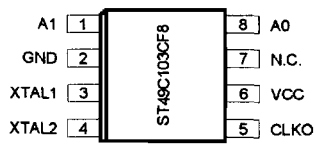
ORDERING INFORMATION

Part number	Package	Operating temperature
ST49C103CP8	Plastic-DIP	0° C to +70° C
ST49C103CF8	SOIC	0° C to +70° C
ST49C104CP8	Plastic-DIP	0° C to +70° C
ST49C104CF8	SOIC	0° C to +70° C
ST49C104CP14	Plastic-DIP	0 ° C to +70° C
ST49C104CF14	SOIC	0° C to +70° C

SOIC Package

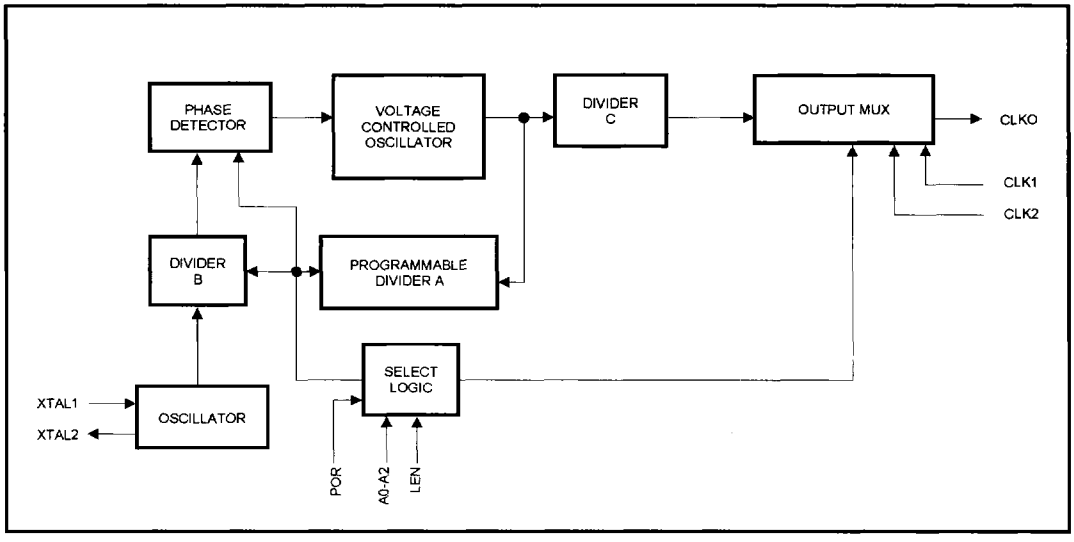






ST49C103/104

BLOCK DIAGRAM



SYMBOL DESCRIPTION (ST49C104 14 pin package)

Symbol	Pin	Signal Type	Pin Description
A1	1	I	Frequency select address input 2.
A2	2*	I	Frequency select address input 3.
LEN	3*	I	Address latch enable input. To latch selected programmed clock output.
AGND	4	O	Analog ground.
DGND	5	O	Digital ground.
XTAL1	6	I	Crystal or external clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external 14.318 MHz clock, XTAL2 is left open or used as buffered clock output.
XTAL2	7	O	Crystal output.
CLK1	8	I	External clock 1 input.
CLK2	9	I	External clock 2 input / output select.
CLKO	10	O	Programmed output clock.
DVCC	11	I	Digital supply voltage. Single +5 volts.
AVCC	12	I	Analog supply voltage. Single +5 volts.
N.C.	13		
A0	14	I	Frequency select address input 1.

* Have internal pull-up resistors on inputs.

ST49C103/104

SYMBOL DESCRIPTION (ST49C104 8 pin package)

Symbol	Pin	Signal Type	Pin Description
A1	1	I	Frequency select address input 2.
A2	2*	I	Frequency select address input 3.
GND	3	O	Digital ground.
EXCLK	4	I	External clock input. Internal phase locked loop reference clock .
CLKO	5	O	Programmed output clock.
VCC	6	I	Digital supply voltage. Single +5 volts.
N.C.	7		
A0	8	I	Frequency select address input 1.

* Has internal pull-up resistor on input

SYMBOL DESCRIPTION (ST49C103 8pin package)

Symbol	Pin	Signal Type	Pin Description
A1	1	I	Frequency select address input 2.
GND	2	O	Digital ground.
XTAL1	3	I	Crystal or external clock input. A crystal can be connected to this pin and XTAL2 pin to generate internal phase locked loop reference clock. For external 14.318 MHz clock, XTAL2 is left open or used as buffered clock output.
XTAL2	4	O	Crystal output.
CLKO	5	O	Programmed output clock.
VCC	6	I	Digital supply voltage. Single +5 volts.
N.C.	7		
A0	8	I	Frequency select address input 1.

ST49C103/104

EXTERNAL CLOCK CONNECTION

To minimize the noise pickup , it is recommended to connect 0.047µF capacitor to XTAL1, and keep the lead length of the capacitor to XTAL1 to a minimum to reduce noise susceptibility.

FREQUENCY SELECT CALCULATION

The ST49C104 contains an analog phase locked loop circuit with digital closed loop dividers and a final output multiplexer to achieve the desired dividing ratios for the clock output.
The accuracy of the frequencies produced by the ST49C104 depends on the input frequency and divider ratios. The formula for calculating the exact output frequency is as follows:

CLKO = (Reference clock) X A/(B.C)

where A=1,2,3,.....127
B=8, 16, 32 ,64
C=1,2,4,8

For proper output frequency, the ST49C104 can accept a reference frequency from 5 - 40 MHz and divider ratio up to 15.

MASK OPTIONS

The following mask options are provided for custom applications.

* Latch Enable can be edge triggered or level sensitive.
* Latch Enable can be active high or active low.
* Any frequency can be in any decoding position.
* CLK 1 and CLK 2 can be included in decoding table.
* CLK2 can control selection of either CLK 1 or the internal frequencies.

FEATURE	ST49C104 14-pin	ST49C104 8-pin	ST49C103 8-pin
8 output frequencies	X	X	
4 output frequencies			X
Programmable LEN pin	X	X	X
Clock input only		X	
Crystal or clock input	X		X
CLK1, CLK2 available for output mux	X		

Address latch (LEN)	State
ST49C104-1	Transparent for LEN high
ST49C104-2	Transparent for LEN low
ST49C104-3	Transparent for LEN low

ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND-0.3 V to VCC+0.3 V
Operating temperature	0° C to +70° C
Storage temperature	-40° C to +150° C
Package dissipation	500 mW

DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits Min	Typ	Max	Units	Conditions
V_{IL}	Input low level			0.8	V	
V_{IH}	Input high level	2.0			V	
V_{OL}	Output low level			0.4	V	I_{OL} = 8.0 mA
V_{OH}	Output high level	2.4			V	I_{OH} = 8.0 mA
I_{IL}	Input low current			-350	µA	Except crystal input
I_{IH}	Input high current			1	µA	V_{IN}=Vcc
I_{CC}	Operating current		20	30	mA	No load. DCLK=80MHz
R_{IN}	Input pull-up resistance	15	20	25	KΩ	

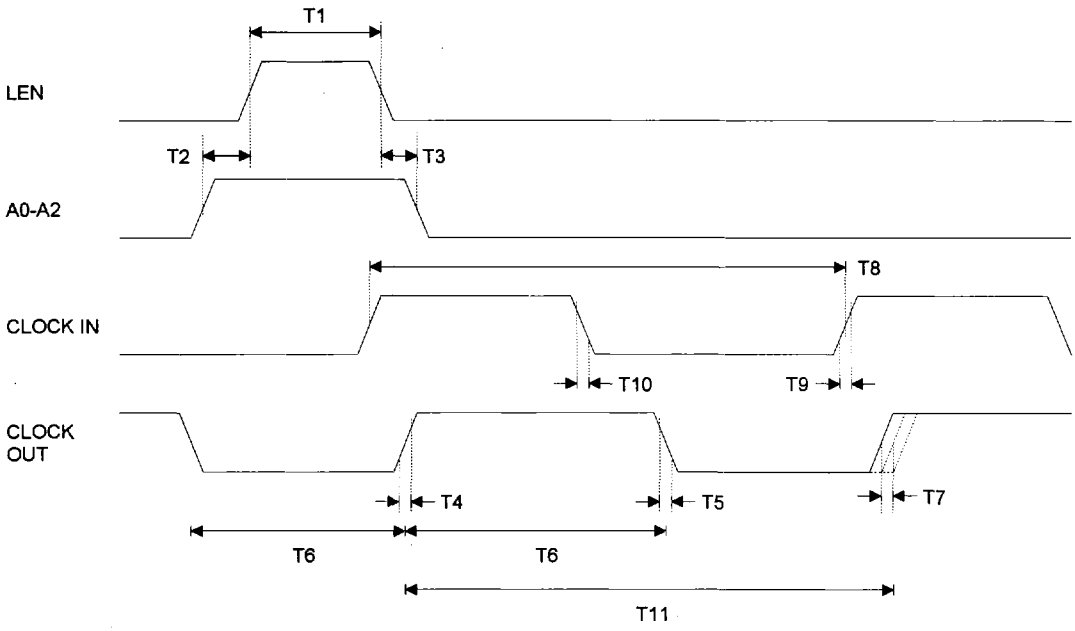
ST49C103/104

AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70° C, Vcc=5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits			Units	Conditions
		Min	Typ	Max		
T_1	Enable pulse width	20			ns	
T_2	Setup time data to enable	20			ns	
T_3	Hold time to data enable	10			ns	
T_4	Rise time		1	1.5	ns	0.8V - 2.0V
T_5	Fall time		1	1.5	ns	2.0V - 0.8V
T_6	Duty cycle	40	48/52	60	%	1.4V switch point
T_6	Duty cycle	45	48/52	55	%	Vcc/2 switch point
T_7	Jitter		±175	±300	ps	
T_8	Input frequency	14.318		32	MHz	
T_9	Input clock rise time			20	ns	
T_{10}	Input clock fall time			20	ns	
T_{11}	Output frequency change		0.005		%	

TIMING DIAGRAM



ST49C103/104

A2 A1 A0	ST49C104-1		ST49C104-2		ST49C104-3		ST49C104-5*		ST49C103**	
	NOMINAL	ACTUAL	NOMINAL	ACTUAL	NOMINAL	ACTUAL	NOMINAL	ACTUAL	NORMAL	ACTUAL
0 0 0	Xtal	Xtal	25.175	25.280	50.350	50.560	39.000	39.000	32.000	32.00
0 0 1	16.257	16.331	28.322	28.412	56.664	56.824	25.000	25.000	40.00	40.00
0 1 0	Clk2	Clk2	32.514	32.663	65.028	65.326	30.750	30.750	50.00	50.00
0 1 1	32.514	32.663	36.000	35.795	72.000	71.590	26.250	26.250	1.00	1.00
1 0 0	25.175	25.056	40.000	39.822	80.000	79.640	32.000	32.000	N/A	
1 0 1	28.322	28.412	44.900	44.744	89.800	89.488	25.250	25.250	N/A	
1 1 0	24.000	23.938	50.000	50.113	75.000	75.169	31.250	31.250	N/A	
1 1 1	40.000	39.822	65.000	65.326	108.00	108.280	37.500	37.500	N/A	

A2 A1 A0	ST49C104-6**					
	NOMINAL	ACTUAL				
0 0 0	25.500	25.500				
0 0 1	16.500	16.500				
0 1 0	20.750	20.750				
0 1 1	22.500	22.500				
1 0 0	24.500	24.500				
1 0 1	19.500	19.500				
1 1 0	15.000	15.000				
1 1 1	14.000	14.000				

Input clock frequency = 14.318 MHz
* Input clock frequency = 16.0 MHz
** Input clock frequency = 8.0 MHz