

ACT-S512K32 High Speed 16 Megabit SRAM Multichip Module

Features

- 4 Low Power CMOS 512K x 8 SRAMs in one MCM
- Factory configured as 512K x 32; User configurable as 1M x 16 or 2M x 8
- Input and Output TTL & CMOS Compatible Design
- Fast 17,20,25,35,45,55ns Access Times
- Full Commercial, Industrial and Military (-55°C to +125°C) Temperature Range
- MIL-PRF-38534 Compliant MCMs Available
- +5 V Power Supply
- Available in two Surface Mount Packages, and two PGA Type Package
 - 68-Lead, Low Profile CQFP(F1), 1.56"SQ x .140"max
 - 68-Lead, Dual-Cavity CQFP(F2), 0.88"SQ x .20"max
(.18 max thickness available, contact factory for details)
(Drops into the 68 Lead JEDEC .99"SQ CQFJ footprint)
 - 68-Lead, Single-Cavity CQFP (F18), .94"SQ x .140"max (Drops into the 68 Lead JEDEC .99"SQ CQFJ footprint)
 - 66 Pin, 1.38" x 1.38" x .245" PGA Type, Aeroflex code# "P1"
 - 66 Pin, 1.09" x 1.09" x .185" PGA Type, With Shoulder, Aeroflex code# "P7"
- Internal Decoupling Capacitors
- DESC SMD# 5962-94611 Released (F1,F2,F18,P1,P7)


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General Description

The ACT-S512K32 is a High Speed, 16 megabit CMOS SRAM Multichip Module (MCM) designed for full temperature range industrial, military, or space, mass memory and fast cache applications.

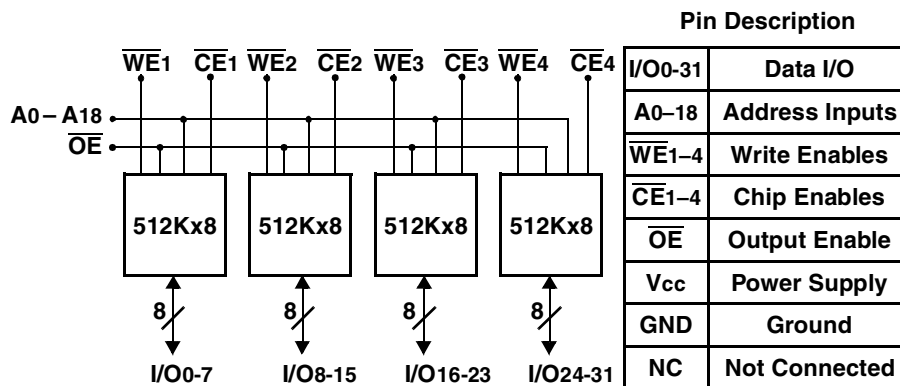
The MCM can be organized as a 512K x 32 bit, 1M x 16 bit or 2M x 8 bit device and is input and output TTL compatible. Writing is executed when the write enable (WE) and chip enable (CE) inputs are low and output enable (OE) input is high. Reading is accomplished when WE is high and CE and OE are both low. Access time grades of 17ns, 20ns, 25ns, 35ns, 45ns and 55ns maximum are standard high speed versions.

The +5 Volt power supply version is standard and +3.3 Volt lower power model is a future optional product.

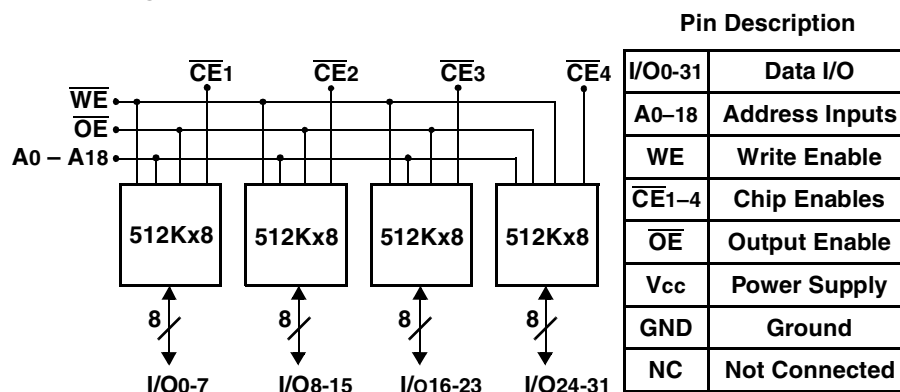
The products are designed for operation over the temperature range of -55°C to +125°C and under the full military environment. DESC Standard Military Drawing (SMD) numbers are released.

The ACT-S512K32 is manufactured in Aeroflex's 80,000 square foot MIL-PRF-38534 certified facility in Plainview, N.Y.

Block Diagram – PGA Type Package (P1,P7) & CQFP (F2,F18)



Block Diagram – CQFP(F1)



Absolute Maximum Ratings

Symbol	Rating	Range	Units
T _c	Operating Temperature	-55 to +125	°C
T _{STG}	Storage Temperature	-65 to +150	°C
P _D	Maximum Package Power Dissipation	3.0	W
θ _{J-C}	Hottest Die, Max Thermal Resistance - Junction to Case	5	°C/W
V _G	Maximum Signal Voltage to Ground	-0.5 to +7	V
T _L	Maximum Lead Temperature (10 seconds)	300	°C

Normal Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
V _{CC}	Power Supply Voltage	+4.5	+5.5	V
V _{IH}	Input High Voltage	+2.2	V _{CC} + 0.3	V
V _{IL}	Input Low Voltage	-0.5	+0.8	V

Capacitance

(V_{IN} = 0V, f = 1MHz, T_c = 25°C)

Symbol	Parameter	Maximum	Units
C _{AD}	A ₀ – A ₁₈ Capacitance	50	pF
C _{OE}	OE Capacitance	50	pF
C _{WE}	CQFP (F1) Package	50	pF
	PGA (P1 & P7) and CQFP (F2 & F18) Packages	20	pF
C _{CE}	Chip Enable Capacitance	20	pF
C _{I/O}	I/O ₀ – I/O ₃₁ Capacitance	20	pF

This parameter is guaranteed by design but not tested

DC Characteristics

(V_{CC} = 5.0V, V_{SS} = 0V, T_c = -55°C to +125°C, unless otherwise indicated)

Parameter	Sym	Conditions	ALL Speeds		Units
			Min	Max	
Input Leakage Current	I _{LI}	V _{CC} = +5.5V, V _{IN} = 0 or V _{CC}	-	10	μA
Output Leakage Current	I _{LO}	CE = V _{IH} , OE = V _{IH} , V _{OUT} = 0 to V _{CC}	-	10	μA
Operating Supply Current 32 Bit Mode	I _{CC1x32}	CE = V _{IL} , OE = V _{IH} , V _{CC} = +5.5V f = 5 MHz CMOS Compatible	-	600	mA
Standby Current	I _{SB1}	CE = V _{CC} , OE = V _{IH} , V _{CC} = +5.5V f = 5 MHz CMOS Compatible	-	80	mA
Operating Supply Current 32 Bit Mode	I _{CC2x32}	CE = V _{IL} , OE = V _{IH} , V _{CC} = +5.5V f = 50 MHz CMOS Compatible	-	700	mA
Standby Current	I _{SB2}	CE = V _{CC} , OE = V _{IH} , V _{CC} = +5.5V f = 50 MHz CMOS Compatible	-	280	mA
Output Low Voltage	V _{OL}	I _{OL} = 8 mA, V _{CC} = +4.5V	-	0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0 mA, V _{CC} = +4.5V	2.4	-	V

AC Characteristics

(V_{CC} = 5.0V, V_{SS} = 0V, T_c = -55°C to +125°C)

Read Cycle

Parameter	Sym	-017		-020		-025		-035		-045		-055		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	17	-	20	-	25	-	35	-	45	-	55	-	ns
Address Access Time	t _{AA}	-	17	-	20	-	25	-	35	-	45	-	55	ns
Chip Enable Access Time	t _{ACE}	-	17	-	20	-	25	-	35	-	45	-	55	ns
Output Hold from Address Change	t _{OH}	0	-	0	-	0	-	0	-	0	-	0	-	ns
Output Enable to Output Valid	t _{OE}	-	9	-	10	-	12	-	25	-	25	-	25	ns
Chip Enable to Output in Low Z *	t _{CLZ}	2	-	2	-	2	-	4	-	4	-	4	-	ns
Output Enable to Output in Low Z *	t _{OLZ}	0	-	0	-	0	-	0	-	0	-	0	-	ns
Chip Deselect to Output in High Z *	t _{CHZ}	-	12	-	12	-	12	-	15	-	20	-	20	ns
* Output Disable to Output in High Z	t _{OHZ}	-	12	-	12	-	12	-	15	-	20	-	20	ns

* Parameters guaranteed by design but not tested

Write Cycle

Parameter	Sym	-017		-020		-025		-035		-045		-055		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	17	-	20	-	25	-	35	-	45	-	55	-	ns
Chip Enable to End of Write	t _{CW}	15	-	15	-	17	-	25	-	35	-	50	-	ns
Address Valid to End of Write	t _{AW}	15	-	15	-	17	-	25	-	35	-	50	-	ns
Data Valid to End of Write	t _{DW}	11	-	12	-	13	-	20	-	25	-	25	-	ns
Write Pulse Width	t _{WP}	15	-	15	-	17	-	25	-	35	-	40	-	ns
Address Setup Time	t _{AS}	2	-	2	-	2	-	2	-	2	-	2	-	ns
Output Active from End of Write *	t _{OW}	2	-	3	-	4	-	4	-	5	-	5	-	ns
Write to Output in High Z *	t _{WHZ}	-	9	-	11	-	13	-	15	-	20	-	20	ns
Data Hold from Write Time	t _{DH}	0	-	0	-	0	-	0	-	0	-	0	-	ns
Address Hold Time	t _{AH}	0	-	0	-	0	-	0	-	5	-	5	-	ns

* Parameters guaranteed by design but not tested

Data Retention Electrical Characteristics (Special Order Only)

(T_c = -55°C to +125°C)

Parameter	Sym	Test Conditions	All Speeds		Units
			Min	Max	
V _{CC} for Data Retention	V _{DR}	$\overline{CE} \geq V_{CC} - 0.2V$	2	5.5	V
Data Retention Current	I _{CCDR1}	V _{CC} = 3V	-	28	mA

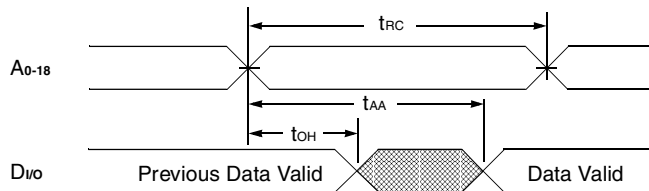
Truth Table

Mode	\overline{CE}	\overline{OE}	\overline{WE}	Data I/O	Power
Standby	H	X	X	High Z	Standby (deselect/power down)
Read	L	L	H	Data Out	Active
Output Disable	L	H	H	High Z	Active (deselected)
Write	L	X	L	Data In	Active

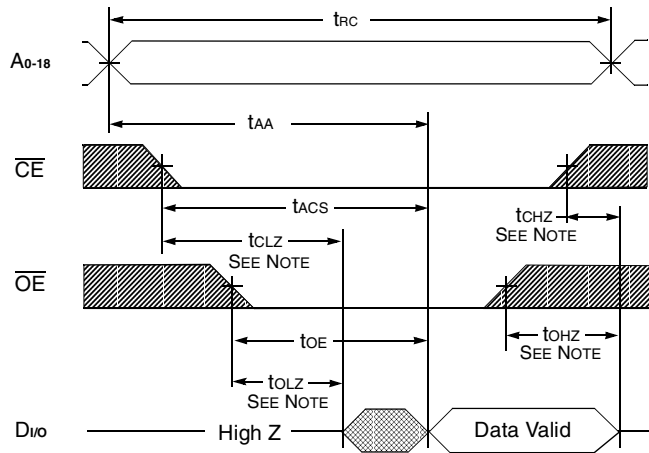
Timing Diagrams

Read Cycle Timing Diagrams

Read Cycle 1 ($\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$)

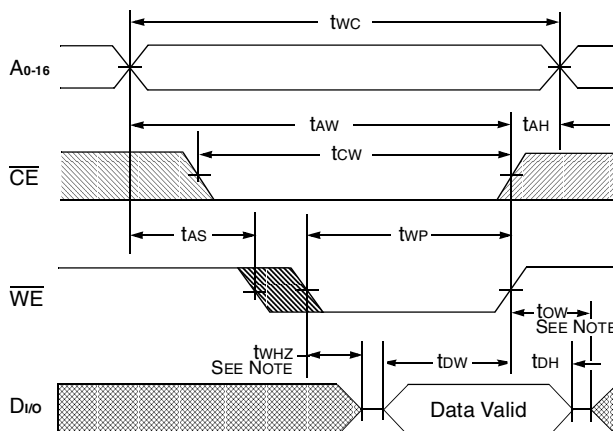


Read Cycle 2 ($\overline{WE} = V_{IH}$)

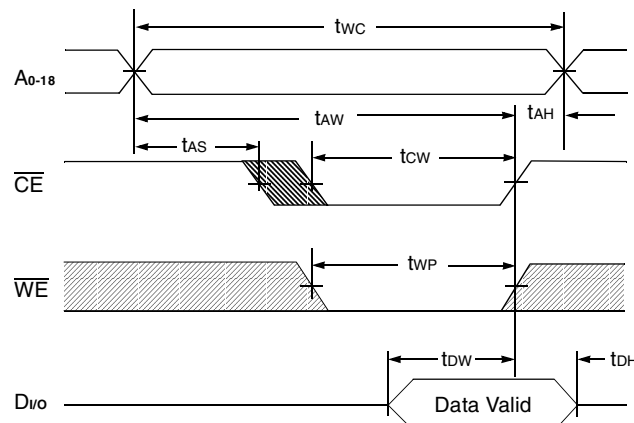


Write Cycle Timing Diagrams

Write Cycle 1 (\overline{WE} Controlled, $\overline{OE} = V_{IL}$)

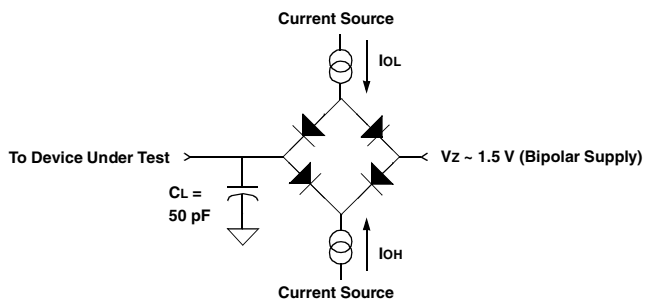


Write Cycle 2 (\overline{CE} Controlled, $\overline{OE} = V_{IH}$)



Note: Guaranteed by design, but not tested.

AC Test Circuit



Parameter	Typical	Units
Input Pulse Level	0 – 3.0	V
Input Rise and Fall	5	ns
Input and Output Timing Reference Level	1.5	V

Notes:

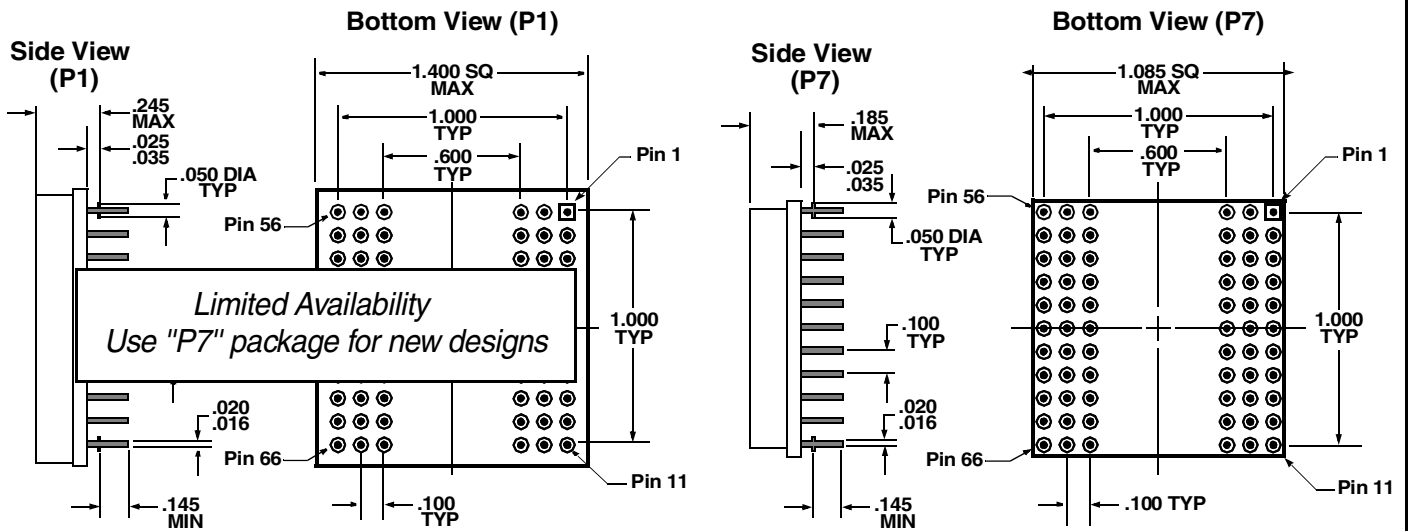
- 1) Vz is programmable from -2V to +7V.
- 2) IoL and IoH programmable from 0 to 16 mA.
- 3) Tester Impedance Zo = 75Ω.
- 4) Vz is typically the midpoint of VOH and VOL.
- 5) IoL and IoH are adjusted to simulate a typical resistance load circuit.
- 6) ATE Tester includes jig capacitance.

Pin Numbers & Functions

66 Pins — PGA-Type							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	I/O8	18	A12	35	I/O25	52	\overline{WE}_3
2	I/O9	19	V _{CC}	36	I/O26	53	\overline{CE}_3
3	I/O10	20	\overline{CE}_1	37	A6	54	GND
4	A13	21	NC	38	A7	55	I/O19
5	A14	22	I/O3	39	NC	56	I/O31
6	A15	23	I/O15	40	A8	57	I/O30
7	A16	24	I/O14	41	A9	58	I/O29
8	A17	25	I/O13	42	I/O16	59	I/O28
9	I/O0	26	I/O12	43	I/O17	60	A0
10	I/O1	27	\overline{OE}	44	I/O18	61	A1
11	I/O2	28	A18	45	V _{CC}	62	A2
12	\overline{WE}_2	29	\overline{WE}_1	46	\overline{CE}_4	63	I/O23
13	\overline{CE}_2	30	I/O7	47	\overline{WE}_4	64	I/O22
14	GND	31	I/O6	48	I/O27	65	I/O21
15	I/O11	32	I/O5	49	A3	66	I/O20
16	A10	33	I/O4	50	A4		
17	A11	34	I/O24	51	A5		

Package Outline — PGA-Type "P1"

Package Outline — PGA-Type "P7"

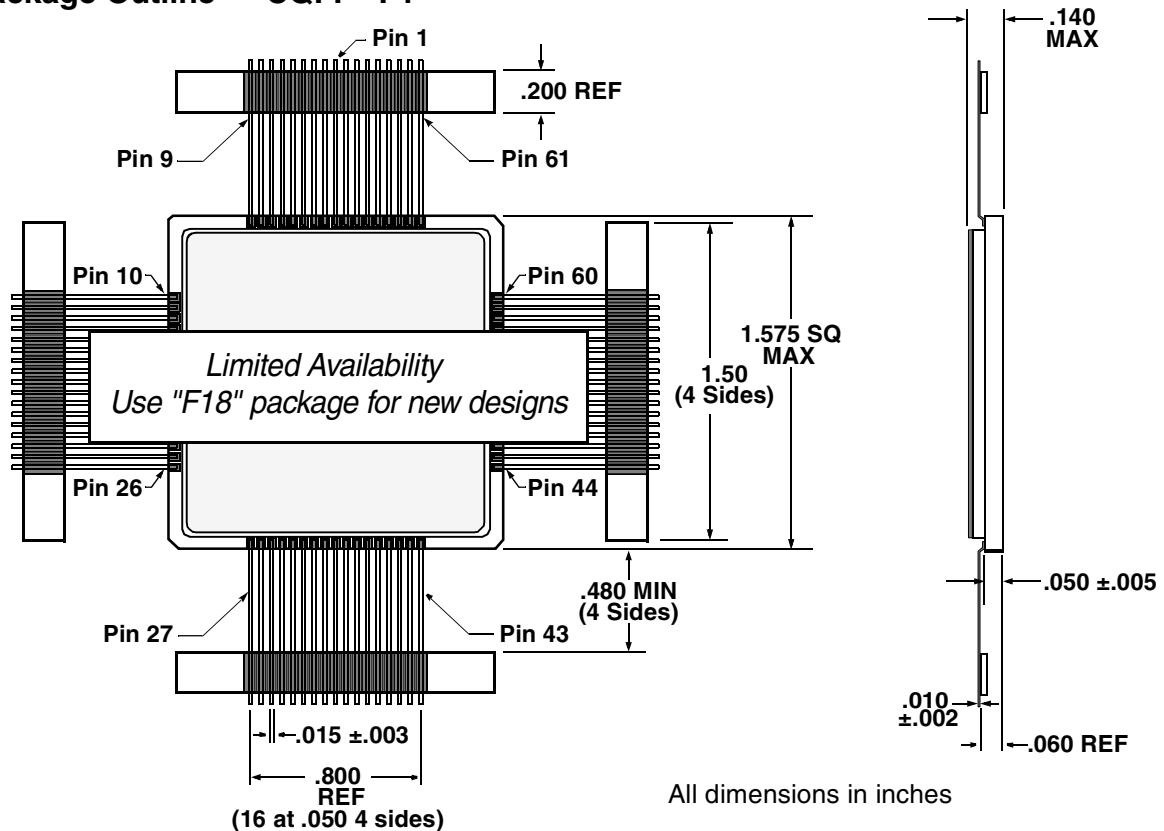


All dimensions in inches

Pin Numbers & Functions

68 Pins — CQFP							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	GND	18	GND	35	\overline{OE}	52	GND
2	\overline{CE}_1	19	I/O8	36	\overline{CE}_4	53	I/O23
3	A5	20	I/O9	37	A17	54	I/O22
4	A4	21	I/O10	38	A18	55	I/O21
5	A3	22	I/O11	39	NC	56	I/O20
6	A2	23	I/O12	40	NC	57	I/O19
7	A1	24	I/O13	41	NC	58	I/O18
8	A0	25	I/O14	42	NC	59	I/O17
9	NC	26	I/O15	43	NC	60	I/O16
10	I/O0	27	V _{CC}	44	I/O31	61	V _{CC}
11	I/O1	28	A11	45	I/O30	62	A10
12	I/O2	29	A12	46	I/O29	63	A9
13	I/O3	30	A13	47	I/O28	64	A8
14	I/O4	31	A14	48	I/O27	65	A7
15	I/O5	32	A15	49	I/O26	66	A6
16	I/O6	33	A16	50	I/O25	67	\overline{WE}
17	I/O7	34	\overline{CE}_2	51	I/O24	68	\overline{CE}_3

Package Outline — CQFP "F1"

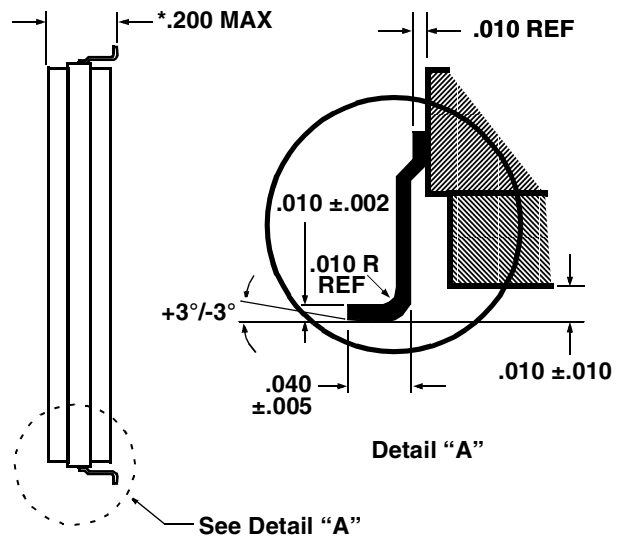
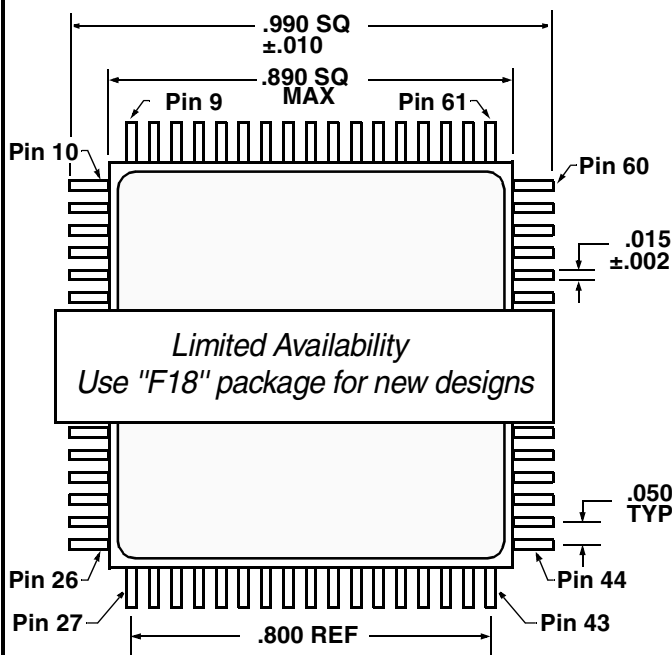


Pin Numbers & Functions

68 Pins — Dual-Cavity CQFP							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	GND	18	GND	35	\overline{OE}	52	GND
2	\overline{CE}_3	19	I/O8	36	\overline{CE}_2	53	I/O23
3	A5	20	I/O9	37	A17	54	I/O22
4	A4	21	I/O10	38	\overline{WE}_2	55	I/O21
5	A3	22	I/O11	39	\overline{WE}_3	56	I/O20
6	A2	23	I/O12	40	\overline{WE}_4	57	I/O19
7	A1	24	I/O13	41	A18	58	I/O18
8	A0	25	I/O14	42	NC	59	I/O17
9	NC	26	I/O15	43	NC	60	I/O16
10	I/O0	27	V _{CC}	44	I/O31	61	V _{CC}
11	I/O1	28	A11	45	I/O30	62	A10
12	I/O2	29	A12	46	I/O29	63	A9
13	I/O3	30	A13	47	I/O28	64	A8
14	I/O4	31	A14	48	I/O27	65	A7
15	I/O5	32	A15	49	I/O26	66	A6
16	I/O6	33	A16	50	I/O25	67	\overline{WE}_1
17	I/O7	34	\overline{CE}_1	51	I/O24	68	\overline{CE}_4

Package Outline — Dual-Cavity CQFP "F2"

Top View



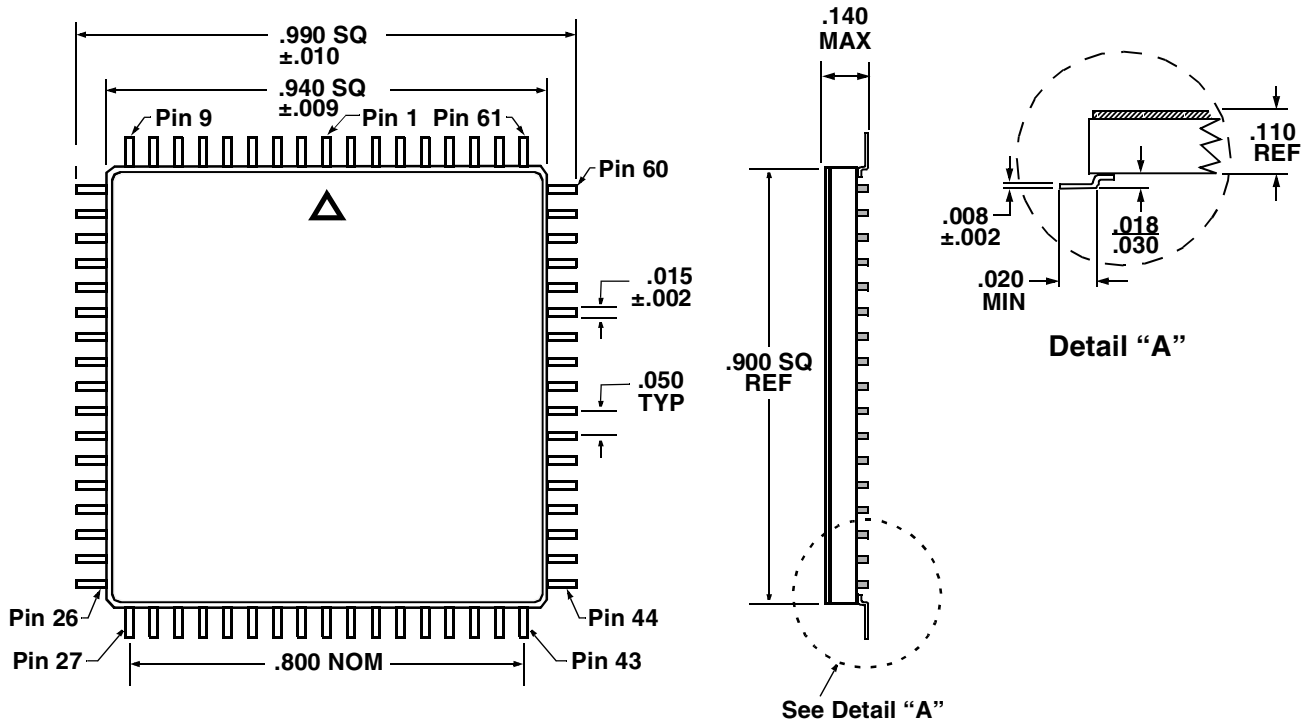
*.180 MAX available, call factory for details

All dimensions in inches

Pin Numbers & Functions

68 Pins — Single-Cavity CQFP							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	GND	18	GND	35	\overline{OE}	52	GND
2	\overline{CE}_3	19	I/O ₈	36	\overline{CE}_2	53	I/O ₂₃
3	A ₅	20	I/O ₉	37	A ₁₇	54	I/O ₂₂
4	A ₄	21	I/O ₁₀	38	\overline{WE}_2	55	I/O ₂₁
5	A ₃	22	I/O ₁₁	39	\overline{WE}_3	56	I/O ₂₀
6	A ₂	23	I/O ₁₂	40	\overline{WE}_4	57	I/O ₁₉
7	A ₁	24	I/O ₁₃	41	A ₁₈	58	I/O ₁₈
8	A ₀	25	I/O ₁₄	42	NC	59	I/O ₁₇
9	NC	26	I/O ₁₅	43	NC	60	I/O ₁₆
10	I/O ₀	27	V _{CC}	44	I/O ₃₁	61	V _{CC}
11	I/O ₁	28	A ₁₁	45	I/O ₃₀	62	A ₁₀
12	I/O ₂	29	A ₁₂	46	I/O ₂₉	63	A ₉
13	I/O ₃	30	A ₁₃	47	I/O ₂₈	64	A ₈
14	I/O ₄	31	A ₁₄	48	I/O ₂₇	65	A ₇
15	I/O ₅	32	A ₁₅	49	I/O ₂₆	66	A ₆
16	I/O ₆	33	A ₁₆	50	I/O ₂₅	67	\overline{WE}_1
17	I/O ₇	34	\overline{CE}_1	51	I/O ₂₄	68	\overline{CE}_4

Package Outline — CQFP Single Cavity "F18"



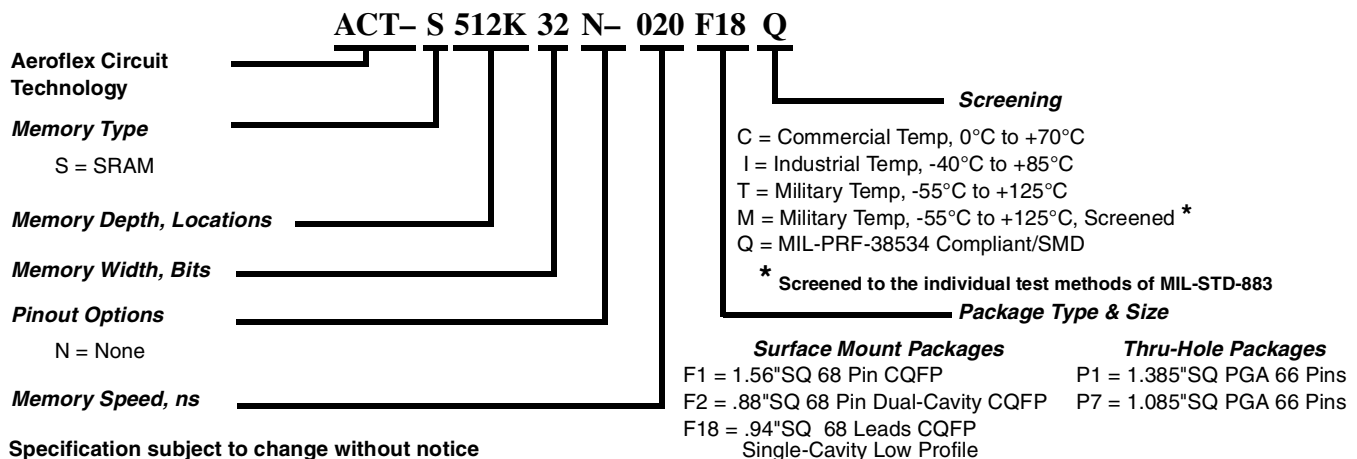
All dimensions in inches



Ordering Information

Model Number	DESC Part Number	Speed	Package
ACT-S512K32N-017F1Q	5962-9461110HYC	17ns	1.56"sq CQFP
ACT-S512K32N-020F1Q	5962-9461109HYC	20ns	1.56"sq CQFP
ACT-S512K32N-025F1Q	5962-9461108HYC	25ns	1.56"sq CQFP
ACT-S512K32N-034F1Q	5962-9461107HYC	35ns	1.56"sq CQFP
ACT-S512K32N-045F1Q	5962-9461106HYC	45ns	1.56"sq CQFP
ACT-S512K32N-055F1Q	5962-9461105HYC	55ns	1.56"sq CQFP
ACT-S512K32N-017F2Q	5962-9461110HMC	17ns	.88"sq CQFP
ACT-S512K32N-020F2Q	5962-9461109HMC	20ns	.88"sq CQFP
ACT-S512K32N-025F2Q	5962-9461108HMC	25ns	.88"sq CQFP
ACT-S512K32N-035F2Q	5962-9461107HMC	35ns	.88"sq CQFP
ACT-S512K32N-045F2Q	5962-9461106HMC	45ns	.88"sq CQFP
ACT-S512K32N-055F2Q	5962-9461105HMC	55ns	.88"sq CQFP
ACT-S512K32N-017F18Q	5962-9461110H9C	17ns	.94"sq CQFP
ACT-S512K32N-020F18Q	5962-9461109H9C	20ns	.94"sq CQFP
ACT-S512K32N-025F18Q	5962-9461108H9C	25ns	.94"sq CQFP
ACT-S512K32N-035F18Q	5962-9461107H9C	35ns	.94"sq CQFP
ACT-S512K32N-045F18Q	5962-9461106H9C	45ns	.94"sq CQFP
ACT-S512K32N-055F18Q	5962-9461105H9C	55ns	.94"sq CQFP
ACT-S512K32N-017P1Q	5962-9461110HXC	17ns	1.38"sq PGA-Type
ACT-S512K32N-020P1Q	5962-9461109HXC	20ns	1.38"sq PGA-Type
ACT-S512K32N-025P1Q	5962-9461108HXC	25ns	1.38"sq PGA-Type
ACT-S512K32N-035P1Q	5962-9461107HXC	35ns	1.38"sq PGA-Type
ACT-S512K32N-045P1Q	5962-9461106HXC	45ns	1.38"sq PGA-Type
ACT-S512K32N-055P1Q	5962-9461105HXC	55ns	1.38"sq PGA-Type
ACT-S512K32N-017P7Q	5962-9461110HTC	17ns	1.09"sq PGA-Type
ACT-S512K32N-020P7Q	5962-9461109HTC	20ns	1.09"sq PGA-Type
ACT-S512K32N-025P7Q	5962-9461108HTC	25ns	1.09"sq PGA-Type
ACT-S512K32N-035P7Q	5962-9461107HTC	35ns	1.09"sq PGA-Type
ACT-S512K32N-045P7Q	5962-9461106HTC	45ns	1.09"sq PGA-Type
ACT-S512K32N-055P7Q	5962-9461105HTC	55ns	1.09"sq PGA-Type

Model Number Breakdown



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